SETTING THE STANDARDS
15 YEARS

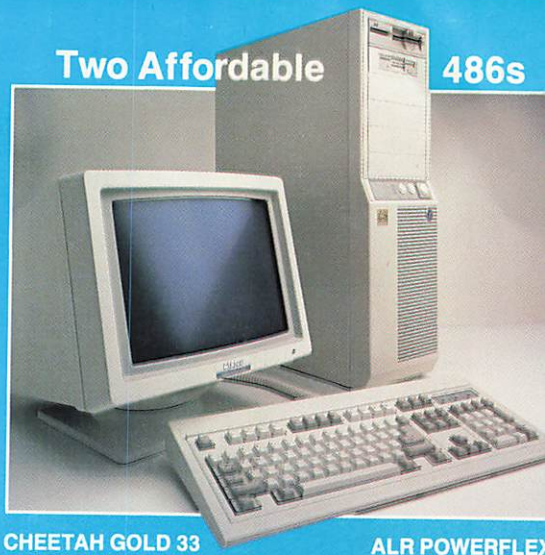
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A McGRAW-HILL PUBLICATION

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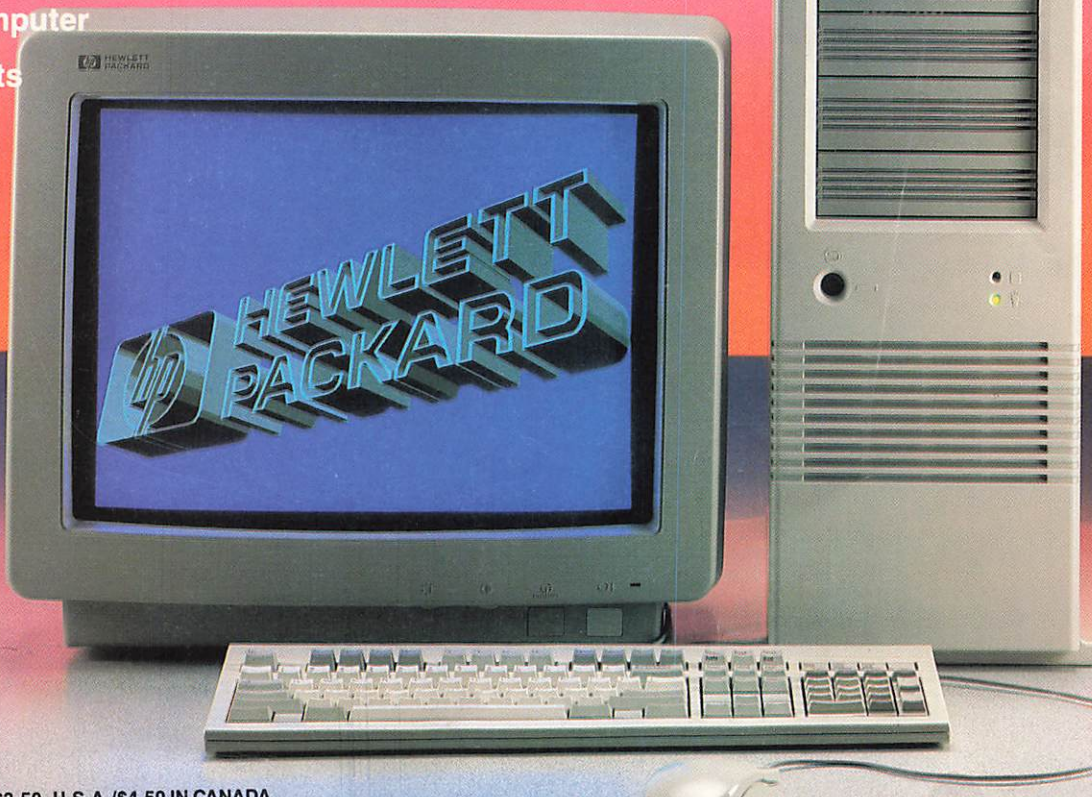
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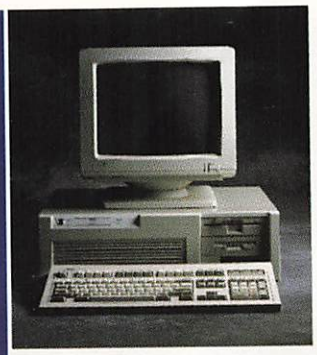
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Two Diskless Workstations



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THE DELL SYSTEM® 310
20 MHz 386.

The best combination of performance and value available in its class.

STANDARD FEATURES:

- Intel 80386 microprocessor running at 20 MHz.
- Choice of 1 MB, 2 MB, or 4 MB of RAM* expandable to 16 MB (using a dedicated high-speed 32-bit memory slot).
- Advanced Intel 82385 Cache Memory Controller with 32 KB of high speed static RAM cache.
- Page mode interleaved memory architecture.
- VGA systems include a high performance 16-bit video adapter.
- Socket for 20 MHz Intel 80387 or 20 MHz WEITEK 3167 math coprocessor.
- 5.25" 1.2 MB or 3.5" 1.44 MB diskette drive.
- Dual diskette and hard drive controller.
- Enhanced 101-key keyboard.
- 1 parallel and 2 serial ports.
- 200-watt power supply.
- 8 industry standard expansion slots (6 available).

Lease for as low as $131/month.
△ Extended Service Plan pricing starts at $251.

40 MB TTL Monochrome System	$3,599
40 MB VGA Color Plus System	$4,099
100 MB VGA Color Plus System	$4,699
100 MB Super VGA Color System (800x600)	$4,799

Prices listed reflect 1 MB of RAM. 150 and 322 MB hard drive configurations also available.

Performance Enhancements (Systems 325, 310, 316 and 220): within the first megabyte of memory, 384 KB of memory is reserved for use by the system to enhance performance. 4 MB configurations available on all systems. Call for pricing.



THE DELL SYSTEM® 316
16 MHz 386SX.™

Expandable, affordable access to 386 architecture.

STANDARD FEATURES:

- Intel 80386SX microprocessor running at 16 MHz.
- Choice of 1 MB, 2 MB, or 4 MB of RAM* expandable to 16 MB (8 MB on the system board).
- Page mode interleaved memory architecture.
- VGA systems include a high performance 16-bit video adapter.
- LIM 4.0 support for memory over 1 MB.
- Socket for 16 MHz Intel 80387SX math coprocessor.
- 5.25" 1.2 MB or 3.5" 1.44 MB diskette drive.
- Integrated high performance hard disk drive interface and diskette controller on system board. (ESDI based systems include a hard disk controller.)
- Enhanced 101-key keyboard.
- 1 parallel and 2 serial ports.
- 200-watt power supply.
- 8 industry standard expansion slots (7 available).

Lease for as low as $98/month.
△ Extended Service Plan pricing starts at $234.

40 MB TTL Monochrome System	$2,699
40 MB VGA Color Plus System	$3,199
100 MB VGA Color Plus System	$3,799
100 MB Super VGA Color System (800x600)	$3,899

Prices listed reflect 1 MB of RAM. 150 and 322 MB hard drive configurations also available.



THE DELL SYSTEM® 220
20 MHz 286.

It's faster than many 386 computers, and has a smaller footprint.

STANDARD FEATURES:

- 80286 microprocessor running at 20 MHz.
- Choice of 1 MB, 2 MB, or 4 MB of RAM* expandable to 16 MB (8 MB on system board).
- Page mode interleaved memory architecture.
- LIM 4.0 support for memory over 1 MB.
- Integrated diskette and VGA video controller on system board.
- Socket for Intel 80287 math coprocessor.
- One 3.5" 1.44 MB diskette drive.
- Integrated high performance hard disk interface on system board.
- Enhanced 101-key keyboard.
- 1 parallel and 2 serial ports (integrated on system board).
- 3 full-sized 16-bit AT expansion slots available.

Lease for as low as $109/month.
△ Extended Service Plan pricing starts at $264.

40 MB VGA Monochrome System	$2,999
40 MB VGA Color Plus System	$3,299
100 MB VGA Monochrome System	$3,599
100 MB VGA Color Plus System	$3,899

Prices listed reflect 1 MB of RAM. External 5.25" 1.2 MB diskette drive available.



THE NEW DELL SYSTEM® 210
12.5 MHz 286.

The price says this is an entry-level system. The performance says it's a lot more.

STANDARD FEATURES:

- 80286 microprocessor running at 12.5 MHz.
- Choice of 512 KB, 640 KB,†† 1 MB, or 2 MB of RAM expandable to 16 MB (6 MB on system board).
- Page mode interleaved memory architecture.
- LIM 4.0 support for memory over 640 KB.
- Integrated diskette and high performance 16-bit VGA video controller on system board.
- Socket for Intel 80287 math coprocessor.
- 5.25" 1.2 MB or 3.5" 1.44 MB diskette drive.
- Integrated high performance hard disk interface on system board.
- Enhanced 101-key keyboard.
- 1 parallel and 2 serial ports.
- 3 full-sized 16-bit AT expansion slots available.

Lease for as low as $64/month.
△ Extended Service Plan pricing starts at $190.

20 MB VGA Monochrome System	$1,699
20 MB VGA Color Plus System	$1,999
40 MB VGA Monochrome System	$1,899
40 MB VGA Color Plus System	$2,199

Prices listed reflect 512 KB of RAM.
††640 KB versions of the above systems are available for an additional $80.
100 MB hard drive configurations also available.

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SAVE NOW ON THE DELL SYSTEM® 325 25 MHz 386.

AN EVEN BETTER VALUE AT THESE NEW LOW PRICES.



STANDARD FEATURES:

- Intel 80386 microprocessor running at 25 MHz.
- Choice of 1 MB, 2 MB, or 4 MB of RAM* expandable to 16 MB (using a dedicated high-speed 32-bit memory slot).
- Advanced Intel 82385 Cache Memory Controller with 32 KB of high speed static RAM cache.
- Page mode interleaved memory architecture.
- VGA systems include a high performance 16-bit video adapter.
- Socket for 25 MHz Intel 80387 or 25 MHz WEITEK 3167 math coprocessor.
- 5.25" 1.2 MB or 3.5" 1.44 MB diskette drive.
- Dual diskette and hard drive controller.
- Enhanced 101-key keyboard.
- 1 parallel and 2 serial ports.
- 200-watt power supply.
- 8 industry standard expansion slots (6 available).

Lease for as low as $178/month.
△Extended Service Plan pricing starts at $370.

40 MB VGA Monochrome System	$4,899
100 MB VGA Color Plus System	$5,799
100 MB Super VGA Color System (800x600)	$5,899
150 MB Super VGA Color System (800x600)	$6,399

Prices listed reflect 1 MB of RAM. 322 MB hard drive configurations also available.

All systems are photographed with optional extras.

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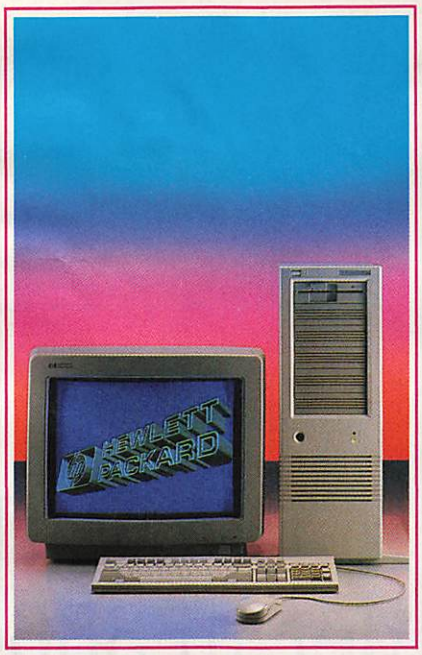
Excel for OS/2 with Presentation Manager, *Microsoft's spreadsheet for OS/2*
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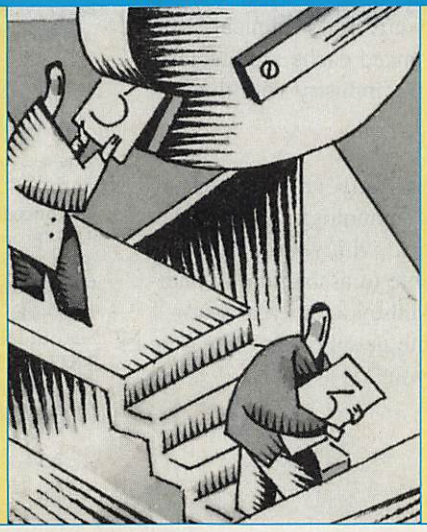
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California Anza-Borrego Desert State Park

(Cannonball-shaped sandstone, These concretions are formed of onion-skin layers of minerals resistant to erosion.)

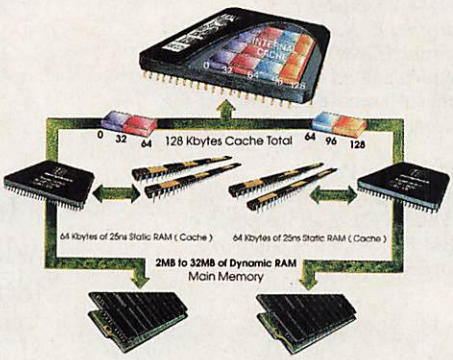
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PowerCache 4 is the first PC to fully utilize 128-bit burst mode and a "read and write-back" 128KB cache design, providing better than zero wait state performance as compared to the i386.

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power4 Cache ...The most advanced
What else would you expect

PC MAGAZINE, *January 1989,*
"In a field of powerhouse machines there can only be one winner, and ALR's FlexCache is it."

INFO WORLD, *July 1989,*
"ALR Systems Unleash 486 Power. The PowerCache 4 shines in the CPU-specific portion of the InfoWorld Automated Benchmark Test, gaining a score of 16.3."

PC WEEK, *July 1989,*
"Based on a series of benchmarks run last week on Advanced Logic Research, Inc.'s prototype 486 desktop system, ALR will enter the 486 market with a bang."

At ALR, we will never rest on our laurels. We strive to be the best, as proven by our past achievements. Now with the introduction of the new ALR PowerCache 4™, we've designed a system that is far beyond comparison. Again, we have taken PC-microprocessing power a step further by designing a unique proprietary PowerCache 4 cache controller using ALR's custom ASIC chips which deliver the fastest processing speed ever.

More important, PowerCache 4 is the first PC to fully utilize 128-bit burst mode and a "read and write-back" 128KB cache design, providing a better than zero wait state performance as compared to the i386. Furthermore, the ALR PowerCache 4 is 100% IBM® PS/2™ Micro Channel™-compatible supporting bus mastering devices and giving

	ALR M130 Desktop	ALR M150, M350 M650 Floor-Standing	IBM M70-A21 Power Platform™
CPU	25 MHz i486	25 MHz i486	25 MHz i486
Bus	MCA	MCA	MCA
External Cache	128 KB cache Read and Write-Back	128 KB cache Read and Write-Back	None
Video Opt. on board	640x480 1024x768	640x480 1024x768	640x480 None
I/O Slots	6 expansion slots	6 expansion slots	3 expansion slots
Storage Expansion	4-3 1/2"	1-full height 2-1/2"-height 2-3 1/2" drives	3-3 1/2" drives
Disk Capacity	130 MB-260 MB	150 MB-650 MB	110 MB
Price	$9,990	Starting at $11,490	$12,990

paper-white screen, VGA Color Plus, or Super VGA for high resolution colors displayed on a larger screen.

Even though the 325 gives you all this performance, it still leaves you six open slots for whatever else you might want to add.

And once you've told us what you want, we'll make sure what you want works—by burning-in the entire system unit.

COMPUTER RETAILERS ARE NO KNOWS.

There are some good reasons computer retailers won't know much about the System 325.

First, with all the new and increasingly sophisticated systems they have to keep up with on a daily basis, you can hardly expect them to know everything.

Second, because Dell sells direct.

Which means you now have the unique opportunity to talk directly with the people who make them. And ask things like, "What is page mode interleaved memory?" or, "How much SIMM RAM should I add?"

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WE COME WHEN WE'RE CALLED.

One of the things that very clearly sets Dell systems apart from other computers is not just how they're sold but how they're supported.

Overkill was one description used in a recent PC Week article.

Perhaps.

But then, we think you'll agree, when something goes wrong, you want as much help as possible, right?

BEST OF ALL, YOU WON'T HAVE TO EXPLAIN TO A COMPUTER RETAILER WHAT ALL THAT MEANS.

Which is why every Dell system comes with a toll-free technical support line and self-diagnostic software. We're able to solve 90% of all problems right over the phone. The other 10% receive next-day, deskside service. Thanks to our new alliance with Xerox Corporation.

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As you've probably guessed, one of the things that drives us most is customer satisfaction.

So we'd like to give you the ultimate guarantee:

Try a System 325 in your office for a month. Run your toughest applications. Put it through its paces, at your pace. If you're not completely satisfied, send it back anytime within 30 days. And we'll refund your money.

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No matter how many reasons we give you to buy a Dell system, sometimes it makes more sense to lease one instead.

Whether you need a single computer, or an entire office full, there is a leasing plan for your business that is just like 100% financing.

And just as we can custom configure your computers, we can see to it you get a custom designed lease plan to fit your exact business needs.† A fact that has not gone unnoticed. Especially by the Fortune 500. Over half of whom now own or lease Dell systems.

And just as we welcome their business, we welcome your business, too.

Just call us, toll-free. And don't be afraid to ask us the tough questions.

That's the part we like best.

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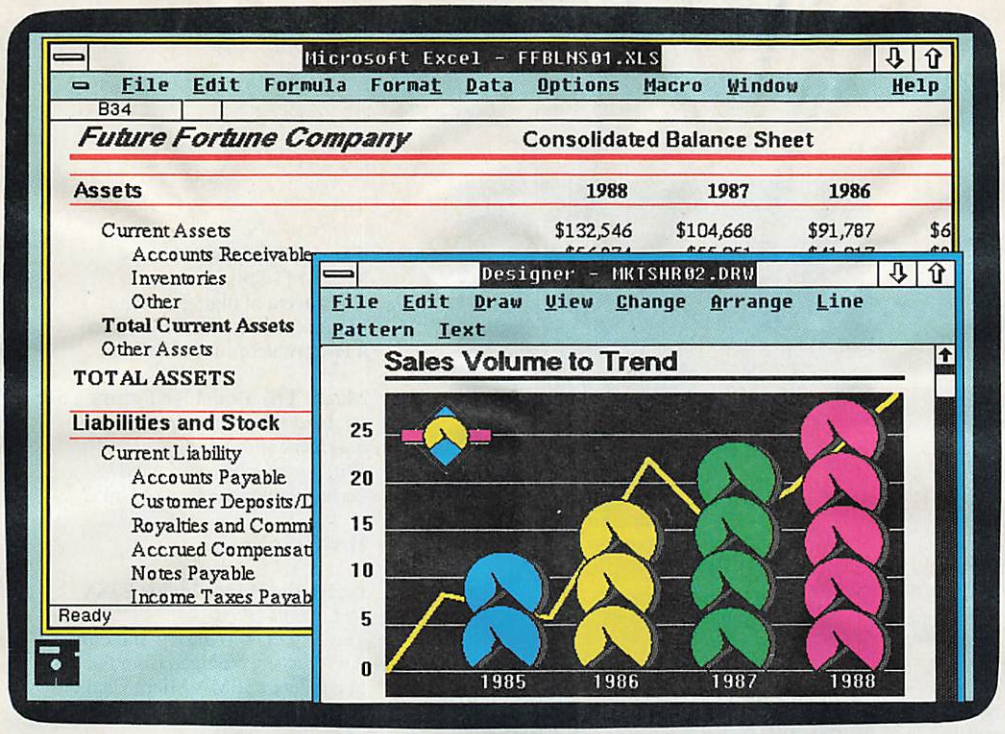
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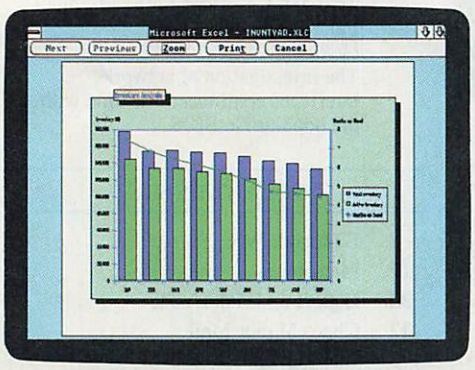
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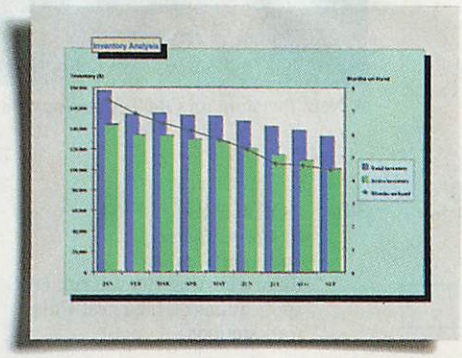
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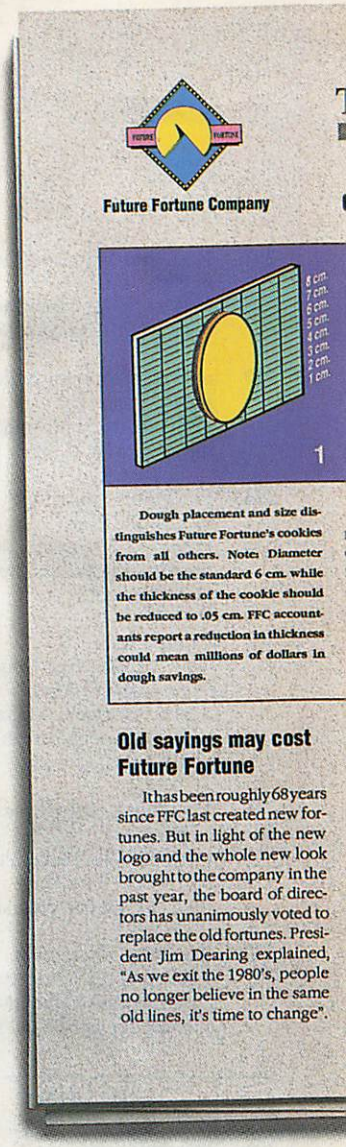
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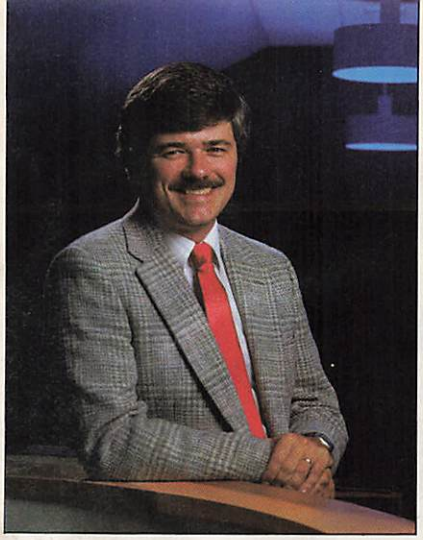
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WHAT SLUMP?

The end of the year produces a flood of new products

You've probably heard naysayers speaking of a slump in the computer industry. One aspect of a slump is a drop in sales volume, a critical issue to vendors, but not what matters most to end users.

Rather, it's the drop-off in innovation and a slowing in the pace of product announcements that can be unsettling to those of us who are hungry for ways to improve our own productivity and that of our companies.

On toward midyear, there were three or four months where nothing much seemed to be happening. We saw some minor upgrades arrive, some new niche products emerge, a couple of disappointing releases of long-delayed major products, and a relative handful of really interesting, meaningful new products. I don't know about you, but toward the end of the summer, I was thinking dark thoughts about the state of innovation in our industry.

50 EISA and/or 80486 Machines?

But with the arrival of fall, new products and technologies are crawling out of the oxide. Just one example: By the end of this month, we expect to see something like 50 new machines using either the new Extended Industry Standard Architecture bus or the 80486. Some, like the Hewlett-Packard Vectra 486 machine that appears on this month's cover, use both.

Machines based on the 80486 are springing up in such abundance that we're already seeing price wars: See this month's First Impressions of amazingly low-cost 80486 boxes from Cheetah and ALR.

A Unix Workstation for Cheap

Innovation isn't limited to Intel-architecture machines, however. Although the 68040 is still not available to compete against the 80486, some nice 68030-based systems are appearing.

For example, Apollo (which is now a subsidiary of Hewlett-Packard) recently introduced the first full-featured 68030-based Unix (System V version 3) workstation priced at less than $4000.

The new Apollo Series 2500 personal workstation "entry-level" system, which lists for $3990, includes a 20-MHz Motorola 68030, a 68882 floating-point coprocessor, 4 megabytes of RAM, and a 15-inch paper-white display with a maximum resolution of 1024 by 780 pixels. All the features of the 2500 are built onto a single motherboard that is approximately the size of a full-size IBM PC AT board.

This model comes without a disk drive because most 2500s will be networked: Apollo built Ethernet, IBM Token Ring, and Apollo Token Ring support into the 2500. (You can, however, add a drive if you choose.)

Consulting editor Stan Miastkowski, who covered the story for BYTE*week* and Microbytes Daily, reports that Apollo hopes to ship the new system by the end of this year.

Chip Advances

There's some welcome activity at the chip level, too, which portends some interesting new products in the not-too-distant future.

For example, Intel announced a new version of its 80960 embedded microprocessor, one that can execute up to three instructions at a time. The result, according to Intel, is a 33-MHz CPU with a top speed of nearly 100 million instructions per second and a routine speed of some 66 MIPS.

The microprocessor is likely to begin showing up in some computation-intensive PC peripherals in the next year, including scanners and laser-printer controllers. That should radically improve the speed of laser printers when they're printing using page-description languages like PostScript.

Rival Motorola announced the 68302 Integrated Multiprotocol Processor, a low-power CMOS package that runs at 16.67 MHz and includes a 68000 processor, a microcoded RISC-based communications controller, three independent serial I/O channels (each with two on-chip direct-memory-access channels), RAM, and a special-purpose synchronous communications port that allows the 68302 to interface directly with components like microcontrollers, digital signal processors, and coders/decoders. The 68302 will be used in a wide range of applications, including LANs, fax machines, modems, telephone switching equipment, computer I/O systems, and even satellite communications equipment.

Speaking of LANs...

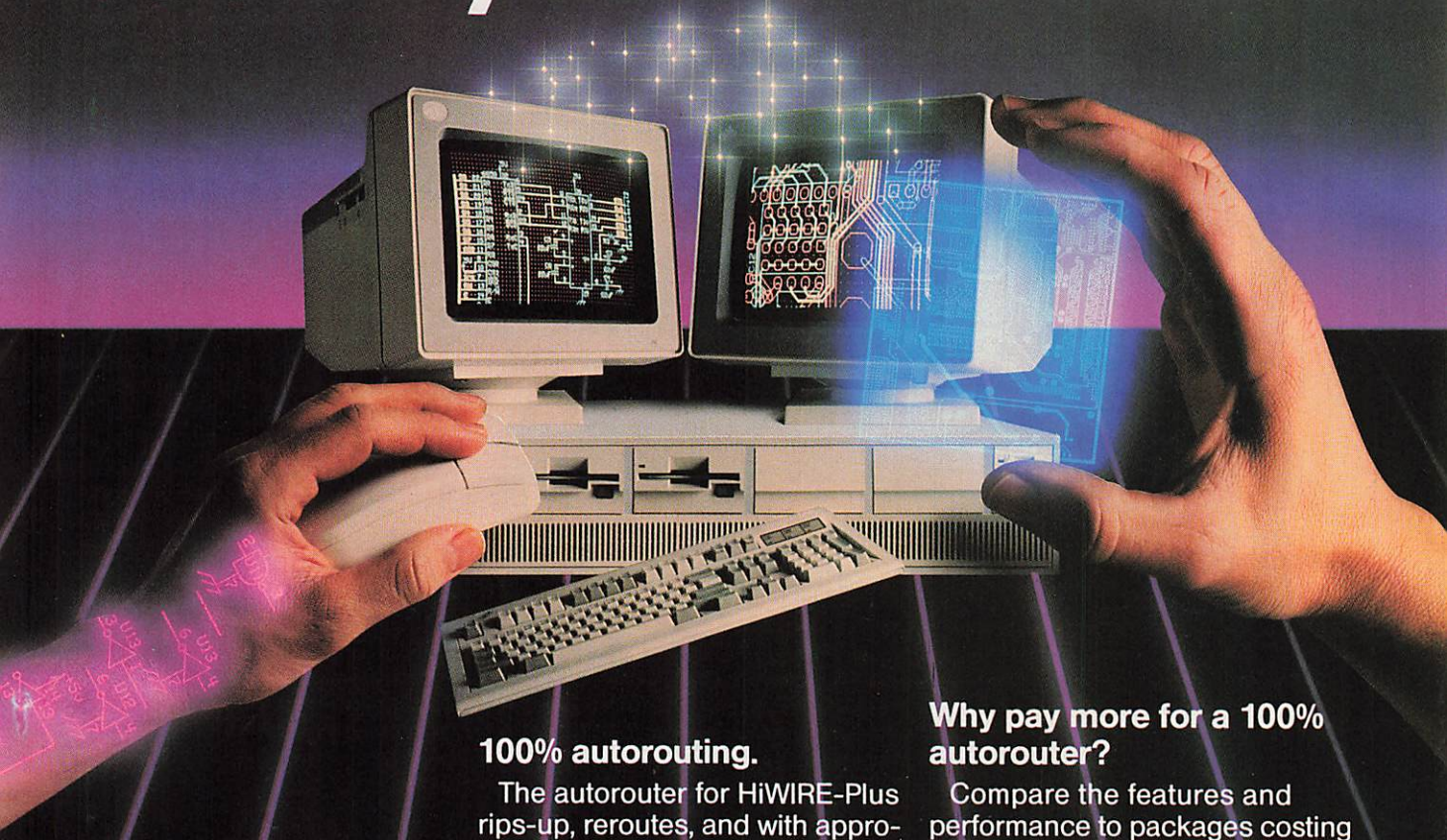
Recent LAN developments include some amazing software from VXM: The software can transform a LAN into a parallel-processing "network supercomputer." The software currently works only on TCP/IP networks, but VXM says the connected configuration can consist of IBM PC compatibles, Macs, Unix workstations, and mainframes.

VXM claims that using its software, a 25-node network of PCs and Macs can deliver the effective processing power of an IBM 3090 mainframe. With 25 RISC workstations, you could have the power of a Cray supercomputer, the company says.

There's lots more—and that's the good news. There is indeed *lots* more. The midyear slowdown is over, and it looks like we're in for some interesting times in the months ahead.

—Fred Langa
Editor in Chief
(BIX name "flanga")

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	Overall Weighted Score	Overall Reliability	Complete of Command Descript.	Overall Perform.	Complete & Organiz. Document.	Document Clarity	Compiling Process Efficiency	Product Support Quality	Value Relative To Cost	Product Support Access.
Turbo C 2.0 (Borland International)	81	87	79	84	77	78	86	72	70	93
C Optimizing Compiler 5.1 (Microsoft Corp.)	76	83	80	81	78	74	76	68	67	70
C++ 1.07 (Zortech Inc.)	66	68	64	71	63	63	69	60	58	76

"Microsoft was No. 1, but they have been unseated by Borland." PC Week, *May 8, 1989*

PC WEEK POLL: SOFTWARE DEBUGGERS

	Overall Weighted Score	Overall Reliability	Effective. Programmer Interface	Document. Clarity	Complete. Command Descript.	Complete. & Organize. Document	Overall Perform.	Integration Within Programming Environment	C Compiler Compatibility	Product Support Quality	Product Support Access	Value Relative To Cost
Turbo Debugger 1.0 (Borland International)	84	89	90	81	81	81	89	88	81	73	72	93
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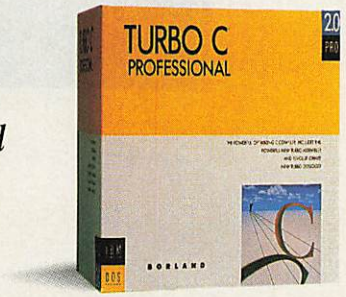
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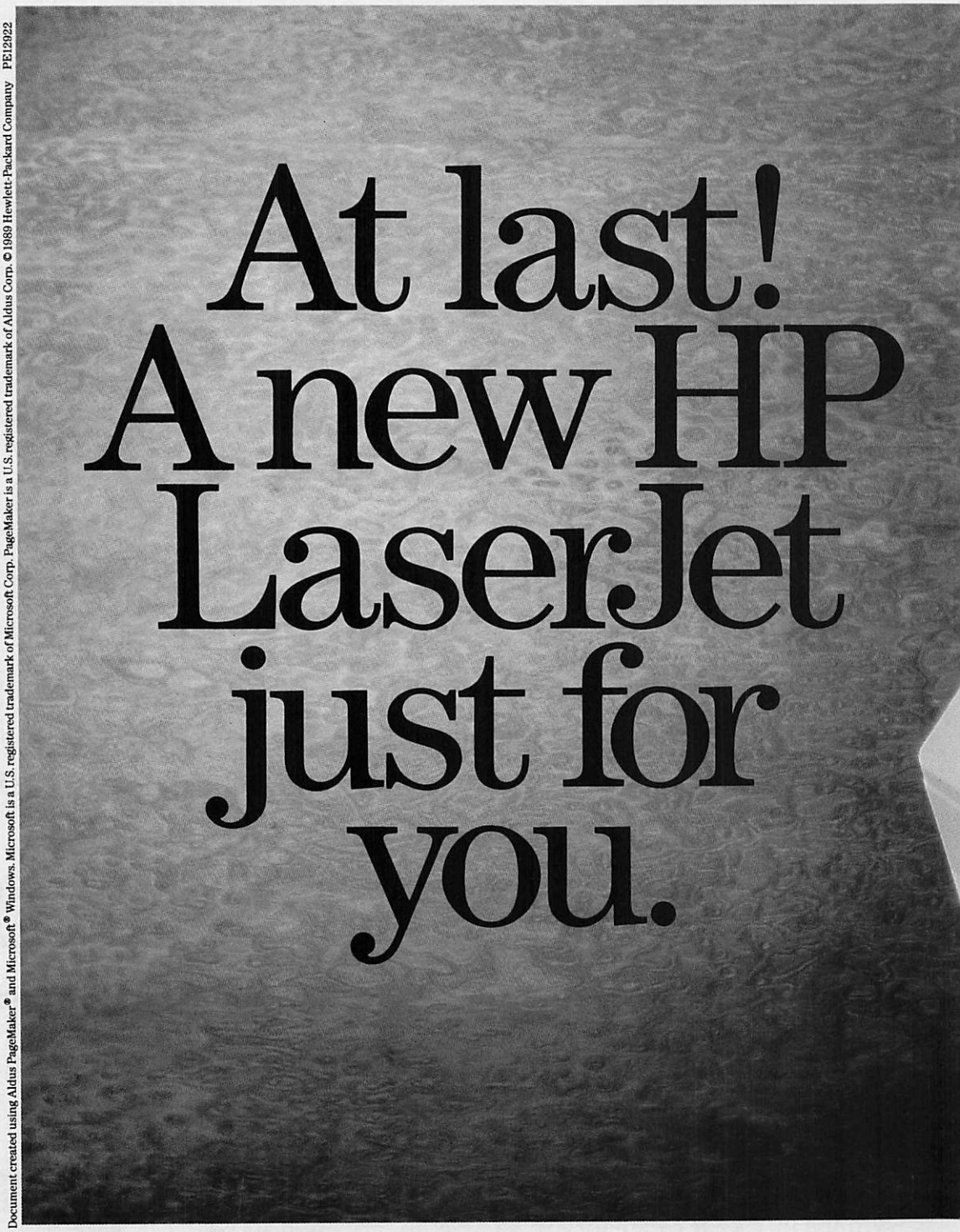


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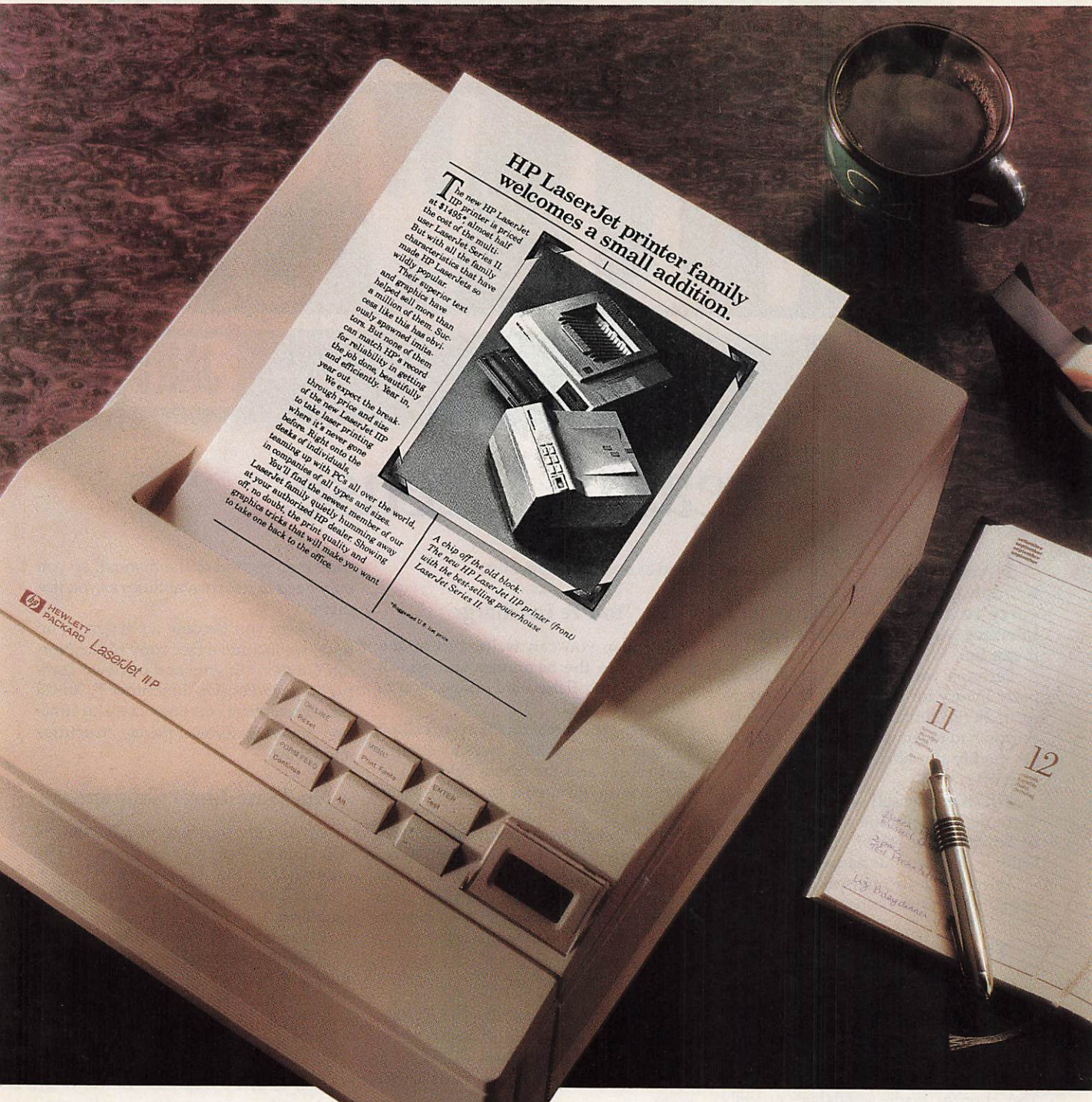
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MICROBYTES

Staff-written highlights of developments in technology and the microcomputer industry, compiled from Microbytes Daily and BYTEWEEK *reports*

Computer Scientists Warn of Physical Limits

Conquering the future frontiers of computing won't be easy, especially with something as big as physics getting in the way. That's the message four researchers delivered to fellow computer scientists at the eleventh World Computer Congress held in San Francisco recently.

Tommaso Toffoli of MIT said that in about 10 years, ICs simply won't be able to get any smaller. Toffoli and Teuvo Kohonen, of the Helsinki University of Technology, both pointed out that the density of microprocessors has been increasing by a factor of 10 every five years. That means that in 10 years, each transistor in a CPU will be one one-hundredth of its current size. But as those transistors get smaller, designers will face the problem of "tunneling" —electrons that won't behave in the expected ways—which means that physical CPU errors would become much more common.

To make computers work accurately beyond that level, Toffoli said, they'll have to depend on the microscopic physics of two electrons rather than the statistical mechanics of millions of electrons. "Maybe in 20 or 40 years we'll have computers where each bit is a quark, and then they will be reliable again," he said.

Kohonen proposed leaving conventional deterministic computers behind in favor of neural networks, using analog systems and a statistical description of data. But, Kohonen admitted, "You wouldn't want to use a neural net to keep your bank account; they're not accurate enough for that."

Gen Matsumoto, of Japan's Electrotechnical Laboratory, offered another alternative: "biocomputing." While neural networks mimic brain activity in computers, biocomputing attempts to electronically duplicate the actual structure of the brain. Matsumoto said that biocomputing work has been going on for five years as part of Japan's "fifth-generation computer project," but at $2 million it's only about 1 percent of the ambitious endeavor's budget.

In an informal poll, Toffoli asked the audience of researchers if they thought that within 10 years it would be possible to hold an extended intelligent conversation with a computer. Almost no one in the audience said yes.

Although digital computers have changed greatly in form over the centuries, said Vladimir Cerny of Comenius University in Czechoslovakia, they haven't changed in function. "We've called it accounting, then calculating, then computing, and now data processing—but the way we do it hasn't changed that much," he said. "Perhaps there is a bigger variety of dynamical systems that can be used for computing." The question isn't whether a machine can compute numbers, Cerny said, but whether it processes information; that's what makes them interesting, he added.

And what happens when machines get much, much better at processing information of all kinds? As Toffoli put it, "Eventually some computers may be interesting enough that they will be able to say, 'Look, leave me alone and let me think about what I want to think about.'"

TI Chips Will Cut Cost of 33-MHz 80386 Systems

Texas Instruments (Dallas) has developed a set of chips that will cut considerably the number of components that it takes to build a 33-MHz 80386-based computer. Most computer makers currently have to design their own discrete logic components to drive the high-speed 80386, and that means from 30 to 60 chips on the system board. But TI's new TACT83000 reduces that chip total down to eight (plus the 80386 CPU). The TACT83000 package is also suitable for 80386SX-based computers, in which case only three "glue-

continued

NANOBYTES

Government and industry are placing too much emphasis on "mission-oriented projects" and not providing enough funding for basic research, renowned computer scientist **Donald Knuth** told the World Computer Congress. The scientific community "faces a crisis," the Stanford University professor said, because scientists can't get funding for projects unless they "**subscribe to somebody else's agenda** telling them what to do. We need a lot of small projects devised by many scientists, instead of concentrating most of our resources on a few huge projects with predefined goals."

Apple Computer (Cupertino, CA) says that it will work with outside developers of "interactive" Mac products to define a framework for accessing information from devices such as VCRs and videodisk and compact disk players. The computer maker says the **Apple Media Control Architecture** specifications will be available to developers by the end of this year. ABC News Interactive, *Newsweek*, Boston's WGBH-TV, Datapro, and the British Broadcasting Corp. have brought out products, on various media, that tap into the Mac's video and audio capabilities.

The U.S. Department of Commerce has revised its list of **computers that can be exported** to Soviet-bloc nations to include most 80286-based laptops. The Department of Defense, concerned that portable computers could have wider military applications, has opposed their export to certain countries. The major laptop manufacturers welcomed the move. "It gives us a level playing field internationally," **Zenith** spokesperson Glenn Nelson told Microbytes Daily. "Naturally, our first step is to evaluate how to pursue these markets. And our next step is to see how we can use the opportunities presented."

NANOBYTES

Send lawyers, guns, and money, but **no computers**: With the recent lifting of restrictions on computer exports to some countries, the **prohibited list** has gotten shorter. According to rules published in the Federal Register, American computer makers cannot legally send computers to Cuba, Cambodia, North Korea, Vietnam, Libya, South Africa, or Namibia.

Seiko Instruments (San Jose, CA) now has a Macintosh model of its **color thermal printer**. The new QD5500 printer incorporates a QuickDraw device driver that supports a set of 35 scalable outline fonts, similar in concept to the fonts that Apple says it will supply with System 7.0 next year. (Seiko will support Apple's outline fonts when they become available, a Seiko official said.) Resolution is 300 dpi. Seiko claims the unit has a print speed of 1 page per minute. Depending on page size and memory capacity, the printers range in price from $7000 to $14,000. The Seiko printer costs about $2000 less than comparable color thermal units from Tektronix and QMS, but it doesn't have its own processor and doesn't support PostScript.

Hewlett-Packard (Palo Alto, CA) and **Samsung** (Seoul, Korea) plan to jointly develop **low-priced workstations** based on HP's Precision Architecture. The RISC-based Unix systems will start at about $5000, an HP official said. The deal calls for Samsung to manufacture the products that result from the shared development work, which will then be sold by HP on an OEM basis. HP and Samsung say they'll have their first codeveloped workstations by 1992.

Intel (Santa Clara, CA) is sampling its 32-bit LAN coprocessor chips for file servers, multiuser systems, and workstations. The 82596 uses the same bus interface signals as the 80386 and 80486 processors; it off-loads the host CPU and transmits data at the 32-bit bandwidth of the system bus. The chips are designed for being built right into the system board.

logic chips" are required.

The new four-chip set requires only four additional off-the-shelf glue-logic chips to form a complete 80386 system. The TACT83000 package will make it possible to build a complete 33-MHz 80386 system on a 4- by 5-inch board, according to TI product manager Gerald Wineinger. The chip set will also allow manufacturers to reduce their design and production costs, Wineinger says.

The chip set consists of the memory control unit (MCU), the data path unit (DPU), and the AT bus interface unit (ATU), a single 208-pin chip that drives the standard AT bus. The ATU is "truly asynchronous," Wineinger said, requiring no wait states or slower clock frequencies. The DPU is a "cascadable" 16-bit unit, allowing multiple DPUs to be configured to form wider data paths. The 32-bit 80386 implementation requires four chips rather than three because two 16-bit DPUs are needed. Since the ATU is a separate chip, TI says that it will be easy to offer "sibling" chip sets that support the new Extended Industry Standard Architecture (EISA) and the Micro Channel architecture bus interfaces. TI is also working on a version that will support the "burst-mode" 64-bit data transfer capability of Intel's 80486 chip.

TI will be competing with Chips & Technologies and Headland Technology, which have 33-MHz 80386 chip sets under development. But TI marketing manager Stephen Tang-Kong says that TI will be the first to deliver. "We're already working with beta boards and will have customers demonstrating systems at Fall Comdex," he says. Tang-Kong claims that the competitors' offerings will require from 9 (Headland) to 30 (C&T) additional logic chips for a complete system.

TI hopes to woo the "HPs, NCRs, and Olivettis of the world" with this new chip set, Tang-Kong says. He claims the chip set could cut prices of 33-MHz 80386 systems in half.

Cypress Claims 40-MHz Chip Fastest SPARC Yet

Cypress Semiconductor (San Jose, CA) has developed what it claims is the fastest RISC processor based on Sun Microsystems' SPARC design. The chip maker says that its new 40-MHz 7C601 RISC chip is capable of performing 29 MIPS.

The new CMOS chip is 20 percent faster than the 24-MIPS version Cypress introduced earlier this year, according to Steve Goldstein, director of marketing of Cypress's Ross Technology subsidiary. Increased performance is a "result of enhancements in clock frequency," he said.

The 7C601 incorporates a large windowed register file (136 general-purpose 32-bit registers), which reduces the number of load and store operations and frees up bus bandwidth, Goldstein said.

In 100-piece quantities, the 7C601 costs $895.

Cypress sees bright days ahead for the SPARC chip, which Sun is trying to establish as the standard architecture for RISC workstations. According to Goldstein, SPARC will eventually be the top RISC choice because of the relatively large number of software applications already running on SPARC-based workstations. Goldstein predicted that the number will climb to 1000 by the end of this year.

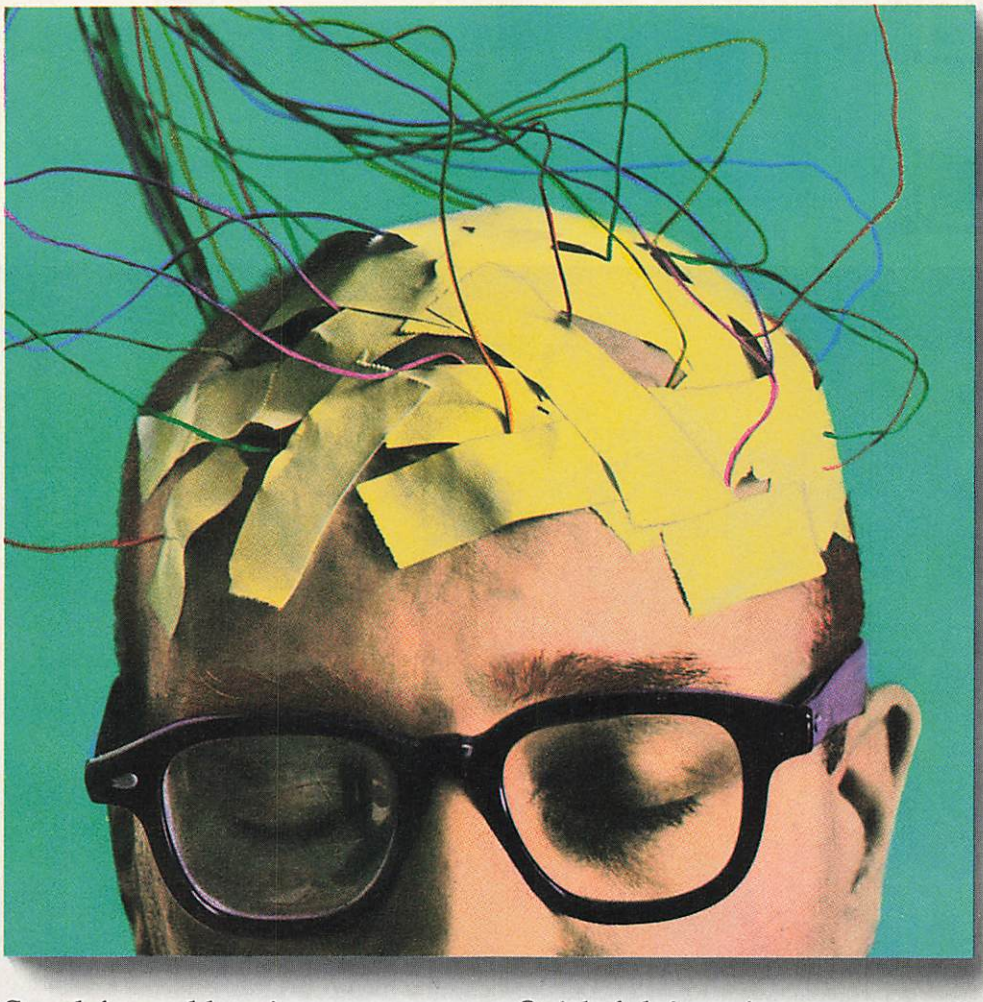
After ISDN, We Can Wait for IBCN

Although ISDN has barely penetrated the communications structure, work is under way to develop the next step beyond: a more functional system called Integrated Broadband Communication Network.

ISDN runs on standard telephone cable at 9600 bps, while IBCN would run on broadband cable at up to 150 million bps by 1995 or so, says P. J. Kuehn of the Institute for Communications Switching and Data Techniques in West Germany. That speed will reach 600 million bps sometime after the year 2000, Kuehn predicts. With the greater bandwidth, users could see such functions as TV and radio programs, videoconferencing, voice or video mail, and interactive videotex delivered to their house, Kuehn says.

continued

Until now there was only one way to integrate C and Assembler.



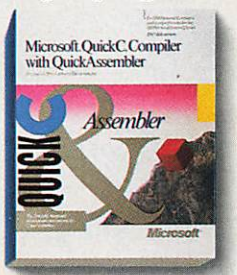
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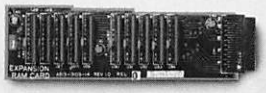
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Neuron Data Systems (Palo Alto, CA) has developed a **HyperCard front end** for its Nexpert Object program, allowing the "expert" to input the rules and objects of the expert system as a series of HyperCard stacks. The company also has announced a **Presentation Manager front end.** Neuron Data has designed a "client/server architecture" for Nexpert Object that will allow PCs and workstations to access knowledge bases residing on a server or host mainframe. According to company official Patrick Perez, a key element in LAN-based expert systems is the use of "shareable image technology," in which a snapshot of the centralized database and knowledge system is processed locally on the network station or PC.

Tumbling price: **Dell Computer** cut the price of its 80386SX system by $430 to $2839. **Sanyo** lowered its 8088-based 16EX computer to $905 and its 80286-based 17Plus5E to $1689. **Boca Research** eased the pain of memory by dropping its 8-megabyte BocaRAM/AT Plus memory board down to $2195, from $3395; the 4-megabyte board is now $1195 instead of $1795; the 2-megabyte model is now $695, $300 less than before. **Orchid Technology** also lowered memory board prices; its 2-megabyte RamQuest Extra 16/32 dwindled from $1499 to $1179. **Applied Engineering** cut 26 percent off the price of its MS-DOS coprocessor board for the Apple II series; the PC Transporter is now $499.

Microtec Research (Santa Clara, CA) said at UniForum in Boston that it will come out with a C compiler and other **programming tools** supporting the Motorola **88000** RISC processor. The tools will run on Sun-3, VAX/VMS, and IBM PC–compatible hardware.

AT&T is going to start letting colleges produce and distribute binary copies of AT&T's **C++ Language System** 2.0 to **students** for $25 each. A license for C++ source code will cost $300 per CPU. For more information, dial (800) 828-8649.

Although critics of ISDN charge that it's already outdated in terms of data capacity, even IBCN won't be able to support such high-volume data generators as high-definition TV, Kuehn says. HDTV already requires a capacity of more than 150 million bps.

During this migration from ISDN to IBCN, different countries will stress certain communications functions above others, says H. Ikeda, of Nippon Telephone & Telegraph in Japan. The U.S., for example, is likely to stress data transmission capabilities over voice or video transmission, Ikeda says. Consequently, evolution scenarios will differ from country to country, but vendors and standards bodies have to make sure that the underlying architecture works with all of them, Ikeda notes.

So what about ISDN? Although ISDN has been used little so far, that's going to change, says R. G. F. Aitchison, of ICL Network Systems. While ISDN lines cost 1.3 to 1.7 times the price of standard telephone lines, that's a "trivial element" compared to the technologies ISDN can provide, Aitchison says.

Computers Get Good Grades in This Study

Maybe it depends on whom you ask. Researchers and teachers attending the National Educational Computing Conference this summer indicated uncertainty about the usefulness of computers in the classroom (see October Microbytes, page 17). But in a study released more recently, most of the teachers questioned gave computers good grades. Two-thirds of the teachers in the U.S. say that use of computers in school should be drastically increased, according to a study published by IBM and conducted by The Wirthlin Group. Titled "Computer Report Card: How Teachers Grade Computers in the Classroom," it's "the most extensive study ever done of teachers' attitudes about computers in the classroom," IBM says.

Here are some of the results from the study: 82 percent of teachers polled said that the use of computer-based writing and reading programs could improve the illiteracy problem; 85 percent said that computers have already had a positive effect on the quality of education; 82 percent said that computers improve student motivation; 74 percent said that students who are not "computer literate" won't be adequately prepared for college; 60 percent of the teachers said that they feel inadequately trained in computer use, and 52 percent said that their students are more computer-literate than they are; 88 percent said that some sort of government funding should exist to expand the use of computers in the classroom, while 70 percent said that the greatest roadblock to more effective use of computers in schools is limited finances.

James Dezell, IBM's vice president of Educational Systems, said that by the time the average student graduates from high school, he or she has spent 20,000 hours in front of the TV and only 12,000 hours in the classroom. He claims that computers give teachers the resources to compete for students' attention "and win."

The nationwide telephone survey of 1100 teachers was conducted in July. All 1100 respondents in the survey were full-time teachers of grades between kindergarten and high school; 66 percent said they currently use computers for instruction.

Quarterdeck Eases RAM Cram with QRAM

Quarterdeck (Santa Monica, CA) has developed a new PC utility designed to squeeze more memory out of DOS computers. QRAM (Quarterdeck pronounces it "cram") is a $59.95 utility for XT and AT compatibles with expanded memory conforming to the EMS 4.0 or EEMS specifications. QRAM can locate unused space in "high memory" —the area above DOS's 640K-byte limit, but below the 1-megabyte limit of the 8088 microprocessor—and lets you load device drivers and TSR programs there.

The idea is to ease "RAM cram." Ordinarily, drivers and TSR programs take up part of the 640K bytes of memory that's available to DOS

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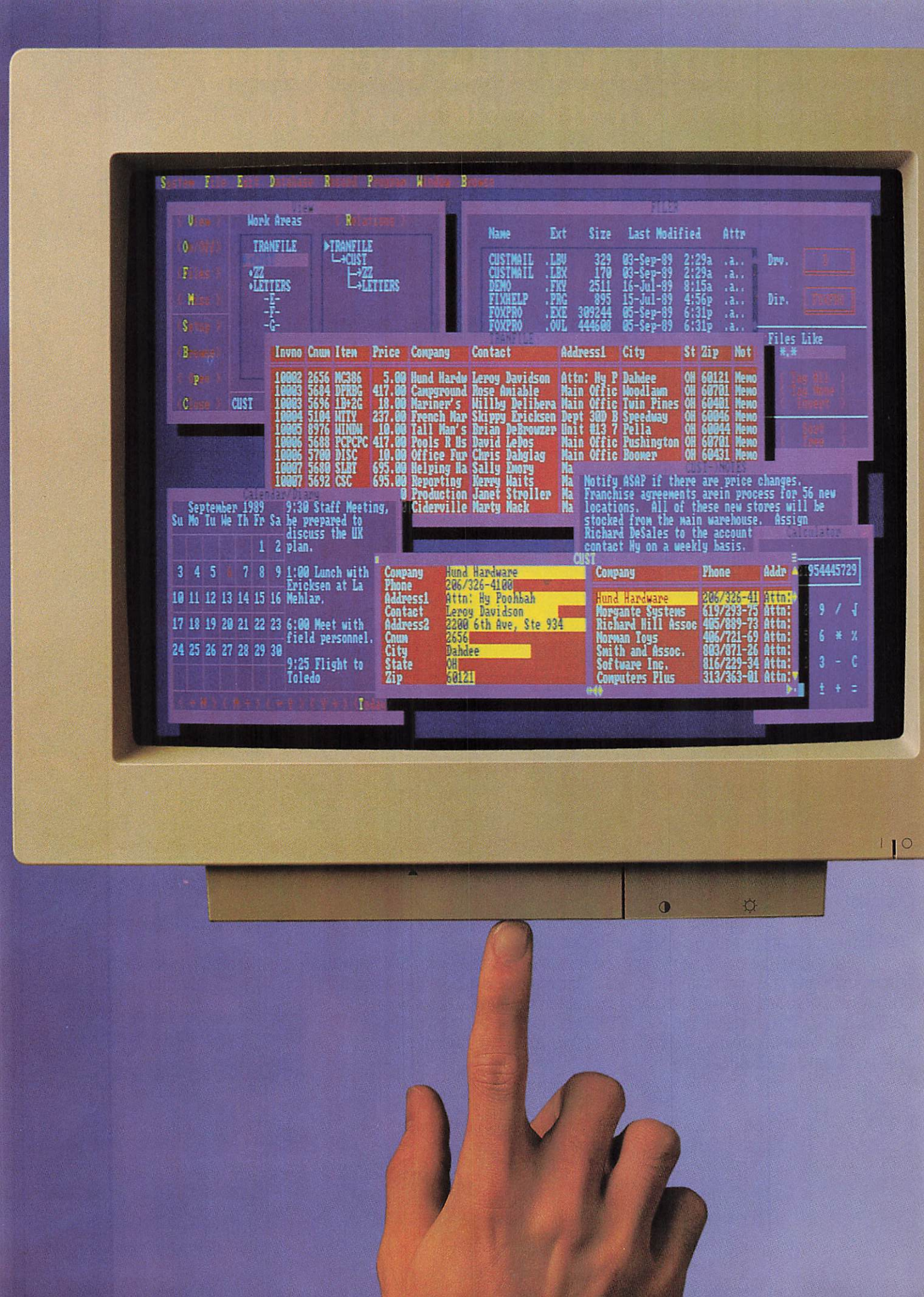
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Work Areas
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Name Ext Size Last Modified Attr
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CUSTMAIL .LBX 170 03-Sep-89 2:29a .a..
DEMO .FKY 2511 16-Jul-89 8:15a .a..
FIXHELP .PRG 895 15-Jul-89 4:56p .a..
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10003 5696 1B+2G 18.00 Mariner's Willby Delibera Main Offic Twin Pines OH 60401 Memo
10004 5104 WTTV 237.00 French Mar Skippy Ericksen Dept 30D B Speedway OH 60046 Memo
10005 8976 WINDW 10.00 Tall Man's Brian DeBrowzer Unit #13 7 Pella OH 60044 Memo
10006 5688 PCPCPC 417.00 Pools R Us David LeDos Main Offic Pushington OH 60701 Memo
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10007 5692 CSC 695.00 Reporting Kerry Waits Ma
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1:00 Lunch with Ericksen at La Mehlar.
6:00 Meet with field personnel.
9:25 Flight to Toledo
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Contact Leroy Davidson
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State OH
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Company Phone Addr
Hund Hardware 206/326-41 Attn:
Morgante Systems 619/293-75 Attn:
Richard Hill Assoc 405/889-73 Attn:
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Tandy (Fort Worth, TX) expected to start selling this month a new **portable word processor** that's based on a 5.5-MHz Z80 chip, weighs 3.1 pounds, and is priced at $350. The new WP-2 is physically reminiscent of the Tandy Model 100/102 but has a bigger screen (an 80-character by 8-line LCD) and a 62-key QWERTY keyboard. Built into the computer is a word processing program (more sophisticated than the simple text editor in the Model 100, Tandy says), a 100,000-word spelling checker, and a 200,000-word thesaurus. Using the two function keys in combination with number keys, you can cut, copy, and paste; search and replace; center and justify text; send output to a printer; and initiate telecommunications. The diminutive unit has 32K bytes of memory, of which 22K bytes can hold documents. The WP-2 is powered by four AA batteries; Tandy estimates the operating battery life to be 12 hours. A lithium battery backs up the RAM.

While most of the specialized software used to gather and analyze the data from the **Voyager** spacecraft during its recent Neptune encounter was custom-written, scientists at the **Jet Propulsion Laboratory** (Pasadena, CA) used several off-the-shelf applications to make their work easier. With a Unix package called **DataViews** from **V. I. Corp**. (Amherst, MA), running on a Sun-3/260 workstation, they were able to graphically display live data on solar wind, atmospheric conditions, and various energy parameters. DataViews is a set of graphical interface application and development tools; the JPL scientists used it to create images for internal use and for the TV networks of nongraphic data using flow patterns, histograms, and spectrograms. They were "essentially doing two-dimensional representations of three-dimensional data in real time," JPL programming manager Pat Liggett told Microbytes Daily. The billions and billions of bits of data coming from the spacecraft were stored using a standard SyBase relational database manager.

programs. Unfortunately, that leaves less and less space for applications. Quarterdeck says that QRAM adds "load-high" capability on top of EMS or EEMS drivers.

But one of the most interesting parts of QRAM isn't the memory manager itself. It's a utility called Manifest, which Quarterdeck is bundling with QRAM and QEMM. Quarterdeck systems architect Dan Spear says Manifest "tells you everything it's possible for software to find out about your hardware." The menu-driven program compiles configuration information, monitors memory usage, and generally provides every facility you're likely to ask for in tracking down hardware and software problems, particularly when you're trying to spot conflicts between programs.

Manifest is a critical part of the QRAM package, Spear says, because with the endless variety of PC clone configurations, it's almost impossible to be sure a TSR program or driver loaded into high memory won't conflict with a video board or other pseudomemory outside the range of standard RAM. For example, video cards that automatically switch between CGA, EGA, and VGA might collide with a driver that QRAM thinks is loaded into unused video memory. Manifest lets you monitor memory use and spot the collision. It also allows mundane explorations, such as checking the CONFIG.SYS and AUTOEXEC.BAT files.

Much of what Manifest does isn't new. Many of the capabilities have been available in bits and pieces for years, in public domain and shareware utilities. Spear says he duplicated every diagnostic utility he could find and then added every remaining tool he could think of.

Speech More Important Interface Than Graphics, Media Lab's Negroponte Tells SIGGRAPH

Nicholas Negroponte, director of MIT's Media Lab, came to the year's biggest computer graphics show and pronounced that the most significant development in the human/computer interface during the next five years will be in speech technology and not in computer graphics. In his keynote address at SIGGRAPH '89, Negroponte said that in the future, "the primary means of communication with computers will be through speech, not through graphics."

Part of the reason that speech-recognition capabilities have not advanced to the point where people can converse with their computers is that "people in the speech-recognition industry are fundamentally not interested in communication," Negroponte said. Because so many people involved in computer research are "not interested in communication," the computer remains "sensory deprived," he said.

Negroponte urged the SIGGRAPH audience, which consisted of researchers, scientists, engineers, designers, and artists at the forefront of computer graphics, to be more concerned with "how people communicate with computers instead of drawing teapots." ("Teapots" was a reference to the half-solid/half-wire-frame kettle in the SIGGRAPH logo, which had been shown rendered with various surfaces in a presentation preceding Negroponte's talk.)

Another development in what Negroponte calls "the sensory apparatus of computing" will be vision capabilities that will enable the computer to receive and interpret visual clues from the user. Right now, if we take our hands off the keyboard, the computer doesn't know if we're just pausing or leaving for the weekend, he said.

Although the desktop metaphor is dominant in the human/computer interface today— "Some people even have the temerity to go to court over it," Negroponte said—that's going to change because the desktop metaphor doesn't work. "Any quantity of data and it starts to fall apart," he said. Negroponte described a day when the interface will simulate efficient procedures that people are already familiar with. Finding a stored document, for example, won't involve "mousing around," he said; it will be similar to what he does now: He calls his secretary through the speakerphone and asks her to please bring in a copy of the needed document. But instead of asking his secretary to find the document, he'll use his voice to ask his computer.

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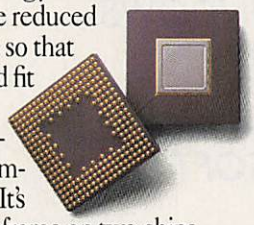
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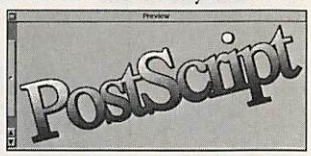
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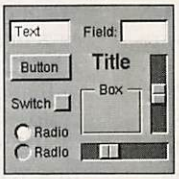
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NANOBYTES

Meanwhile, as Voyager brushed past Neptune, earthlings were able to see images of the distant planet and its moons on IBM PS/2s at several museums around the U.S. The computers were running DOS-based image management software called **PicturePower**, from **PictureWare** (Bala Cynwyd, PA). The software stores and indexes images and lets the user annotate and manipulate them. Images can be imported in several formats and tied to textual dBASE records. The latest version of PicturePower sells for $1995. An optional image compression board, which uses the TI DSP 320C10, is $2000.

Although **Logitech** (Fremont, CA) thinks its **TrackMan** "stationary mouse" will be popular, "it will not replace the mouse" as the standard pointing device, company president Pierluigi Zappacosta said. So what will? **Doug Engelbart**, who invented the mouse in 1962, was at Logitech's briefing when it rolled out the new trackball-equipped TrackMan; he said he is a "great believer in evolution. Eventually the mouse will probably pass, and something else will replace it."

The **operating environment that dominates** desktop computing in the next decade will have to be able to handle four things, **Quarterdeck** president **Terry Myers** says: "communications, graphics, video, and voice." Those in the running right now, Myers said in an interview, are DOS, Digital Research's DR DOS, Microsoft Windows, OS/2, and Unix.

Apple's new $1.5 million corporate TV studio occupies the building where the **Macintosh design team** once roosted. In those days, they flew a pirate flag from the roof. The remodeled building now houses Apple TV, which will produce in-house training programs and videos for employee inspiration. Apple is currently installing a fiber-optic network throughout its buildings; combined with real-time video cards, such as the new Micro TV from Nolan Bushnell's Aapps, every Mac at Apple could be an Apple TV set.

Vortex Controller Takes Different Approach to Reconstructing Disks After Disaster

Vortex Systems (Pittsburgh) has designed a new disk drive controller card that could significantly affect disk backup systems. Vortex says that its new RetroChron controller will continuously back up data and will allow system administrators to restore a disk to the exact state it was in at any previous time. Although the first version of the board will be expensive—about $5000 in single-unit quantities—the RetroChron could be useful on large network file servers, and its technology will surely migrate to less expensive controllers.

The RetroChron is essentially an enhanced SCSI disk drive controller for AT-compatible systems. The board has a small cache and can control three SCSI drives, which can appear to system software as one giant "perfect" virtual drive. It differs from other disk drive controllers in that it keeps a time-stamped record of every sector of this virtual drive, and it records every new version of the sector that the system writes to the drive.

With this information, the RetroChron can reconstruct a state of the virtual drive at any previous time by returning the version of each sector that was current at that time. As in the case of a disk-mirroring system, backup is continuous. And, like a tape cartridge system, the Vortex approach maintains a chronological record of the state of the disk. Every time a new version of a sector is written, it must be written twice—once on the primary drive and once on the backup drive.

Vortex officials claim that, in most cases, the disk-caching memory of the RetroChron board offsets this overhead and that users won't notice any drops in speed. However, during massive disk writes (e.g., copying a whole directory), speed degradation will be noticeable. The company says that it is planning a future model that will improve disk performance by replacing the card's 80186 processor with an 80386 and 4 megabytes of disk-cache memory.

In addition to a backup disk drive, the RetroChron board requires its own 40-megabyte disk drive for queuing disk writes, and a terminal or a PC running terminal-emulation software, by which the system adminstrator controls the controller.

Mac's a Part of the Puzzle, AT&T Unix Exec Says

Picture vast and glorious networks of multibrand computers, desktop systems and engineering workstations and giant file servers, DOS machines here, OS/2 and Unix machines there, swapping documents and programs, sharing resources and data in an open and harmonious environment. Does this computing pastoral look familiar?

But there's something wrong with this picture of interoperability, according to AT&T's executive in charge of Unix: There's no Macintosh in it.

Unix vendors have to become more concerned with the Macintosh, AT&T's Larry Dooling told an audience at UniForum in Boston. "How come nobody's worried about the Mac interface?" asked Dooling, president of AT&T's Unix Software Operation. "I'm worried about it," he said. Although computer users are currently concerned with interoperability between Unix systems and IBM-compatible systems, they will soon start demanding that these connected environments include the Mac. It's "the most important user interface today on the desktop," Dooling told his audience of Unix users and developers. "I think we've got users out there who are going to demand that we address interoperability with those systems as well."

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LETTERS

and Ask BYTE

Package Deal

I read Don Crabb's "Smalltalk Can Be Cheap" (April) with great interest, and I'm looking forward to the appearance of the course next year. Of course, not having the product is something of a deterrent. Consequently, I suggest that Crabb put together a good book or reference material to be sold with Smalltalk/V for either the Mac or an IBM PC or clone. The possibility of the 80286 should also be kept in mind. In this way, many versions of Smalltalk could be sold, and we'd be able to follow more closely what is being presented in the course. Making object-oriented programming available would be a great service.

C. Metelmann
Hellerup, Denmark

Ultimate or Penultimate System?

I just finished reading "The Ultimate Upgrade" by Stanford Diehl (June). As an avid (sometimes rabid) hobbyist, I was very surprised at the upgrade approach that Diehl took—and even more by the total cost.

In May, I completed the upgrade of an old XT clone to a mighty 80386-based machine. My goal was speed with lots of capacity and room to grow. Here's what I got for less than half what you paid. Aside from the Ethernet abilities of your machine, there's not a lot of difference in what yours and mine will do.

I started with an XT form-size 80386 motherboard by Hauppauge Computer Works. This board has a 20-MHz 80386 processor and 1 megabyte of RAM, a Phoenix BIOS, a coprocessor slot, an internal clock, and all the other normal goodies. It cost me $1895. In the 32-bit slot, I added a card for up to 8 megabytes of memory and loaded it with 4 megabytes of 80-nanosecond RAM for $1080.

For storage, I settled on the Seagate 4096 hard disk drive with 80 megabytes of storage and a 28-millisecond access time for $549; I chose it mainly due to price and my knowledge of the product. I replaced the standard 5¼-inch floppy disk drive with a TEAC 360K-byte 5¼-inch dual floppy disk drive for $110. To make backups easier, I added an Everex 40 AT 40-megabyte tape streamer for $349.

For a controller to run the floppy disk drive, hard disk drive, and streamer, I chose the Western Digital WDL1006V-MM2 (it controls two hard disk drives and two floppy disk drives with an 89K-byte look-ahead cache, has a 1-to-1 interleave, and is 16-bit) for $255.

Most of my work is text-related, so I wanted a graphics adapter and monitor that would not give me eyestrain. I selected the combination of a 14-inch color Taxan 770 Plus Monitor (multisync) and an ATI EGA Wonder adapter. These give me all the colors I need in WordPerfect, Lotus 1-2-3, and Harvard Graphics, as well as 132 columns in Lotus 1-2-3. I paid $248 for the card and $930 for the monitor.

I dropped in an I/O card with two parallel ports and two serial ports ($28) to take my printer and mouse and leave me some spares. For long-distance communication, I added the ATI 2400 modem for $152.

Just to make sure that there wouldn't be any problems in the power department, I replaced the XT power supply (175 watts) with a 220-W model for $46. As a last present to myself, I added a 20-MHz 80387 coprocessor for $395.

The only remaining piece of the XT is the flip-top case. Everything else is different.

Total price: $6037 plus 2½ hours for assembly and setup.

For the hobbyist willing to take the

continued

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time to investigate the equipment on the market and match it to his or her needs, it is possible to build a machine as good as or better than a brand-name machine.

Mark E. Hazlewood
Middes, Switzerland

OS/2 on the Cheap

In his article entitled "OS/2 for Cheap" (April), Mark Minasi went to great lengths building an "inexpensive workstation that supports Presentation Manager," yet his total price for a 10-MHz 80286 machine was $3444. Cut me a break!

First of all, why would anyone buy a slow 80286 when he or she could buy a 20-MHz 80386 for less money than Minasi spent? I would suggest that he carefully read Steve Apiki and Stanford Diehl's article "80386s for the Masses" (October 1988).

Second, Minasi spent $300 extra on an 80-megabyte hard disk drive (the approximate price difference between a 40-megabyte and an 80-megabyte hard disk drive) when a 40-megabyte drive would have done just fine.

Third, everyone knows that PM and all the application software being written for it will be graphics-based, yet Minasi chose to save money by buying a monochrome monitor.

I suggest that Minasi forget the 80-megabyte hard disk drive and buy a VGA monitor, recheck the mail-order prices for 20-MHz 80386 machines, and read his copies of BYTE more carefully.

William Vantine
Arlington, VA

You seem to be saying three things: Buy an 80386, because it will be cheaper than the 80286 that I recommended; buy a VGA graphics system; and don't buy an 80-megabyte drive—buy a 40-megabyte drive and save $300. I'll cover these points one at a time.

First, I said that a 4-megabyte 80286 system with a hard disk drive controller, keyboard, and 1.2-megabyte floppy disk drive would cost about $2390. Sure, you can find 20-MHz 80386s for about $2000, but you've got to add 3 megabytes more of RAM at that point, which cost about $1600 in December 1988, when I wrote the first column. In "Electing the PM" (February), I said, "To simply boot the PM with the compatibility box requires 2.6 megabytes, and you're best with a minimum of 4 megabytes." Refer to point 3 in your letter.

Second, you seem to be confusing the notion of a monitor type with a graphics board type, which is a common and quite understandable confusion. You see, merely having a monochrome monitor does not imply that you do or do not have graphics capabilities: It is the video board that determines what level of graphics you can support. As I said in my column, the Paradise Monochrome EGA card, as you would expect, supports full EGA graphics on a monochrome monitor. You get the full functionality of an EGA card and monitor—the only difference is that you see shades of gray rather than colors. Sure, VGA monitors are nice, but they're also pricey. The Paradise board and a monochrome monitor can be found discounted for about $270. For a little more money, my fellow columnist L. Brett Glass speaks highly of the MultiSync GS, a monochrome multiscanning monitor that can display VGA as shades of gray.

Third, how large a hard disk drive to buy is a matter of personal preference.

continued

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The reason that I recommended 80-megabyte drives is that they seem, at the moment, to be an excellent buy in terms of bucks per megabyte. For example, the advertisement on page 358 of the June BYTE for Mead Computer shows that a Seagate 4096 80-megabyte drive sells for $649. And Mead sells its 40-megabyte 4053 for $519. Paying $180 for 40 megabytes is a deal that I just can't refuse. And the Seagate 4096 can be had for even less—the one in the machine that I'm now working with cost me $550.

Remember, hard disk space is like all the good things in life—you just can't get enough of it.—Mark Minasi

Nectar in a Sieve

Nick Pelling's letter describing a more efficient algorithm for the Sieve of Eratosthenes ("Algorithm Optimizing," May) fired my imagination, with startling results.

In the Sieve, all multiples of numbers greater than 1 are cleared in an array of flags. The remaining flags are prime numbers.

Pelling made the following points: In choosing numbers whose multiples to test, only prime numbers need to be used; each prime number used can begin the search at its own square; and the highest prime to use in this way is the square root of the size of the array.

This was the fastest prime-number algorithm I'd ever seen, and I got excited. After a while, this led to an inspiration: While each prime is testing its way through the array, every second test is against an even number. If these are eliminated, the speed of the algorithm doubles.

Pelling's BASIC program was similar to this (I've added line numbers for reference):

```
1  max=8192 : root=INT
   (SQR(max)) : DIM flags(max)
2
3  FOR num=1 to max
4     flags(num)=TRUE
5  NEXT num
6  FOR num=2 TO root
7     IF flags(num) THEN
8        FOR mult=num*num TO max
               STEP num
9           flags(mult)=FALSE
10       NEXT mult
11    END IF
12 NEXT num
```

I changed three of the lines:

```
2  flags(2)=TRUE
3  FOR num=1 to max STEP 2
8        FOR mult=num*num TO max
               STEP num+num
```

The altered program runs twice as fast as the original.

A second idea is to compress the array. The new algorithm never uses the even-numbered flags, so they don't have to be there. By having the flag array represent successive odd numbers, twice as many primes can be found in the same amount of memory.

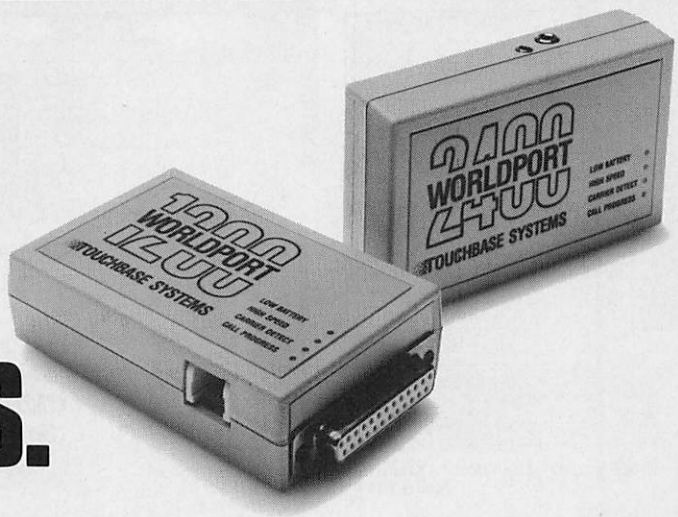
Milton Pope
Bakersfield, CA

Patents Aren't Panaceas

I have seen enough of these shortsighted pieces extolling the virtues of patents ("Quarterdeck Patents Multitasking Technique," BYTE *Special News Supplement*, July).

continued

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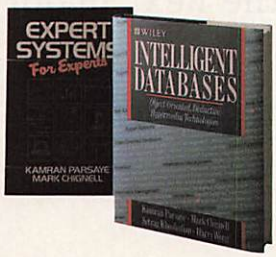
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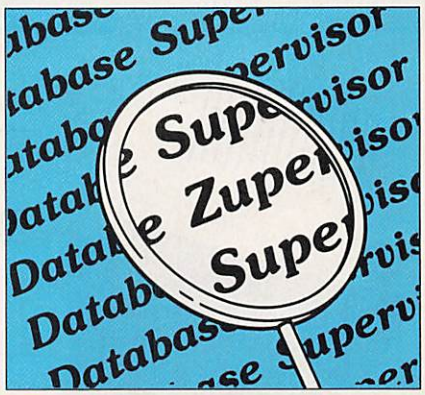
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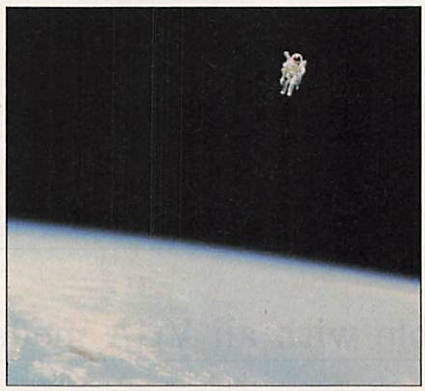
The Intelligence/Compiler is a powerful state of the art system for real-world applications. Its intelligent editing and debugging facilities are a bonus. *AI/Expert Magazine*, February 1988.

Considering the variety of features that the Intelligence/Compiler provides, it is hard to believe that you can get better value for your money. *PC/AI Magazine*, June 1989.

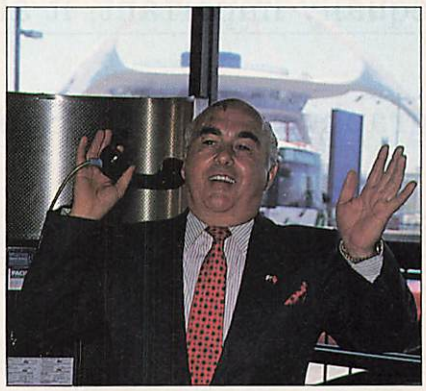
Having used IXL on a large database of geological test data, we were surprised by the many relationships it found. This has greatly helped us to interpret our Oil Company database. *Mr. James Brown*, Oil Industry Consultant, July 1989.



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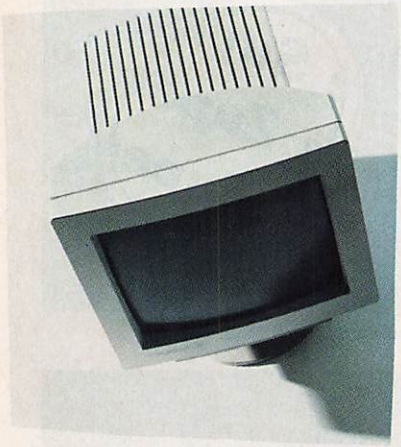
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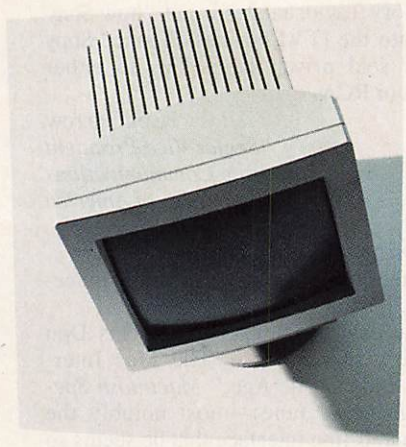
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Digitron Telecommunications is a small computer engineering company specializing in audiotex and automated telemarketing systems. Since it is our innovative technology that sets us apart from our much larger and well-established competition, we viewed patents as a logical way to protect our innovative technologies. After consulting with patent attorneys, we soon found that the picture wasn't nearly so rosy as the article would have us believe.

Obtaining a patent for a piece of software typically costs between $3000 and $10,000. This is more expensive than patents for mechanical devices because of the flow charts and other software-specific documentation required. Most companies, even small ones like ours, can afford this price. However, once you have obtained the patent, you are not out of the woods yet. If one of your competitors challenges your patent, the costs of defending it can easily run into several hundreds of thousands of dollars. If one of the megacompanies (e.g., IBM, Computer Associates, or Microsoft) comes after a little software company, it can bury the small company in the legal costs of defending the patent.

Also keep in mind that by patenting a technology, you release your trade secrets, so that everyone has access to the details of your work.

In the end, we decided not to patent our software, since we don't want to give it away for free and we couldn't afford several hundred thousand dollars in legal fees to defend our patents.

Like so many things in our litigious society, the patent process defends the mighty at the expense of the weak. The eventual outcome of widespread software patents will be to kill innovative small companies and to ensure a software monopoly for the few megacompanies who can outspend everyone else in court.

Steven Marc Abrams
Westbury, NY

Praising the Pioneers

I enjoyed Rick Grehan's "Directory Assistance" (Parts 1 and 2, May and June) but lamented his omission of the pioneer TRS-DOS and LS-DOS systems on the TRS-80s. While these veteran operating systems may not hold the market share they once did, they provide many useful and sophisticated features that their more popular contemporaries sorely lack.

For instance, file specifications are hashed to an 8-bit value and indexed in a table occupying one directory sector. Once it has located the information, the disk operating system goes directly to the directory entry and wastes no time wading through all the other directory entries. Thus, the TRS-80 has faster file access than many of its 16-bit rivals.

Directory sectors use a unique data address mark so that the system can distinguish them from data sectors, making it nearly impossible for an application inadvertently to destroy the directory.

The flexibility that TRS-DOS and LS-DOS afford is also noteworthy. Though it predates 3½-inch floppy disks, it automatically recognizes them in a system (there's no need for CONFIG.SYS device specifications). The directory is normally located on the center cylinder, but the user can specify any cylinder at format time (BOOT.SYS on track 0 points to the directory). Until I learned of MS-DOS's insistence on putting the directory on track 0, I wondered why the drives chugged so much before doing anything!

From the user's perspective, however, the most important feature of any disk operating system is the friendliness and utility of its file-handling features. Here the TRS-80 disk operating systems surpass many popular systems. TRS-DOS and LS-DOS go far beyond simply assigning attributes and access levels to files. Owner and user password protection is provided, and a password may be assigned to protect the entire disk as well.

BACKUP outperforms many commercial backup products I've used under MS-DOS. An irritating feature of MS-DOS (and CP/M) is the archaic need to "log into" a drive and then set up a path to overcome this deficiency. TRS-DOS and LS-DOS will automatically search all on-line drives until the file is found (this means there can be no subdirectory structures, but that's easily overcome by disk partitioning). The meager MS-DOS DIR display has always irked me; TRS-DOS and LS-DOS use the full video display width to show useful information like the number of extents, number of records, protection level, logical record length, and end of file (in addition to the usual stuff).

The TRS-80 Z80-based family has never received the recognition that it deserves for efficiency and functionality. I only hope that the new Z-280 isn't too late to change that.

Jeff Joseph
Wheeling, IL

Sony Singled Out?

We were quite distressed to read Hugh Kenner's review of Fred Warshofsky's *The Chip War* (June).

Warshofsky's original text was incorrect. Although his quote was based on an interview with William Taylor, we suspect that Taylor may have been using the Sony name as being symbolic of all Japanese manufacturers. The bottom line in the story Taylor relates is not "how Sony got into the [TV] business," since Sony never sold private-label TVs to either Sears or RCA.

Jason Farrow
Senior Vice President
Corporate Communications
Sony Corp. of America

Growing Old Gracefully

May the Macintosh never grow old gracefully.

The day that Apple implements Don Crabb's suggestions ("The Mac Interface: Showing Its Age," *Macintosh Special Edition*, June)—most notably the command-line interface that he seems so fond of—is the day I stop buying and recommending Apple computers.

It's not that I wouldn't appreciate some way to batch up repetitive tasks, but I already have that in any of several macro tools (including one that comes with the computer). I cannot think of anything that grep will do for me that direct manipulation or a quick HyperCard program won't do better (with a lot less chance of destroying more data than any virus ever did).

Tom Pittman
San Jose, CA

ASK BYTE

High-Energy Help

I am a computer science major interested in robotics and high-energy physics. I am seeking any information regarding what past issues of BYTE may have had Circuit Cellar projects concerning those subjects. My local libraries and school libraries carry BYTE only from 1985 on. I remember several years ago reading an article in BYTE that dealt with the technical aspects and considerations of constructing a robot manipulator arm. I cannot recall what issue that was in.

Jim Burke
Carrollton, TX

There have been precious few Circuit Cellar articles on topics in high-energy physics. In fact, that's a subject we rarely cover in detail anywhere in BYTE. As for robot manipulator arms, a search through BYTE's back issues revealed "A

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Circle 147 on Reader Service Card

Hobbyist Robot Arm" in our February 1979 issue. Perhaps that's the article you recall. The most recent construction article on robotics that BYTE presented was in our April and May 1987 issues: "Build BERT, The Basic Educational Robot Trainer."—R. G.

Desktop Publishing

I am the computer operator for a small realty company, and we need a good, powerful desktop publishing system and a hand-held graphics scanner. We have an IBM PS/2 Model 50 with 1 megabyte of memory, a 1.44-megabyte 3½-inch floppy disk drive, a 20-megabyte hard disk drive, and a monochrome monitor. We also have an Okidata Microline 320 printer.

Kevin C. Redden
Vanceburg, KY

The Model 50 should be more than capable of handling either PageMaker or Ventura Publisher, both of which are excellent desktop publishing software packages. To install PageMaker, you will also want to buy a full copy of Microsoft Windows 286. PS/2 mice are available from a number of sources.

The Okidata Microline 320 can be purchased as either Epson FX-80–compatible or IBM Graphics–compatible. If you choose PageMaker/Windows, you could try either the IBMGRX driver or the EPSON9 driver. As I recall, Ventura Publisher supports the printer directly.

Take a look at "Handy Scanners" in the June BYTE for a review of popular hand scanners. After you scan your image, convert it to either PCX or TIFF. From there, either PageMaker or Ventura Publisher can merge your scanned images into your layout. The only problem you might run into is disk space—desktop publishing programs and files take up a lot of it.—H. E.

Pass the Drives, Please

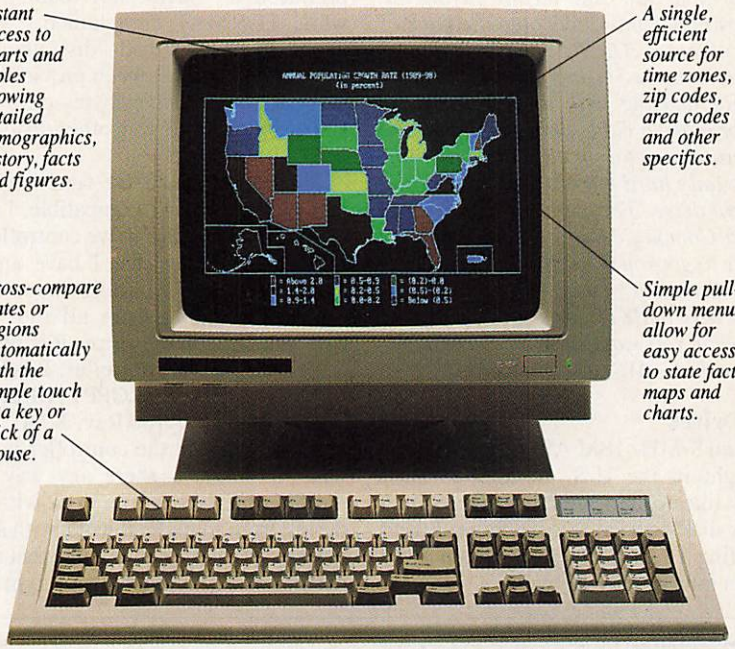
I have a Compaq Portable 386 with an internal 3½-inch floppy disk drive. I have looked all over for a way to install an external 5¼-inch disk drive in this system. Any inspirations?

Scott Kirkwood
Minneapolis, MN

According to Compaq, your Compaq Portable 386 provides for only one floppy disk drive, which can be your choice of either 3½-inch or 5¼-inch. The only way to get the second drive connected is through a second floppy disk drive controller. You'll need one that responds to a

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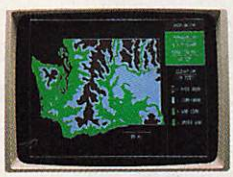
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secondary device address. The CompatiCard I from Micro Solutions (132 West Lincoln Hwy., De Kalb, IL 60115, (815) 756-3411) may be just the beast you're looking for.

To install it, you need a card slot. On the Portable 386, that means buying the expansion box that bolts onto the back of your computer. On the drive side, you'll have to locate a 5¼-inch disk drive in an external housing with a power supply. Find or make a cable that attaches to the external connector on the CompatiCard.

The only hard part here is finding the external drive. The expansion box comes from a Compaq dealer. The dealer may be able to get you the external floppy disk drive. A number of mail-order places advertise here in BYTE, or you can probably find what you want at a local computer flea market.—H. E.

Bad Drives

I own an 8-MHz IBM AT compatible that I bought in the U.S. in May 1986. I would like to add an internal 3½-inch floppy disk drive to this machine. I tried installing a 1.44-megabyte Chinon drive but ran into serious problems.

After configuring the system with SETUP (I told it I had a 720K-byte drive, since it doesn't know about newer 1.44-megabyte drives), I discovered that only DIR and CHKDSK would recognize the drive. Copying files to or from the drive produced a "Sector not found" error, while FORMAT complained, "Invalid media or Track 0 bad—disk unusable." The disk I used had been previously formatted for 1.44 megabytes on an IBM PS/2 Model 80. Trying other disks didn't help, either.

Since the same drive functions flawlessly in an MCI AT compatible, I am assuming that my disk drive controller is at fault. It could be that I have an older model that can't handle these drives properly. Judging from all the "WD" part numbers on the chips, it is probably a Western Digital controller. It is labeled "FIXED DISK - FLOPPY DISKETTE ASSY. 61-031099-00 Rev. X7A."

Assuming that the controller is otherwise in order, is there any way (e.g., jumper settings or some work with a soldering iron) to make it work with a 1.44-megabyte drive? Is it possible that a drive from another manufacturer might work? Failing all the above, is there a cheap floppy disk drive controller that I could add just for the new drive? I'd hate to junk an otherwise perfectly functioning controller for the added convenience of 3½-inch disks, despite the recent low prices for such drives.

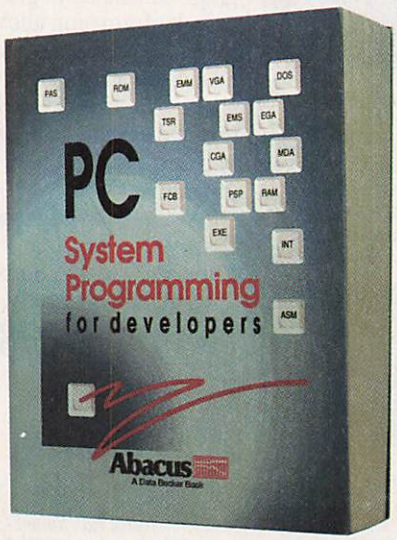
Dr. A. C. Kridiotis
Köln, West Germany

In describing your problem, you failed to mention which versions of DOS are running on your AT and MCI AT compatibles. I'd guess that you are running PC-DOS 3.1 or an even earlier version of DOS on your PC AT. If so, upgrade your system to PC- or MS-DOS 3.3. This newer DOS has the DRIVER.SYS device driver that will enable DOS to recognize add-on disk drives.

Once the newer DOS is on your system, you can add the following line: DEVICE =DRIVER.SYS /D:N (where D is 2 for the new second drive and N is 3 for a 1.44-megabyte 3½-inch floppy disk drive) to your CONFIG.SYS file. The new drive will then be assigned as drive D.—S. W.

continued

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Circle 142 on Reader Service Card (DEALERS: 143)

Bits Across the World

Our newspaper, *YABALASH*, in the State of Qatar on the Arabian Gulf, has a circulation of 50,000 worldwide. Consequently, our office does a lot of corresponding with remote locations daily.

We are looking for a good computerized system to manage our day-to-day office work. We would like to feed it all incoming and outgoing mail and would like to be able to access mail by date and company category. A scanner would also be helpful in handling the mail.

Do you have any suggestions?

A. S. Ahmed
Doha, Qatar

A custom application written for any good database system should be able to manage the mail flow. If this seems unworkable, look around for an office automation consultant. This is a relatively new field, made up of people who specialize in installing office management systems. One of these consultants should be able to point you toward a vertical application specifically geared toward mail management.

As for the scanner, one of the best low-cost optical character recognition systems we've seen here at BYTE is the TrueScan system from Calera Recognition Systems (2500 Augustine Dr., Santa Clara, CA 95054, (408) 986-8006). It's an OCR board and software that work with many flatbed scanners. We've tested it on the Hewlett-Packard ScanJet.

The project you suggest is not a simple one—it will take some time to identify the issues and pick your solutions. A good consultant will make that much easier.

—H. E.

Another Task for Hercules

I have an IBM PC AT–compatible system (AdvanTech SP/AT-800) with a Samsung MA256 monochrome display and a Juko G7-A multidisplay I/O adapter. I have set the adapter to Hercules monochrome graphics mode. My GWBASIC supports monochrome text but does not support Hercules graphics mode. I use the computer mainly for scientific calculations and word processing, so this is not a serious problem. However, my son is crazy about graphics.

Where can I get a version of GWBASIC that supports both the monochrome text and the Hercules graphics modes? Also, can I set the multidisplay adapter to CGA mode without damaging my monochrome monitor?

Ren Yanru
Beijing, China

GWBASIC does not support the Hercules graphics modes, but many of the compilers do. You should take a look at Microsoft's QuickBASIC or Borland's Turbo Basic. Both of these products are GWBASIC-compatible and extend the graphics support to include the Hercules card.

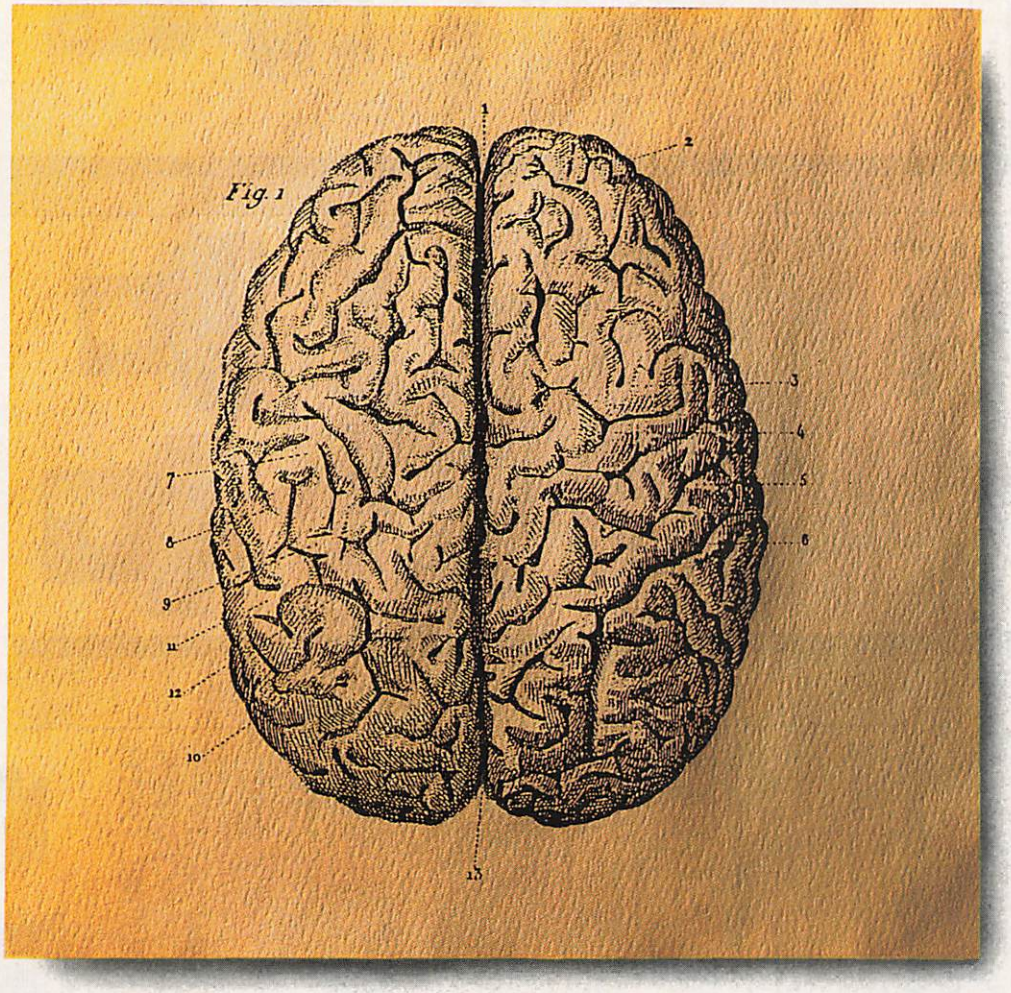
I've been unable to dig up any information on your display card. I've seen other CGA-compatible cards that handle the monochrome monitor perfectly. What does the Juko documentation say about it? The street price on a monochrome monitor around here is less than $60. At that price, I'd risk trying it.

Other multidisplay cards that I've seen require DIP switches to select either Hercules or CGA emulation. Switching to CGA mode will let you run GWBASIC and your son's games, while losing the ability to use the higher-resolution Hercules mode available in QuickBASIC and Turbo Basic.—H. E. ■

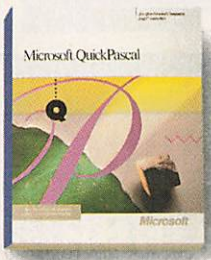


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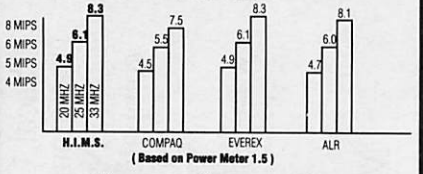
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CHAOS MANOR MAIL

Jerry Pournelle answers questions about his column and related computer topics

Supporting Supercomputers

Dear Jerry,

I noted a bit of incredulity in your April Computing at Chaos Manor with regard to the fact that computer science and mathematics departments account for only 1 percent of the academic use of the National Science Foundation (NSF) supercomputer centers. It shouldn't be that surprising. Computer scientists, like mathematicians, develop basic computing concepts and techniques that are applied in other fields. It doesn't take a supercomputer to test most new algorithms, just a good workstation. The engineers, physicists, and biologists, on the other hand, have massive amounts of data to be processed; thus, they use far more time on supercomputers and always want more.

For computer scientists like myself, who work in computer vision, or those who work in other data-intensive research areas, such as speech recognition, information retrieval, and knowledge-based systems, the type of processing power provided by the supercomputing centers is inappropriate. Our work requires the manipulation of large amounts of symbolic data instead of double-precision floating-point calculations. The supercomputing centers also do not support the interactive capabilities (e.g., real-time image I/O) required or the languages and tools that we need (e.g., Lisp, Prolog, and X Window).

Unfortunately, Congress was sold the idea of the supercomputer centers as the way to advance computer science in this country and to keep our technological edge against foreign competition. What's amazing about all this is that nobody consulted with the computer scientists for advice. The people who were consulted were the engineers, physicists, and biologists. If Congress had asked the computer science community how to bolster computer research, we would have seen a much different program—a program that involved enhanced nationwide networks, advanced display devices like high-definition TV, and parallel processors, such as the Connection Machine and the Cosmic Cube.

Sadly, Congress is now convinced that it is heavily supporting computer science research through the supercomputing centers. It is unwilling to provide significant additional funding for computer science; thus, while ours is the discipline with the greatest expansion in total researchers in the last 20 years, it has seen a net decrease in available federal research funding. The only agency that currently supports any large, focused programs in computer science is the Defense Advanced Research Projects Agency, through its Information Sciences and Technology Office. However, DARPA's budget is also being heavily cut, since the current military cutbacks, as always, are being concentrated on programs with short-term contracts to save those with long-term obligations, such as aircraft carriers and stealth bombers.

Thus, your call for support of increased funding for the supercomputing centers, while it may give the physicists some new toys to help them design their new Superconducting Super Collider, is likely to result in further reductions to the basic research that makes supercomputers work. The $100 million that you told people to ask their representatives to allocate will likely be used to buy the next generation of supercomputers from Japan.

Your efforts would better serve the long-term interests of the country if they were directed at increasing support for basic computing research. $100 million per year would move 10 of our better computer science departments into the upper echelon of research currently inhabited only by MIT, Carnegie Mellon, and Stanford. Alternatively, it could be

continued

Jerry Pournelle holds a doctorate in psychology and is a science fiction writer who also earns a comfortable living writing about computers present and future. He can be reached c/o BYTE, One Phoenix Mill Lane, Peterborough, NH 03458, or on BIX as "jerryp."

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used to build a fiber-optic network that would allow real-time transmission of digitized images across the country, or to buy 20 of the largest parallel processors for computer science and AI research.

I hope that in the future you will use some of your broad influence to encourage others to back increased support of computer science research in addition to computational support for other sciences. Senator Albert Gore is one key official who is leading such a drive, and he would probably welcome additional popular exposure of his plans.

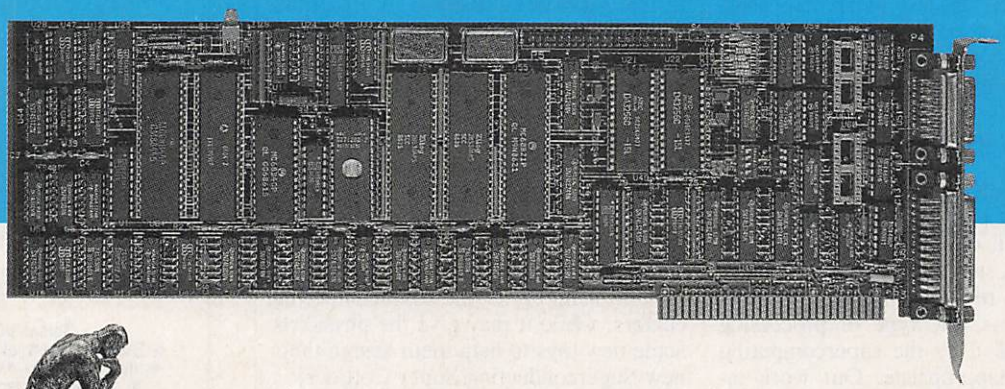
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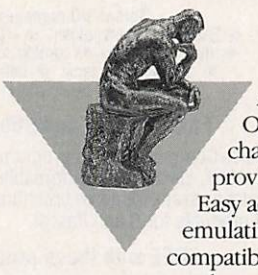
I suspect you exaggerate my influence, although one of Gore's key people turns out to be a former student of mine.

I'm not sure how one goes about "supporting computer science"; a lot of government programs tend to have effects opposite to what was intended. After all, we have *the Connection Machine. As to ARPANET, I agree that it was a Good Thing, but I can't write about it any longer: They closed out my account.*

The problem, it seems to me, isn't my support of the supercomputers; it's that scientists see the science budget as a zero-sum game. That's the wrong approach. Go convince them that support of your project is a good investment.—Jerry ■

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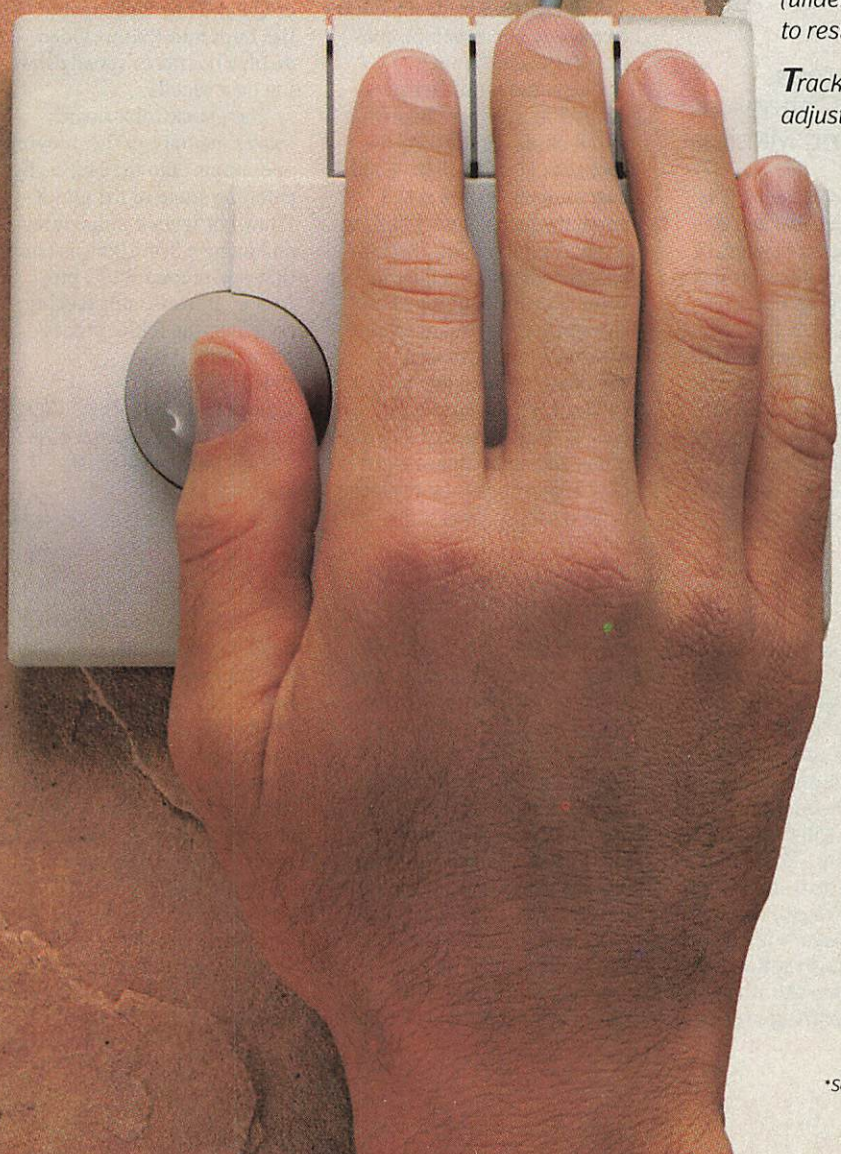
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Circle 209 on Reader Service Card (DEALERS: 210)

MCA QuickCapture Now Has AT Counterpart

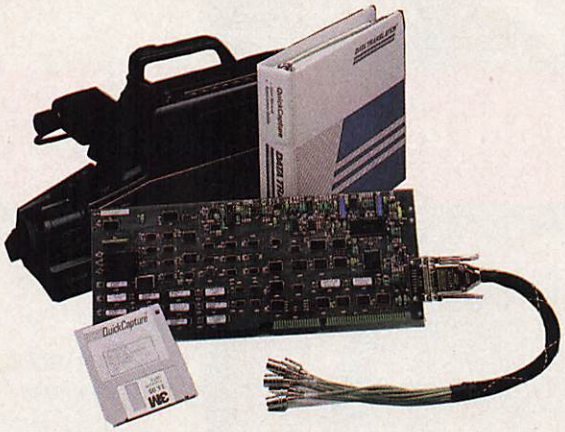
Data Translation's Micro Channel architecture–based QuickCapture frame-grabber board now has an AT-based counterpart.

Like the PS/2 version, the QuickCapture AT captures, stores, and displays images from video cameras, VCRs, and still-video cameras. Both cards use the same software drivers.

QuickCapture AT captures video images in real time (one-thirtieth of a second) and includes a phase-locked loop circuit for jitter-free image capture from VCRs. And when it's used with external video devices, QuickCapture automatically genlocks to the video source or to a separate composite synchronous signal. It can also supply a synchronous signal to display stored images.

You can display the images in real time on any RS-170 RGB (National Television System Committee) analog monitor, with 256 shades of gray and VGA resolution. Each board includes 512K bytes of RAM and an on-board processor. An overlay processor lets you mix text and graphics.

Price: $1995.
Contact: Data Translation, 100 Locke Dr., Marlborough, MA 01752, (508) 481-3700.
Inquiry 1121.



QuickCapture AT captures images in real time.

Audio Comes in Three Channels with Sound Master

The Sound Master PC is an inexpensive audio board and speaker system that lets you mix sound files with moving graphics on your IBM AT or XT.

It features a music/sound chip from Micro Chip, a direct-memory-access-driven 8-bit digitizer, a stereo amplifier, and dual digital joystick ports. Sample rate is variable from 10 Hz to more than 100 kHz. The frequency range has 16 bits of resolution and is adjustable from 50 Hz to ultrasonic.

There are three independently programmable analog output channels with separate frequency and envelope controls for each channel.

The audio amplifier produces 250 mW per channel into 8 ohms. Frequency response is flat to 5 kHz. Total harmonic distortion is 0.2 percent. Each channel has separate, digitally controlled, 4-bit gain stages for adjusting volume or for panning. You can connect the board to an external stereo, booster speakers, or headphones.

The 2¼-inch speakers have an impedance of 4 to 8 ohms and a maximum input of 0.3 W. Frequency response is 50 Hz to 12 kHz.

Price: $89.95.
Contact: Covox, Inc., 675-D Conger St., Eugene, OR 97402, (503) 342-1271.
Inquiry 1122.

Mac II Graphics Acceleration to 600 Percent

The Radius QuickColor Graphics Accelerator board for the Mac II works in tandem with Radius video boards to boost the performance of Apple's 32-Bit QuickDraw by as much as 600 percent, Radius claims.

QuickColor Accelerator uses both the modular design of QuickDraw and capabilities built into Radius video display boards to speed drawing on a Mac II.

The QuickColor board moves the bulk of the drawing operations onto the NuBus by patching some of the QuickDraw bottleneck procedures and using a 5-million-instruction-per-second RISC processor. It loads multitasking code into the RISC processor's static RAM.

Price: $795.
Contact: Radius, Inc., 1710 Fortune Dr., San Jose, CA 95131, (408) 434-1010.
Inquiry 1120.

continued

Big Blue Goes Multimedia

IBM's Audio Visual Connection (AVC) software, coupled with two new Micro Channel add-in boards, brings multimedia capabilities to PS/2s.

They let you combine, edit, and store high-resolution still pictures along with text and full-range audio for multimedia presentations in educational and business applications.

In addition to creating presentations, you can use AVC to develop applications that manipulate business data, such as an audiovisual home database for realtors.

The AVC software offers exact synchronization and mixing of audio, video, and text, plus 256-color image enhancement. You can also change the size and location of screen images, move text over an image without disturbing the graphics, and even animate the image by rapidly displaying a series of graphics. The package uses a hypertext-like technique that lets you link text with related images and audio.

AVC requires an IBM PS/2 with at least 2.5 megabytes of RAM and OS/2 1.1 or DOS 4.0 or higher. It's also IBM Token Ring–compatible. AVC is designed to work with the PS/2 Video Capture Adapter/A, which captures, digitizes, and stores individual images from standard video or computer graphics sources. For the audio side, you'll need IBM's PS/2 Audio Capture/Playback Adapter for analog audio input.

Price: Audio Visual Connection, $495; Video Capture Adapter/A, $2250; Audio Capture/Playback Adapter, $565.
Contact: IBM Corp.; check your local telephone book's white pages or call (800) 426-2468.
Inquiry 1119.

If You Want To Talk Fast DBMS Call 1-800-db-RAIMA™ And Start Screaming

You'll be screaming, all right. db_VISTA III from Raima Corporation combines the flexibility of a relational DBMS and the lightning speed of the network database model.

db_VISTA III is written for C Programmers. Source code available. The interactive database utilities and outstanding documentation make db_VISTA III easy to learn. All applications are portable to VMS, UNIX, OS/2, MS-DOS, even Macintosh. No royalties.

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Features	**Yes**	**No**
db_VISTA 3.1 High Performance DBMS:		
Single and Multi-User available	✓	
Relational B-tree Indexing	✓	
Network Database Model	✓	
Multiple database access	✓	
Referential integrity	✓	
Automatic recovery	✓	
Record & File locking	✓	
RAM resident		✓
db_QUERY 2.1 SQL-based Query:		
Relational Query & Report Writer	✓	
db_REVISE 1.0 Database Restructure Program:		
Total database redesign/restructuring	✓	
Operating Systems*: VMS, ULTRIX, UNIX	✓	
BSD 4.2, SunOS, XENIX, MS-DOS,	✓	
Macintosh and MS Windows, OS/2 compatible	✓	
C Compilers*: Most compilers supported	✓	
C++ compatible	✓	
LANs*: 3COM, Novell, Banyan, AppleShare	✓	
WKS Library:		
Read & Write WKS, WK1 & DBF files	✓	
SOURCE CODE AVAILABLE:	✓	
ROYALTIES: (Absolutely not!)		✓✓

*Other environments are supported; call for complete list.

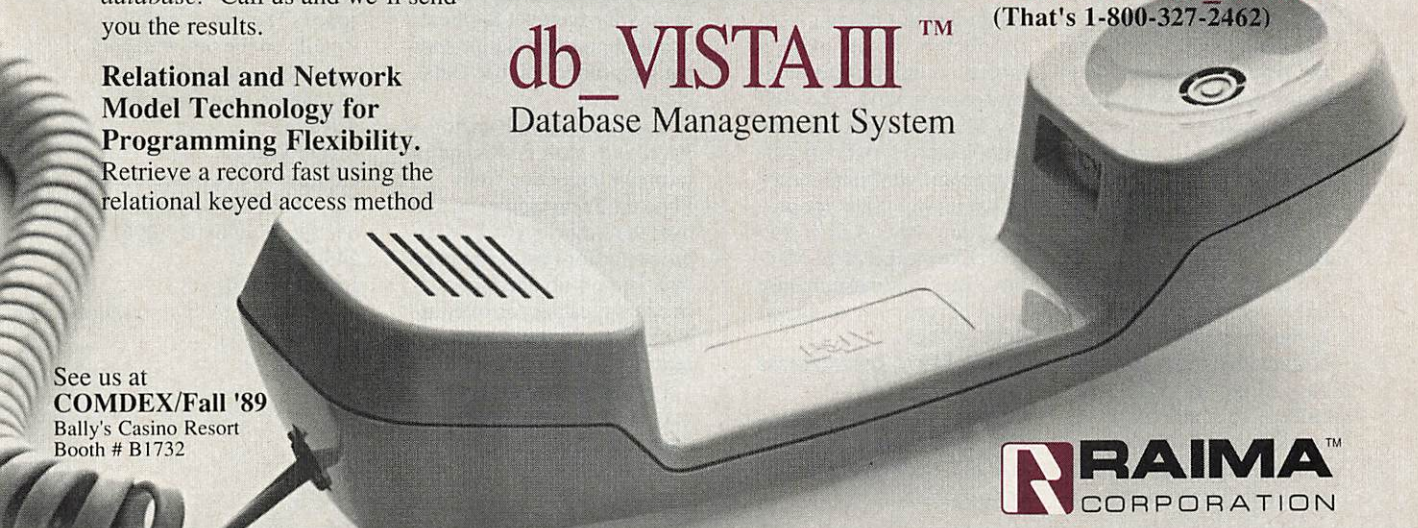
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Kurzweil Reading System Available on PC Platform

The groundbreaking Kurzweil reading machine, which uses a scanner, optical character recognition, and speech synthesis to read documents to the blind and disabled, has finally migrated down from a stand-alone product and is available on a conventional IBM PC platform.

The new PC/KPR products include software, a desktop scanner, and an XT- and AT-compatible interface card. They require a PC with 640K bytes of RAM, DOS 3.0 or higher, and a hard disk drive. The only thing missing that was on the original stand-alone reading machine is a speech synthesizer, which you must purchase separately.

Like its stand-alone predecessors, the PC/KPR reads aloud scanned documents and can store text files for conversion to Braille or transfer the files into standard word processing applications.

Models 15 and 25 both use 300-dpi Ricoh scanners.
Price: Model 15, $3995; Model 25, $4995, optional document feeder, $595; Model 35, $7995; optional document feeder, $1595.
Contact: Kurzweil Computer Products, 185 Albany St., Cambridge, MA 02139, (617) 864-4700.
Inquiry 1124.



Kurzweil's PC/KPR reading machine reads scanned documents aloud, just like the original proprietary system.

Add Two Parallel Ports to Your PC

The LPT:123 is a two-thirds-size 8-bit card that adds two parallel ports to the IBM PC, XT, AT, or compatibles. It is compatible with DOS, Windows, and Xenix, and it is supported by the popular programming languages. You can add up to four LPT:123 adapters to a single personal computer.

Features include I/O address and interrupt-register select switches for each channel. Output is through DB-25 connectors.
Price: $179.
Contact: Commtech, Inc., 8622 Mt. Vernon Court, Wichita, KS 67207, (316) 651-0077.
Inquiry 1128.

PostScript Emulation in a Font Cartridge

PacificPage is a font cartridge that inexpensively turns your LaserJet Series II printer into a PostScript-compatible printer, Pacific Data claims.

You just plug in PacificPage, and, with PostScript interpreter emulation from Phoenix Technologies, it takes over the LaserJet II's 8-MHz processor for PostScript printing. There's no need for add-in boards, cables, or software manipulation, the company reports.

PacificPage gives you access to 35 Apple LaserWriter–equivalent fonts in many point sizes. It also provides all the PostScript capabilities: reversed text, scaled fonts, text rotation, and graphics such as arcs, circles, screens, patterns, and halftone images, according to Pacific Data.

You need at least 2 megabytes of RAM in your printer, and you're limited in print speed because the code in the font cartridges works off the LaserJet's 8-MHz three-wait-state processor.
Price: $695.
Contact: Pacific Data Products, 6404 Nancy Ridge Dr., San Diego, CA 92121, (619) 552-0880.
Inquiry 1125.

Reduce Macintosh Fan Noise with the Fan Controller

If you're tired of the loud fan noise from your Macintosh II or IIx, you might try the Nova Fan Controller from Nova International. The company claims that by continuously varying the fan speed, the Controller can reduce your fan noise by as much as 50 percent.

Nova says that the Mac II fans are factory-set to cool a fully configured system, but a less-equipped system doesn't require the fan's default speed. The Fan Controller installs on the power supply, and a separate sensing unit attaches to your hard disk drive.
Price: $79.
Contact: Nova International, Inc., 435 North 34th St., Seattle, WA 98103, (206) 548-9339.
Inquiry 1130.

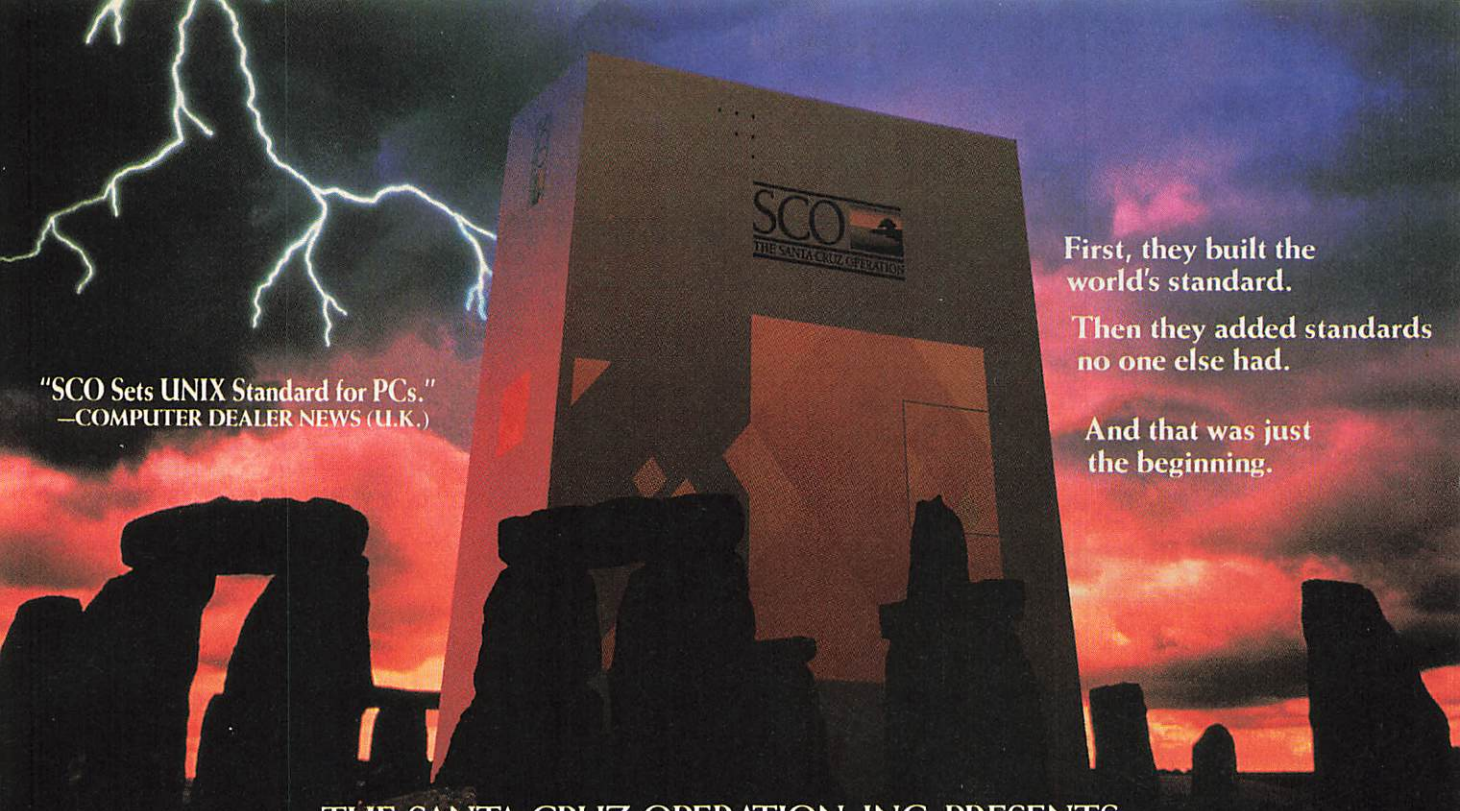
continued

Key Tronic Replaces Your Mac's Keyboard

The MacPro is an inexpensive replacement for Apple's high-end keyboard. It features Key Tronic's capacitance key-switch technology and programmable macro software, and it's compatible with the Macintosh SE, SE/30, II, IIx, and IIcx.

The MacPro looks much like the standard Macintosh keyboard except for a larger L-shaped Return key. The backslash key has been moved from above the Return key to just below it.

The keyboard plugs into any Apple Desktop Bus connector and has its own ADB connector for use with a mouse or other ADB-compatible peripheral. The 105-key MacPro comes bundled with Tempo II, Affinity Microsystems' keyboard macro software, which lets you program any key. And if you don't like the feel of the MacPro's keys, you can purchase a Key Tronic kit to adjust their stiffness.
Price: $197; key-stiffness kit, $15.
Contact: Key Tronic Corp., P.O. Box 14687, Spokane, WA 99214, (509) 928-8000.
Inquiry 1126.



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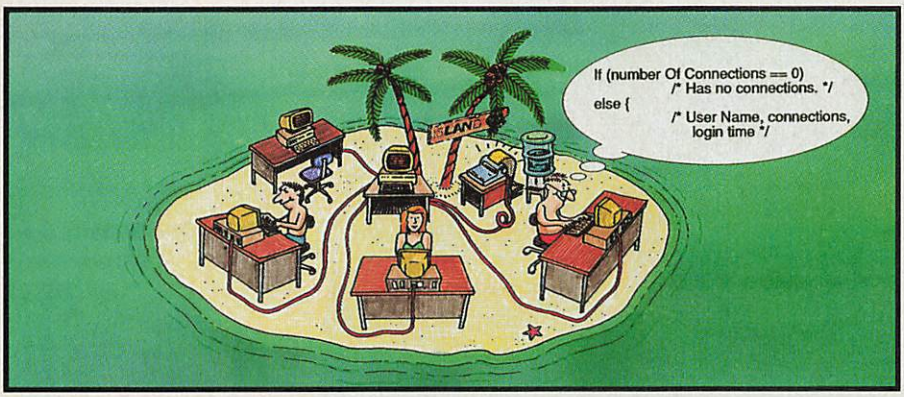
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November's NOVELL month in



***Novell**, the technology leader in the network industry, provides a full array of programming tools designed to streamline the development of distributed applications. Novell's data management tools, connectivity tools, system-level application programming interfaces, and network compilers are optimized for the NetWare environment, so you and your users enjoy the flexibility, reliability and performance you expect from NetWare. When you are ready to build applications that fully exploit the power and flexibility of the NetWare environment, turn to Novell and Programmer's Paradise!*

XQL and NetWare SQL

NetWare SQL is an open interface relational database engine that has been tightly integrated with the NetWare operating system to provide back-end database services to a wide variety of front-end applications including database managers, 4GLs, accounting systems and spreadsheets.

Build your own front-end applications for NetWare SQL using XQL, an open programming interface that provides you with relational access to NetWare SQL databases through two programming levels: ANSI-standard Structured Query Language (SQL) statements and powerful, low-level relational database primitives.

By making simple subroutine calls from C, Pascal, BASIC or COBOL, you can access data by field name, move forward or backward through the database, compute fields from other fields or constants, and even manipulate composite records built from multiple, joined data files. XQL provides a wide range of data types and application-defined buffering for fast data retrieval.

NetWare RPC

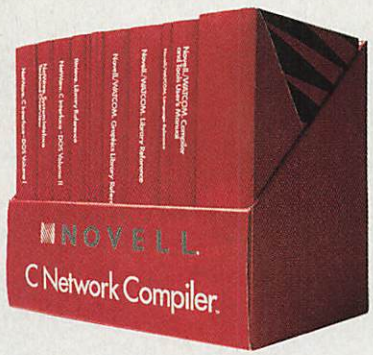
NetWare RPC (Remote Procedure Call) is a set of sophisticated tools designed to assist you in creating distributed network applications. NetWare RPC extends application procedure calls across a network by automatically generating a set of subroutines that allow remote procedure calls to look and act like local procedure call routines.

NetWare RPC raises your development efforts above communication details and frees you from writing to complex IPC interfaces, thereby shortening the development cycle and decreasing the cost of developing distributed applications.

C Network Compiler

C Network Compiler gives you a direct link into NetWare, the leading network operating system with the world's largest installed base of network application users.

Using standard programming techniques and this complete development kit, you can build applications that take full advantage of the NetWare environment.



This 100% ANSI C optimizing compiler is based on technology from WATCOM Systems Inc., and produces object code that out-performs any other C compiler for DOS.

In addition, the C Network Compiler kit includes Express C, a C Graphics Library, a Network Application Design Tutorial, an enhanced text editor, linker, debugger, and other utilities, plus a library of over 300 NetWare application programming interfaces (APIs), including those for the Btrieve record manager.

SPECIAL OFFER!!

The ***Novell C Network Compiler*** gives you a direct link into NetWare, the leading network operating system with the world's largest installed base of network application users.

Order the C Network Compiler from Programmer's Paradise before November 30 and save $95 on the purchase of any other software we carry!

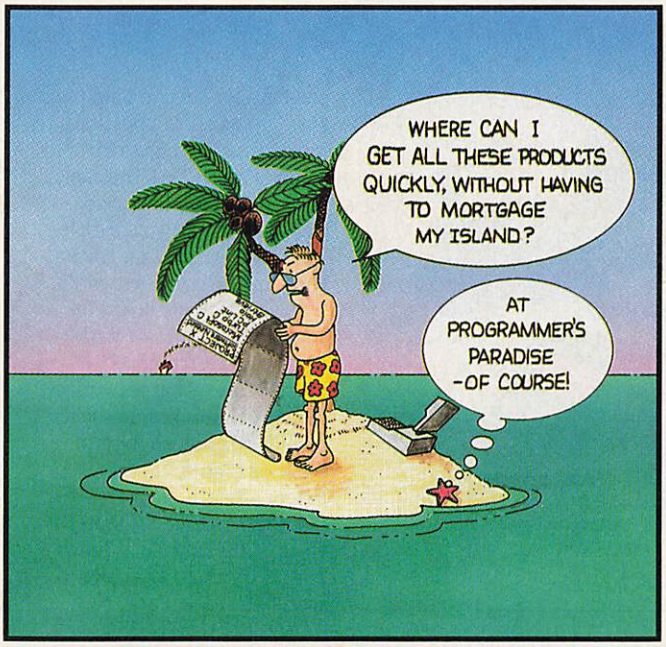
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Paradox/386	895	625
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MS Macro Assembler	150	105
Sourcer w/ BIOS Pre-Processor	140	125
Turbo Assembler/Debugger	150	105
Visible Computer: 80286	100	89
C COMPILERS		
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Lattice C 6.0	250	199
Microsoft C	450	299
MS QuickC	99	69
MS QuickC w/ QuickAssembler	199	135
Turbo C	150	105
Turbo C Professional	250	175
WATCOM C 7.0	395	319

NEW RELEASES

XVT by GSS
Library of C functions providing a common programmer interface across the Apple Macintosh, MS Windows, and MS Presentation Manager. XVT supports events, windows, graph primitives, fonts and text output, cursors, carets, menus, modal and modeless dialogs, file handling, printing, clipboard and a help system.
List: $595 **Ours: $519**

Dr. Switch by Black & White
Memory switching utility. Call any program of any size from any other program all within the limits of 640K. Applications are swapped in and out of memory at lightning speed whether you are using expanded memory, a RAM disk, or saving to disk. Easy to use. Needs less than 15K.
List: $60 **Ours: $55**

C Video Course by Zortech
Learn C without having to spend hundreds of dollars in seminar tuition fees. You get ten one-hour tapes containing 36 lessons from beginner's to advanced. Includes 365-page workbook and free Zortech C Compiler.
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Zortech C++ Video	CALL	CALL
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Breakout II	125	99
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dBC III	250	219
db_FILE Bundle	295	249
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Greenleaf SuperFunctions	299	209
Turbo C TOOLS/2.0	149	115
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C-Worthy w/ forms and source	495	CALL
FaceIt	99	89
Greenleaf DataWindows	395	279
JAM	595	529
Panel Plus	495	395
Vermont Views	395	CALL
w/ source code	790	CALL
Vitamin C	225	165
VC Screen	149	125
Vlib	149	129
C-SOURCE ANALYSIS		
AutoFlow-C	299	269
C/Analyst	150	135
Clear +	200	169
C:Lines/C:Tree	80	75
C-UTILITIES/OTHER		
Code Master v. 2	289	259
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PC-lint	139	105
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Clipper 5.0	695	439
dBASE IV	795	489
FoxBASE+	395	249
Paradox 3.0	725	509
R&R Report Writer	150	129
w/ Clipper/ FoxBASE module	200	159
R&R Code Generator	150	129
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Lahey Personal FORTRAN 77	95	89
MS FORTRAN	450	299
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.RTLink	195	185
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LOGITECH Modula-2:		
Compiler Pack	99	75
Development System	249	199
Repertoire	149	135
TopSpeed Modula-2:		
B-Tree Toolkit	80	72
Communications Toolkit	80	72
Compiler Kit	100	89
DOS 3-Pack	200	179
TechKit	60	55
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Turbo-Plus 5.5	150	129
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Smalltalk/V PM	CALL	CALL
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Whitewater Resource Toolkit	195	169
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Periscope IV/20 MHz	2295	1839
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Circle 289 on Reader Service Card

InterLan Software Links NetWare to LAN Manager

LMN Server allows Novell NetWare nodes transparent access to an OS/2 LAN Manager file server, InterLan claims.

LMN Server runs as a service under OS/2 on any OEM version of LAN Manager. Features include command-line utilities that are similar to NetWare utilities and limited support for NetWare menu utilities, such as SYSCON and FCONSOLE.

Transparent access from LAN Manager nodes to NetWare files, however, isn't yet an LMN Server feature, InterLan concedes, although there is an LMN Server utility for simple file transfer.

Requirements for the LMN Server include an IBM AT, Compaq, or compatible with 4 megabytes of RAM, an InterLan data-link controller (add-in board for 802.3 Ethernet), OS/2 1.0, LAN Manager 1.1, and Novell NetWare 286 version 2.15.
Price: $1295.
Contact: InterLan, 155 Swanson Rd., Boxborough, MA 01719, (800) 526-8255; in Massachusetts, (800) 835-5526.
Inquiry 1131.

Microsoft Adds Store-and-Forward Messaging to E-Mail

Microsoft Mail 2.0, for Macs and IBM PCs, features store-and-forward messaging to send E-mail even when another server isn't available.

The Mail 2.0 server keeps trying at specified intervals and returns the message with an error if it's not received in a specified time. This method, which Microsoft says is also used on global networks such as Internet, means that users don't need a permanent connection to every mail server.

The servers, rather than the users, also handle directory management. When servers are brought onto the mail system, they automatically exchange directory information with the other servers. Microsoft says that Mail 2.0 works on any networking hardware or software that supports AppleTalk networking protocols, including AppleTalk and Ethernet hardware.

Mail 2.0 ships in five packages: a starter kit (Mac server and one workstation), a single-node pack, a 20-node pack, a gateway to MCI Mail, and a gateway to AppleLink.

Price: Mail 2.0 server starter kit, $395; node pack, $125; 20-node pack, $1495; MCI Mail gateway, $595; AppleLink gateway, $295.
Contact: Microsoft Corp., 16011 Northeast 36th Way, P.O. Box 97017, Redmond, WA 98073, (206) 882-8080.
Inquiry 1135.



NetWare and LAN Manager meet with InterLan.

MacRing SE Runs as a Token Ring Node or Bridge

Because Apple Computer's recent connectivity announcements included NuBus adapters and nothing for Mac SEs, h-three Systems has made that SE connection.

The MacRing runs your SE as a Token Ring node, giving you the benefits of 4-megabit-per-second data rates and AppleTalk applications. It also runs your SE with Apple's AppleTalk Internet Router software bridge to transparently tie your AppleTalk network to your Token Ring and Ethernet networks.

Each MacRing board includes 128K bytes of RAM and Texas Instruments' 4-Mbps Token Ring networking chip. Software requirements include Macintosh System 6.0.1 or higher.
Price: $895.
Contact: h-three Systems Corp., 100 Park Dr., Suite 204, P.O. Box 12557, Research Triangle Park, NC 27709, (919) 549-8334.
Inquiry 1134.

DMA Links DOS and Macintosh

pcMacTerm II and pcMacTerm II/Network give you fast data transfer and remote control of PCs and Macs.

The basic products give you bidirectional file transfer between Macintosh computers running System 6.0.2 or higher and PCs and compatibles equipped with at least 256K bytes of RAM. Data transfer is rated at up to 57,600 bps. Graphics to the VGA level are supported, as is a chat window for on-line conversations. Or you can use your computer's on-board LANs for additional communications.

The Network version of the software is for AppleTalk networks, supporting background file transfer under MultiFinder.
Price: pcMacTerm II, $195; pcMacTerm II/Network, $395.
Contact: Dynamic Microprocessor Associates, Inc., 60 East 42nd St., New York, NY 10165, (212) 687-7115.
Inquiry 1136.

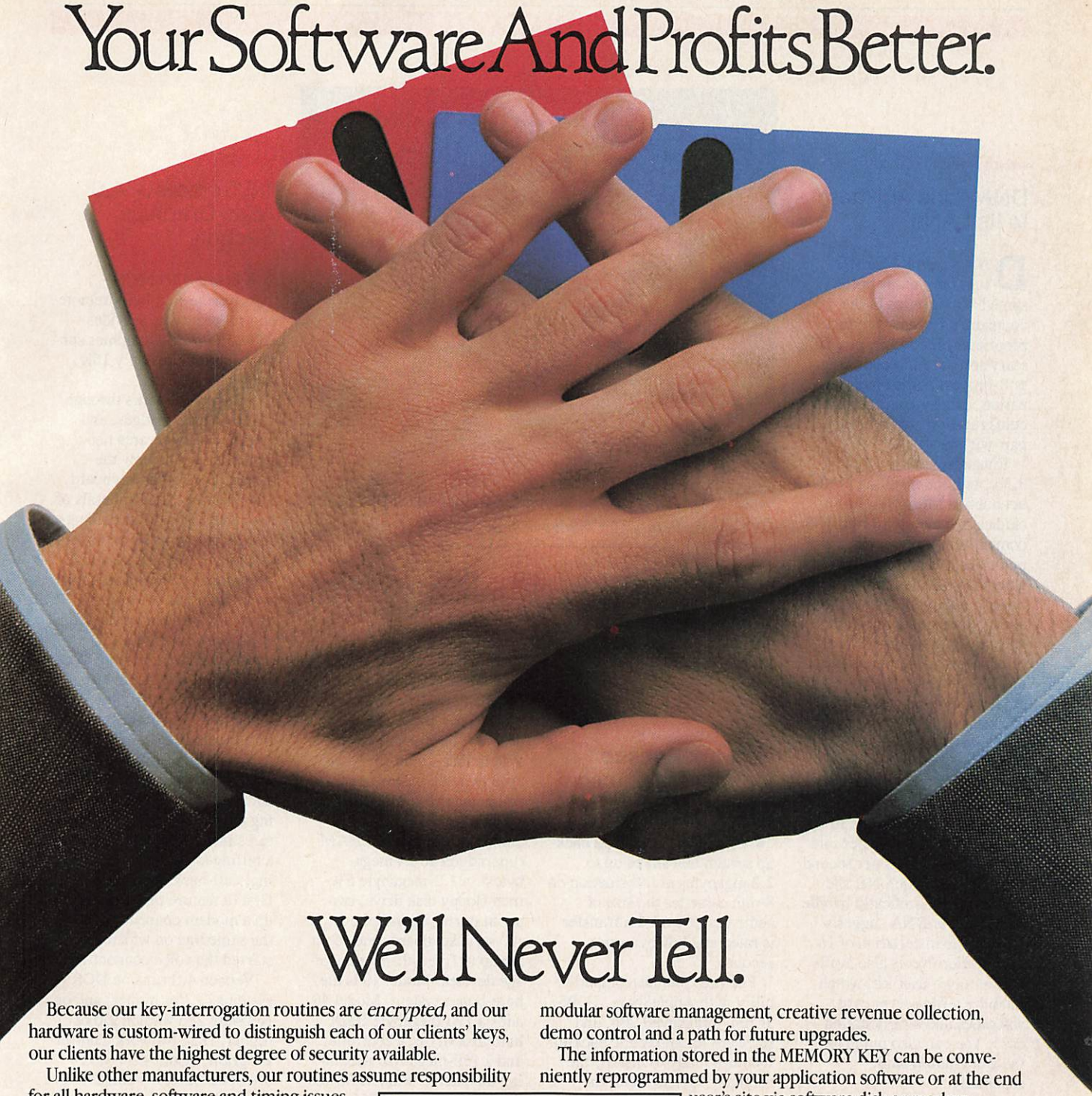
continued

Mac Connection for Sharp's Wizard

The new Organizer Link for the Macintosh lets you transfer your Macintosh files to your hand-held Sharp Wizard computer and vice versa. File transfer was previously possible only with DOS-based machines.

The physical link is through the Macintosh's modem port, and the data transfer rate is 9600 bps. Cables are included in the package.
Price: $149.99.
Contact: Sharp Electronics Corp., Sharp Plaza, Mahwah, NJ 07430, (800) 237-4277.
Inquiry 1133.

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For Americas & Pacific circle 293 on Reader Service Card

DNA Adds Abilities to Its LANs

DNA's new LAN offerings have many of the same basic features of the company's flagship product: proprietary hardware, proprietary software incorporating poll-process collision elimination, a daisy-chain physical configuration, and twisted-pair wiring.

Enhancements to DNA 3.36, with the resulting product dubbed MicroNet, include a menu system; NetBIOS compatibility; messaging capabilities; support for shareable fax machines, fax boards, and modems; and the ability to farm out program executions to other workstations. Memory requirements are 120K bytes at the file server and 12K bytes at the workstation, or you can load parts of both programs in either extended or expanded memory.

Enhancements to the company's hardware include increasing the data transfer rate from 1.25 megabits per second to 2 Mbps. A MicroNet file server can theoretically handle 64 users, but DNA suggests the average installation of 16 users. MicroNet is also available as a two-user kit, which includes a file server card, software, and a workstation card. You can also purchase the workstation card separately.

An entirely new product, which also works with DNA 3.36, is MegaNet. It's a 10-Mbps network for up to 256 users. As with MicroNet, the cards support distances of 500 feet with unshielded twisted-pair cable, and 5000 feet with shielded twisted-pair cable.
Price: MegaNet file server, $695; MegaNet workstation, $395; MicroNet file server, $295; workstation, $195; MicroNet two-user kit, $345.



DNA offers MicroNet for small businesses.

Contact: DNA Networks, Inc., 351 Phoenixville Pike, Malvern, PA 19355, (800) 999-3622 or (215) 296-7420.
Inquiry 1132.

Speedy Network Backup for Your Macintosh

The MaxStream MS2200e is a SCSI-based tape backup system that stores up to 2.2 gigabytes of information on 8-mm cassettes the size of audio cassettes. Data transfer is rated at 233K bytes per second.

Features include compatibility with AppleShare, TOPS, 3Com, and Novell 286, and software for automatic backup. It comes ready to install, the company says, with all the necessary cables and terminators.
Price: $6695.
Contact: Archive Corp., Data Storage Division, 1650 Sunflower Ave., Costa Mesa, CA 92626, (800) 237-4929.
Inquiry 1118.

Mark 386 Unix-Based System Supports 64 Users

The 25-MHz Mark 386 is a Unix-based, 64-user desktop (or optional tower) system that's built for what used to be classified as minicomputer applications.

Standard equipment includes 4 megabytes of RAM (upgradable to 24 megabytes), a 1.2-megabyte 5¼-inch floppy disk drive, two serial ports, a parallel port, an AT-style keyboard, and room for up to five half-height storage devices. Model 10 is the bare-bones system. Model 40 adds a 170-megabyte ESDI hard disk drive, a controller, and a 150-megabyte streaming tape drive. Models 60 and 80 feature 382- and 765-megabyte ESDI drives. The tower chassis lets you have three additional half-height storage devices.
Price: Model 10, $7400; Model 40, $11,100; Model 60, $12,400; Model 80, $16,300; add $1000 for tower style.
Contact: Point 4 Data Corp., 15442 Del Amo Ave., Tustin, CA 92680, (714) 259-0777.
Inquiry 1110.

NETremote + 4.0 Adds Graphics, Security

Version 4.0 of NETremote+, a LAN remote-control program, provides CGA/EGA/VGA graphics support and requires only 15K bytes of RAM.

Version 4.0 works through LANs, across bridges, and even across wide-area networks to let you view the screen, control the keyboard, and even access peripherals of any other IBM PC or compatible. Brightwork Development claims that you can perform bridging and WAN functions twice as fast as you could with previous versions.

You can also use it to monitor large processing jobs. Brightwork says it has also added better security; now the "listening" PC is able to refuse access.

You can now hot-key from an active call to the local PC and back without disconnecting the call. New dial-in features include keyboard chat, a billing log, session recording, call-back, and voice-first (a feature that lets you set up a modem connection on the same line on which you started the voice connection).

Version 4.0 runs on DOS systems (3.1 or higher) and on NetWare 286 version 2.0 or higher, IBM Network Control Program, 3Com's 3+ and 3+Open, AT&T's StarLAN, Banyan's VINES/386, and TOPS. Also new is compatibility with IRMA boards.
Price: One-server version, $350; multiserver version (for up to four file servers), $695.
Contact: Brightwork Development, Inc., P.O. Box 8728, Red Bank, NJ 07701, (201) 530-0440.
Inquiry 1137.

continued



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QNX programmers have a decided advantage.

You see, people who use QNX enjoy the freedom that comes only with a flexible, modular OS. They appreciate the elegance of a **message-passing architecture**. And they marvel at the fact that QNX runs so lean—under 150K—yet out-performs any other PC operating system.

QNX users never worry about whether their applications will make it at runtime, because they know QNX has proven itself again and again in the real world.

It's no wonder that QNX users have achieved so much since the product was first released for the PC in 1982: over 80,000 systems installed in 47 countries world-wide, in all kinds of applications—from making cars to selling books to handling online credit card transactions.

One reviewer dubbed QNX "The multi-everything OS." Now, you might expect multiuser and multitasking, but realtime? *And* integrated networking? *And* true distributed processing? Best of all, these terms take on a new meaning with QNX.

Multiuser, for instance, means up to 32 terminals per micro. **Multitasking** cashes out as 150 tasks per machine. **Realtime** means not only priority-driven, preemptive task scheduling, but also speed: at 6,896 task switches/sec on a 16MHz 286, QNX is at least a full order of magnitude faster than a typical UNIX system. **Integrated networking** means you won't need yet another layer of software to set up a LAN, and you can use *any mix* of Intel-based micros—from vintage '81 PCs to PS/2s.

Distributed processing with QNX sounds too good to be true. But it is: *Any task can access any resource*—programs, files, devices, even CPUs—without going through the bottleneck of a central file server.

Besides the satisfaction that QNX developers get from using a fast, powerful, and flexible OS, did we mention that they also enjoy *free technical support?*

If you're wondering why you don't already know all about this great OS, you could try asking the over-achievers who are smugly guarding the secret of their success.

Better yet, give us a call. We'll tell you everything you need to know to become an over-achiever yourself.

QNX

Circle 305 on Reader Service Card

For more information or a free demo disk, please phone (613) 591-0931.

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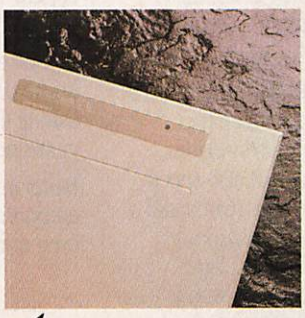
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We kept all the features that have made SummaSketch the industry standard – features that have led to more SummaSketch tablets being used today than any other brand.



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You said you wanted a complete plug and play package, not a basic tablet with a list of optional extras. So we're giving you the works – both in PC and Macintosh® SE and II versions. A 12″ by 12″ or 18″ by 12″ active area tablet; your choice of a four-button cursor and two-button stylus or 16-button cursor; utilities diskette and more. The PC version includes interface cables for the IBM® PC, PS/2, AT and compatibles, while the Macintosh version has a unique Apple® Desktop Bus interface device to connect the tablet to the computer.



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When asked about the one key benefit you look for in deciding on an input device, your answer was productivity. And SummaSketch II delivers.

Unlike a mouse, our stylus gives you a more natural "pen-to-paper" feel for free-hand drawing. Our 4- and 16-button cursors can be programmed to move you quickly through the most sophisticated software. For the PC market, we offer a free tablet template (US and Canada only) that puts hundreds of software commands in view . . . and at your finger tips. No need to memorize commands or scroll through two or three screen menus to use the functions you want.



☑ **Push-button productivity.**

IBM Compatible inquiries circle 342; MAC inquiries circle 343, and dealer inquiries circle 344 on Reader Service Card.



No tablet offers more software compatibility than SummaSketch. Our tablets work with over 250 PC programs and all Macintosh SE and II software written under the Apple Software Developers guidelines.

Since we are the standard, most competitive tablets offer software compatibility by emulating Summagraphics tablets (just look it up in their manuals). In fact, in a recent article comparing IBM PC version tablets, all nine competitive tablet manufacturers emulated Summagraphics in order to provide software compatibility.

But that's not all. Our PC version utility diskette also includes diagnostic test and reset software, an Autodesk® Device Interface™ driver, Universal Mouse Emulator™ and a Microsoft® Windows driver.



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When it comes to digitizing, the one deciding factor every tablet buyer wants (and every tablet manufacturer touts) is accuracy. SummaSketch II tablets have an accuracy measurement of ± 0.015 inches. This figure is based on the average accuracy found over the entire SummaSketch II surface – not just a "sweet spot" found in the center of the tablet. And both the 4- and 16-button cursors come with an easy-to-view cross-hair sight for precise tracing.

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☑ **High accuracy and control.**

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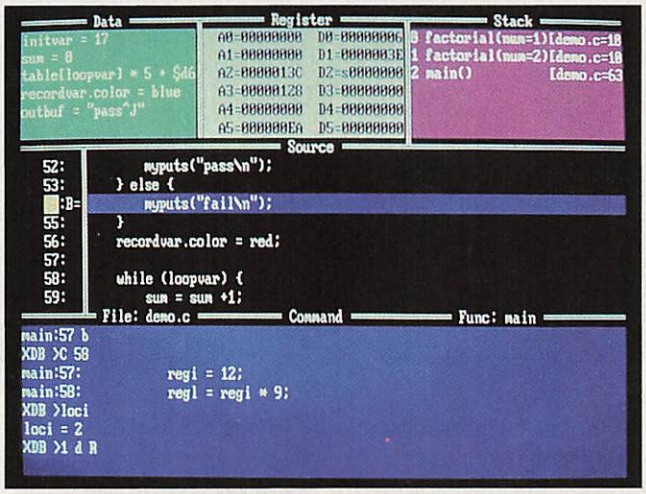
Tools and Utilities for the DSP96002

Intermetrics' newest version of InterTools, the optimizing C compiler, assembler, cross debugger, and utilities library, will support the DSP96002, Motorola's 32-bit, IEEE-standard, floating-point digital-signal-processing (DSP) chip. The new version of InterTools and the DSP96002 should be available in the first quarter of 1990, both companies report.

The 32-bit 96002 is an architectural superset of Motorola's 24-bit 56001 chip. The DSP96002 is compatible with Motorola's 56001 fixed-point products, but it offers speeds of up to 40 million floating-point operations per second and on-chip test and debugging functions, Motorola reports.

The InterTools compiler supports embedded systems development, and the macro cross-assembler provides an interface between 96002 assembly language and C. Utility programs include a linker, a locator, a formatter, a librarian, a symbol lister, and a symbol mapper.

Intermetrics reports that the first development platforms that InterTools will support will be the IBM PC and Sun workstations. Versions will follow about a month later for other platforms, including other Unix workstations, the VAX Ultrix, and the VAX/VMS. Running on the IBM PC, InterTools' compiler requires about 260K bytes of RAM and DOS 3.1 or higher.
Price: $3500.
Contact: Intermetrics, Inc., 733 Concord Ave., Cambridge, MA 02138, (617) 661-1840.
Inquiry 1157.



Intermetrics' cross debugger gives real-time diagnostics in C or assembly language for Motorola's 32-bit DSP chip.

Compile Applications for the NeXT Computer

Absoft's FORTRAN 77 compiler is optimized to run on the NeXT system, allowing you to port programs written for the VAX/VMS, IBM/VS, Sun, and Apollo machines to the NeXT. You can use the program to compile and execute from the standard Unix interface, or you can add a graphical interface to a standard FORTRAN program with the NeXT Interface Builder and the object-oriented superset of FORTRAN 77.

An object created with Object-Oriented FORTRAN can be used the same way as an object created in Objective-C, Lisp, or the Interface Builder, Absoft reports. The compiler uses the same function-calling interface, allowing it to work with C functions.

FORTRAN 77 currently supports version 0.9 of the NeXT operating system; Absoft reports that it will support 1.0 when that is released.
Price: Universities, $750; retail, $1000.
Contact: Absoft Corp., 2781 Bond St., Rochester Hills, MI 48309, (313) 853-0050.
Inquiry 1158.

Oasys, an established provider of compilers for Unix, VMS, and DOS, now has three native compilers for C, Pascal, and FORTRAN on the NeXT system. The Green Hills compilers have language-specific front ends with common back ends that allow you to mix and match different programming languages in the same application.

All three compilers are switch-selectable to emit assembly code for the 68000 family of processors and instructions for the 68881 floating-point coprocessor.
Price: $1500 each.
Contact: Oasys, Inc., 230 Second Ave., Waltham, MA 02154, (617) 890-7889.
Inquiry 1159.

Help for HyperCard Programmers

ICOM Simulations' HyperTMON lets you single-step through HyperTalk scripts line by line, including XFCN and XCMD extensions, so that you can detect mistakes and set multiple breakpoints to isolate bugs before they cause problems. Once you discover a bug, you can immediately modify the offending code.

Once you've installed HyperTMON in HyperCard or the Home Stack, two new menu items appear on the menu bar: HyperTMON and Debug. After you've invoked HyperTMON, HyperCard-like floating windows appear, letting you examine a button's script or examine the contents of variables. You can set breakpoints in the script or single-step through it.

If a script is called by another script, HyperTMON follows it up the hierarchy. As the script executes, the Expressions window updates and displays the present value of local and global variables. You can enter any HyperTalk expression for HyperTMON to evaluate in real time.
Price: $99.95.
Contact: ICOM Simulations, Inc., 648 South Wheeling Rd., Wheeling, IL 60090, (312) 520-4440.
Inquiry 1160.

Somak's ScriptEdit improves the script-editing capabilities of HyperCard's basic script editor. With ScriptEdit, you can open and edit as many script windows as your available memory can handle, and you can use Find and Replace functions to search through the open scripts. You can also use the Find and Replace functions on all scripts of the current card.

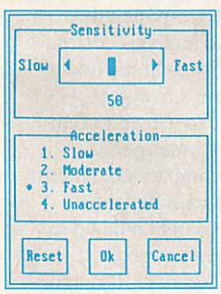
Other HyperCard functions, including all navigation commands, are available while ScriptEdit is open, and the program saves all font, size, and window positions for each script. Script windows contain an index to all stack objects and are instantly updated when changing cards.
Price: $79.
Contact: Somak Software, Inc., 535 Encinitas Blvd., Suite 113, Encinitas, CA 92024, (619) 942-2556.
Inquiry 1161.

continued

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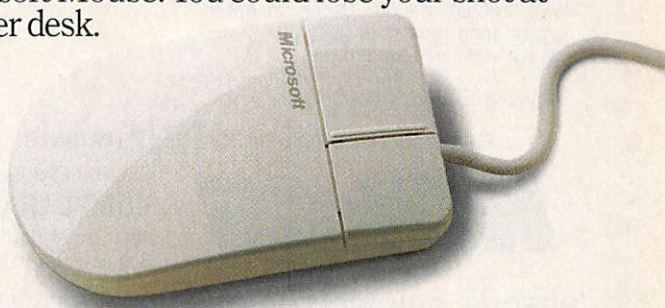
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- Shadow RAM, Clock, Battery, AMI BIOS
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4. AT 386-25MHz (25MHz CPU) W/0K W/Chips 82C307 Cache Controller.....$1395
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6. Baby 386 SX Motherboard W/0K.....$375

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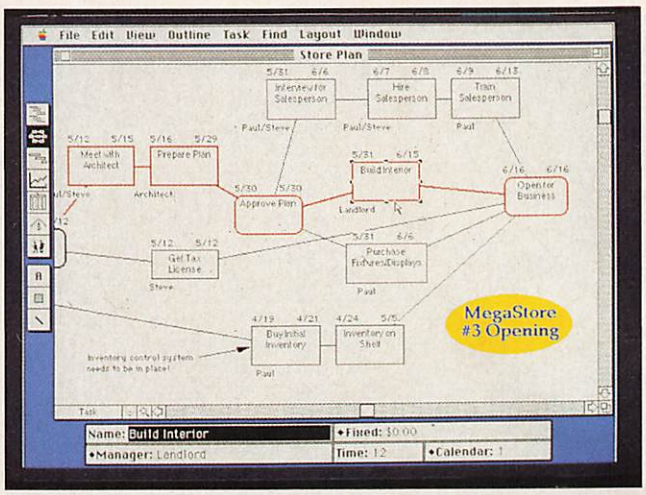
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To build a network view with KeyPlan, you pull your topics from the outline.

Project Management on the Mac

According to Symmetry, the problem with most project management programs is that they are designed for those who already know how to manage a project. If you're new to the profession, project management programs have a steep learning curve. With that in mind, the company developed KeyPlan, which lets you start your project management with nothing but a to-do list.

KeyPlan's integrated outliner lets you outline and attach data to tasks that you can then convert to a PERT or Gantt chart. To create charts, you select and drag tasks, bars, headings, and other elements into place. The program creates a Gantt chart automatically from your outline.

The program lets you track actual against planned time lines. When you plot your data in a bar chart, you can highlight a peak area (e.g., an inordinate number of delays) and click on it to display the cause.

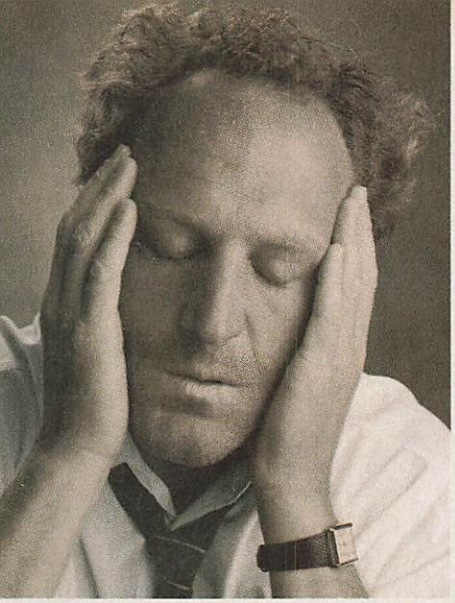
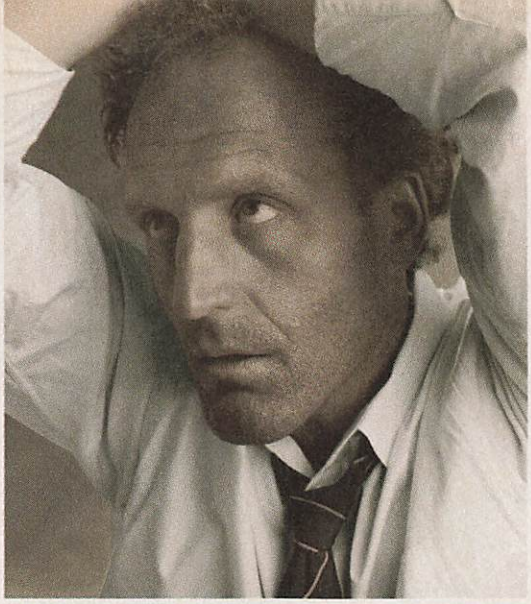
KeyPlan supports color, all installed fonts (including PostScript), and the Clipboard. It works on the Mac Plus or higher.
Price: $449.
Contact: Symmetry Corp., 225 East First St., Suite 107B, Mesa, AZ 85201, (800) 624-2485 or (602) 844-2199.
Inquiry 1138.

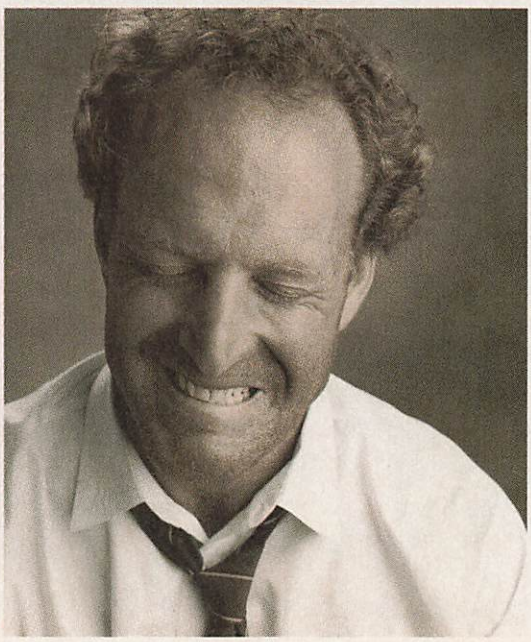
Micro Planning International, known for its project management programs that run on the Macintosh and on the IBM PC under Windows, recently released a new version for the Mac that can handle multiple projects and subprojects, and up to 10,000 activities.

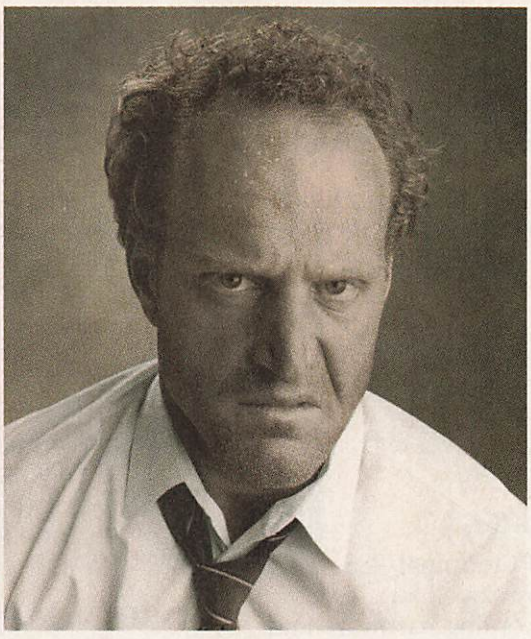
Called Micro Planner X-Pert, the program includes earned-value analysis costing and the ability to break down work structures to eight levels. You can use up to four different cost rates per resource and compare actual cost information with budgeted cost. X-Pert can handle up to 200 calendars per project; 100 zone, responsibility, and cost labels; and 50 subprojects with 1364 records.

Micro Planner X-Pert runs on the Mac SE and II with at least 2 megabytes of RAM.
Price: $1995.
Contact: Micro Planning International, 235 Montgomery St., Suite 840, San Francisco, CA 94104, (415) 788-3324.
Inquiry 1139.

continued





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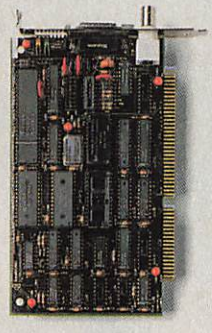


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NETWORKING vs. NOTWORKING.

Both the Samsung 386AE and PCterminal/286 have been tested exhaustively by Novell for compatibility with popular networking hardware and NetWare products. In fact, no other LAN hardware has ever undergone such extensive testing.

But then Samsung and Novell didn't set out to design just another make-do desktop computer.

Samsung's 386AE Fileserver, for example, was designed from the bus up to be a high-performance fileserver, starting with its Novell-developed BIOS. It also sports eight expansion slots for the inevitable inventory of interface and controller cards. Plus an oversize power supply capable of driving the requisite 100 megabyte-plus hard disk, tape backup system, etc. And it includes 4 megabytes of high-speed RAM for disk caching.

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To maintain NetWare compatibility throughout

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your network, choose Samsung's PCterminal/286, a Novell-tested LAN workstation. Inside you'll find a built-in Ethernet interface adapter, and functional features like Novell's NetWare Autoboot EPROM.

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LOOK FOR THE CO-LABEL.

The partnership between Samsung and Novell has created a hardware/software compatibility standard unparalleled in the industry. That means your network can experience all the speed of Novell's new 386 NetWare without being subjected to a lot of hardware hiccups.

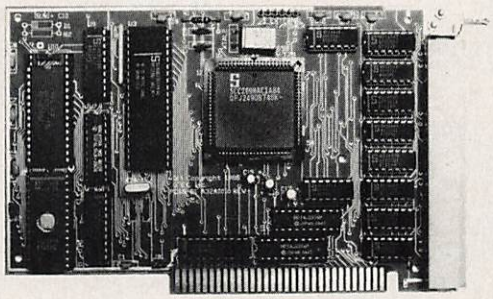
Just look for the Samsung/Novell co-label. You'll find it at your nearest reseller. For the location, call **1-800-366-7472.**



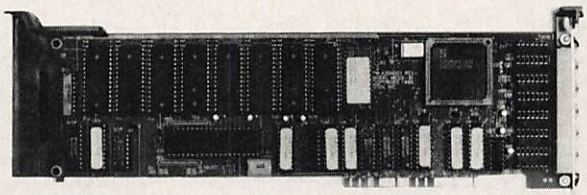
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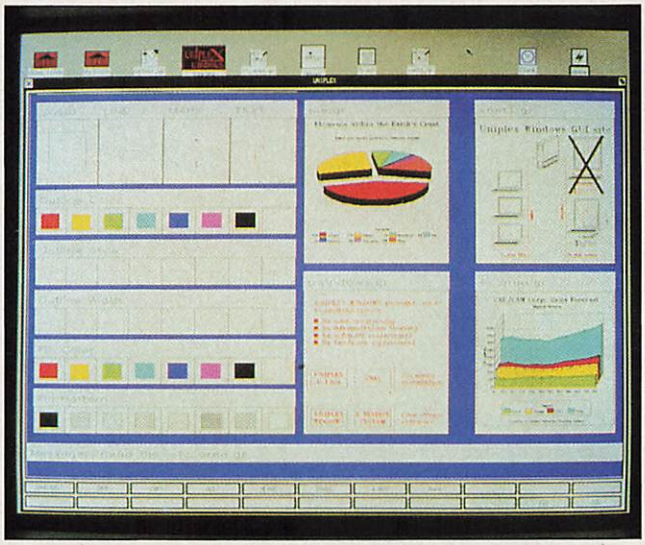
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Uniplex Windows will support any X Window 11.3–based implementation, Uniplex reports.

Uniplex to Run Under X Windows

Uniplex, the Unix multi-user office system with word processing, spreadsheet, E-mail, and relational database capabilities, is now available running under the X Window graphical user interface (GUI). The new version will allow X Window or compatible terminals to display Uniplex Business Software through multiple overlapped windows with icons and mouse commands.

Uniplex Windows works like a terminal emulator: What you see is a view of the program through an X Window GUI. The same Uniplex application that runs on character terminals drives the X terminals, with Uniplex Windows acting as the intermediary between Uniplex source code and what you see on the terminal. If you have terminals that support X Window, and others that support character-based programs, Uniplex Windows will let you use both, the company reports.

The program will support any X Window 11.3 implementation, and the new release uses the Athena Toolkit and technology from IXI Limited for the GUI. Uniplex reports it is also working on a version to support Motif.
Price: $175 to $300 per user.
Contact: Uniplex, 150 West Carpenter Freeway, Irving, TX 75039, (214) 717-0068.
Inquiry 1144.

Database for Legal Case Notes

For Legal Case Notes is a database that lets you track case notes and statutes of note. You can use the program to find cases and statutes by topic, case name, or subject. You can print reports on cases and statutes by criteria that you specify. HomeCraft reports that the program, which is designed for people who aren't DBMS experts, can handle up to 10,000,000 cases and allows you to cross-reference notes. For Legal Case Notes runs on the IBM PC with 256K bytes of memory.
Price: $99.95.
Contact: HomeCraft Computer Products, P.O. Box 974, Tualatin, OR 97062, (503) 692-3732.
Inquiry 1143.

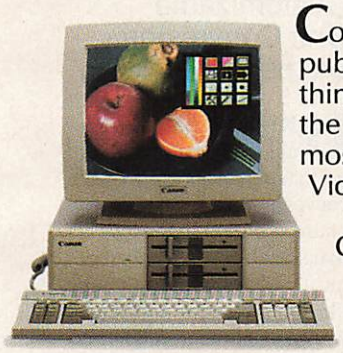
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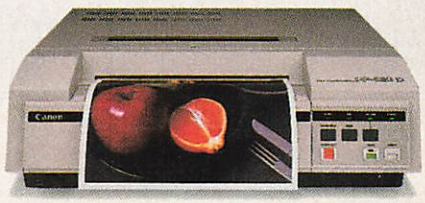
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Canon has a wide range of still video cameras. There's the Xap Shot, a basic combination recorder/player that's easy to use. There's the RC-470, with extra high resolution that can potentially raise horizontal resolution to 400 lines! And there's the RC-760, with a 600,000 pixel CCD—the highest of any still video camera.

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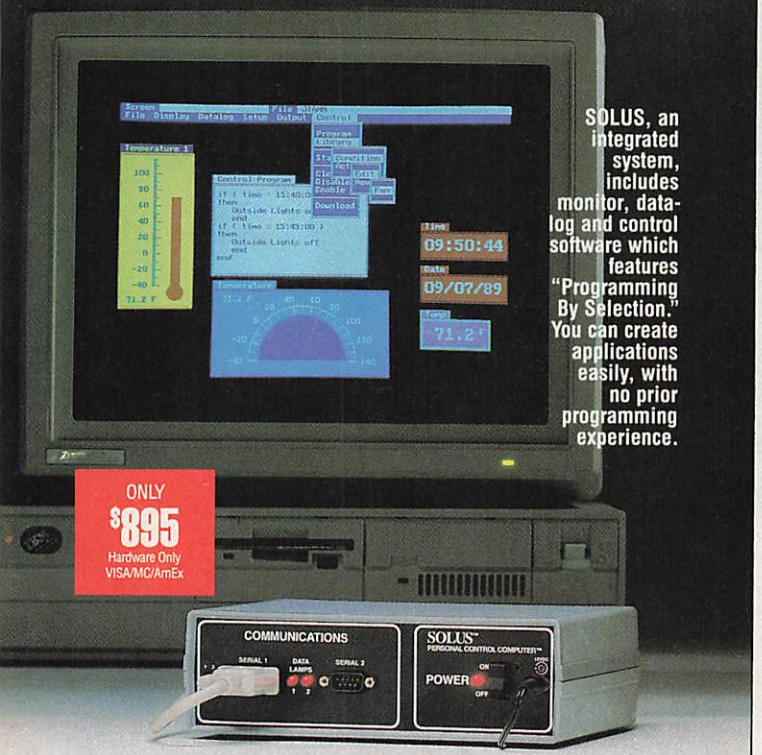
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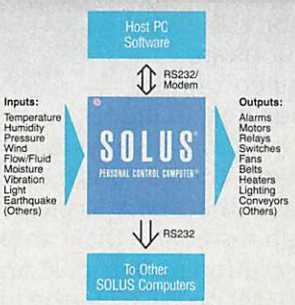
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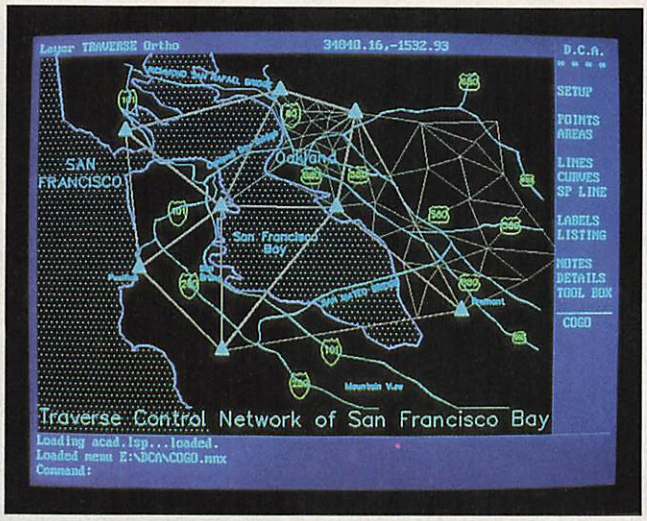
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The Surveyor, a coordinate geometry program for surveyors and civil engineers, can handle sites as large as San Francisco.

Survey and Coordinate Geometry Program

D.C.A. Engineering developed the Surveyor for civil engineers and surveyors who need a coordinate geometry program to process raw field data and use it to develop site plans. After you've manually entered the data from field notes or downloaded it from a hand-held computer through your IBM PC's serial port, the Surveyor's subroutines will perform all necessary geometric calculations, such as intersection points and traverse adjustments.

After the program has reduced the raw data, you can use it to subdivide a lot into smaller lots, design rights-of-way, and position houses. The Surveyor can handle up to 250,000 lots; other capabilities include complete point protection, automatic calculation of lots, building ties, and setbacks, lot and polygon storage, and automatic lot recalculations.

The stand-alone program is compatible with D.C.A.'s civil engineering programs, such as Design, DTM, and EarthWork (for site design, digital terrain modeling, and earthwork calculations). The Surveyor runs on the IBM PC with DOS 3.0 or higher and 640K bytes of RAM.
Price: $2995.
Contact: D.C.A. Engineering Software, Inc., P.O. Box 955, Henniker, NH 03242, (603) 428-3199.
Inquiry 1151.

Customizable Unit Conversion on the Mac

UNITize 1.3 is a modifiable unit-conversion utility that performs almost 200 conversions (e.g., ounces to pounds, or feet to inches) that scientists and engineers must make. If it doesn't handle the conversion you need, you can add the needed units to the program's quantity set.

UNITize 1.3 runs on the Mac 512KE or higher.
Price: $79.95.
Contact: Rainbow Bridge Software, Inc., 4243 Hunt Rd., Suite 210, Cincinnati, OH 45242, (800) 548-8871 or (513) 984-6861.
Inquiry 1155.

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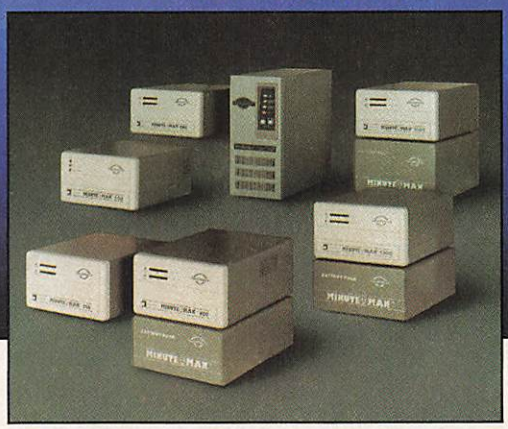
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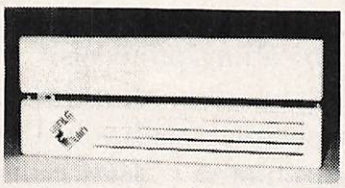
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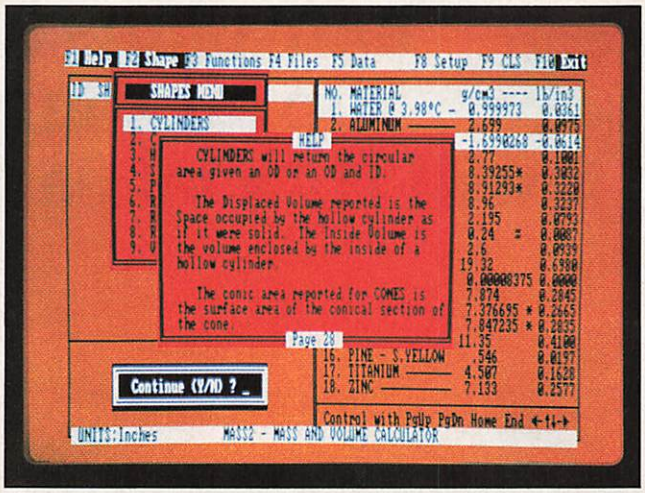
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Mass2 can calculate the weight of a container, what's inside it, and the combined weight of both.

What Does It Weigh?

Mass2 is a mass and volume calculator that you can use to calculate the weight of an object or a shape. The program calculates the volume of any geometrically defined shape and uses its database of materials to calculate the final weight.

The program accepts input in decimal, fractional, or scientific notation. It has a center-of-gravity calculator and can determine mass if the volume is already known. The program's database has over 700 entries, including construction materials, gases, plastics, rocks, and minerals.

Mass2 works on the IBM PC with 384K bytes of RAM.
Price: $69.
Contact: Dempsey's Forge, Software Division, Route 2, Box 407, Gladys, VA 24554, (804) 283-4602.
Inquiry 1154.

Engineering and Drafting on the Mac II

Ashlar says that Vellum, its new Mac II design and drafting program, is software that thinks. It simplifies mechanical engineering, design, drafting, graphics, and technical illustration tasks with the Drafting Assistant.

The Drafting Assistant automatically pinpoints and aligns geometry as you draw. For example, if you're drawing a symmetrically shaped object, Ashlar Vellum will pick up midpoints, intersections, perpendiculars, and so on, and align them based on the geometry already entered. You can make rough sketches of an object, and Vellum will align it for you and let you attach values to it. You can also enter variable dimensions into a drawing and then store the variable parameters for repeated use.

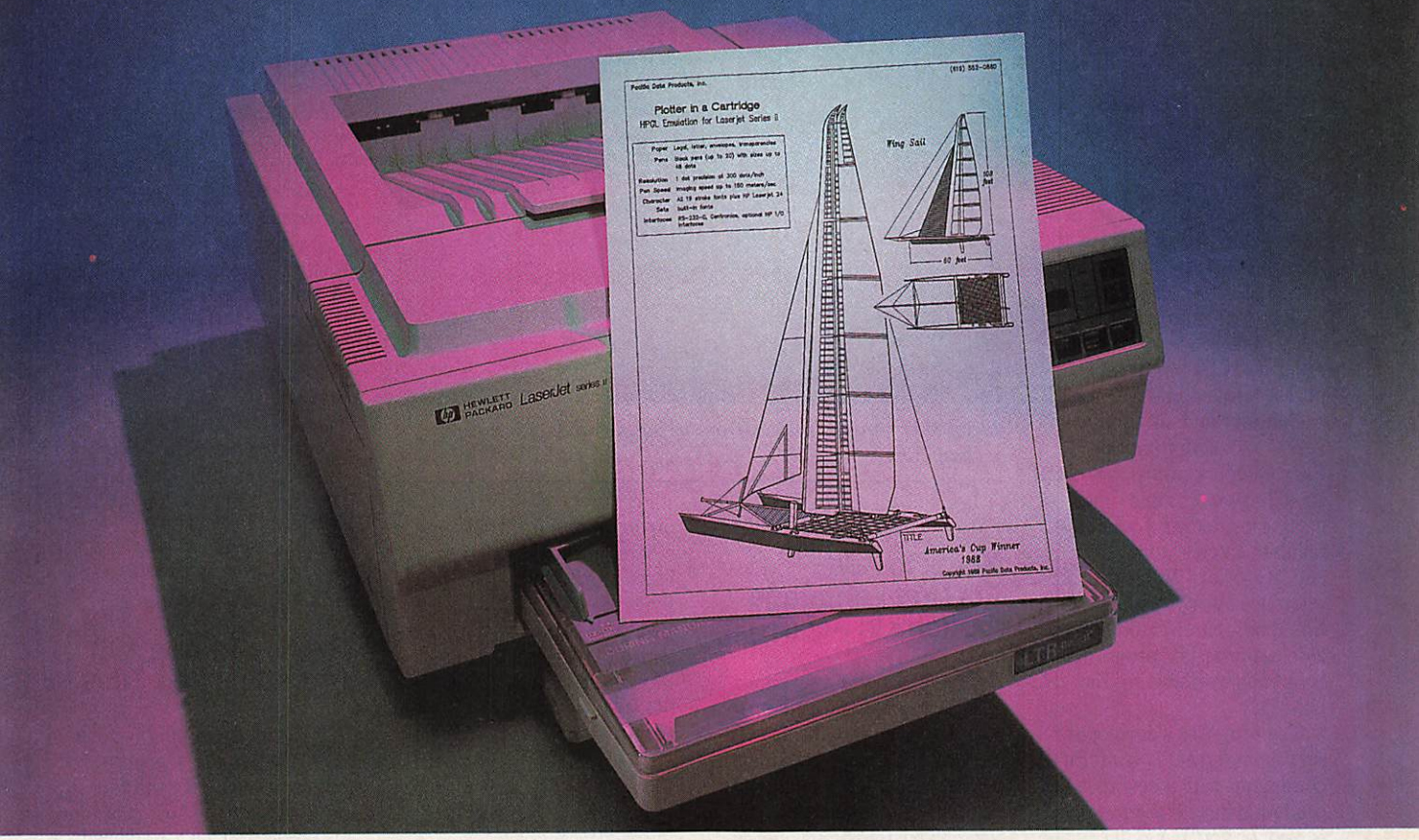
With Vellum, you can create and edit nonuniform rational B splines. It gives you double-precision floating-point accuracy to 16 decimal places. Other features include 256 layers, seven colors, eight line widths, and 11 line styles. The program supports drawing sizes A through E.

Vellum requires a Mac SE/30 or higher with 4 megabytes of memory and a hard disk drive.
Price: $995.
Contact: Ashlar, Inc., 1290 Oakmead Pkwy., Suite 218, Sunnyvale, CA 94086, (408) 746-3900.
Inquiry 1152.

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The Wait is Over.





HPGL Emulation for HP's LaserJet Series II

Now you can produce precise, high quality plots without the wait required by pen plotters or PC-based emulations. Pacific Data's *Plotter in a Cartridge* is the newest and fastest way to emulate HPGL on your laser printer. In fact, it's as much as 100 times faster! Complex engineering or architectural plots taking 10 to 20 minutes on a plotter can be completed within 10 seconds! Crucial when multiple revisions and check plots are needed.

But there's more to *Plotter in a Cartridge* than speed. In addition to standard pen plotter features, *Plotter in a Cartridge* enables you to define 20 pens and 48 widths, automatically scales to fit envelopes, letter and legal size paper and improves resolution to 1/300 inch. And, you can produce up to 99 quality copies and use virtually any media source.

Because the cartridge plugs right into your printer, you can plot directly from CAD/CAM, engineering, or graphics software.

Plotter in a Cartridge combines plotter precision with laser speed.

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Circle 265 on Reader Service Card (DEALERS: 266)

Fishing for Ideas on the Mac and PC

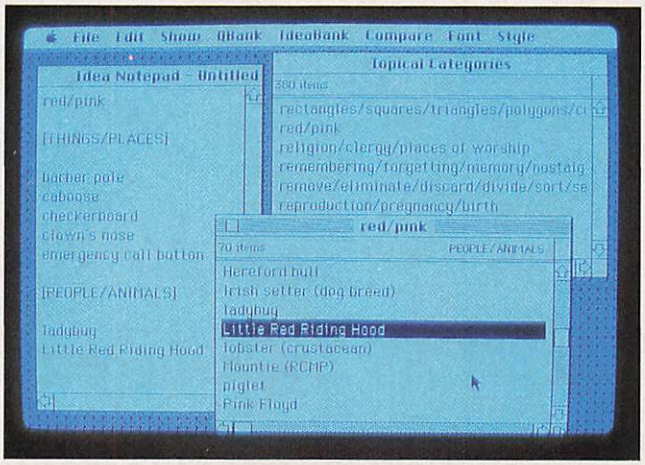
IdeaFisher, the database that helps you generate new ideas when you've reached a mental block, will be available in a Macintosh version this month, Fisher Idea Systems reports. The program consists of 60,000 idea words and phrases linked into 373 broad categories, such as "controversy" or "action/motion." Each category points to a list of subsidiary words and other categories, letting you cross-tabulate entries from different categories. With the cross-reference ability, you can link more than 675,000 direct associations. The program is already available for the IBM PC.

The program's developer says the program is good for coming up with a new idea or product name. If the problem is hazy or you're having trouble framing exactly what you want, you can use the program's QBank.

QBank asks you a series of up to 3700 questions to clarify the exact problem you're trying to solve and compare the ideas it generates with the original objective. After you've developed a list of central ideas, you use the IdeaBank to generate idea associations.

On the Macintosh, you'll need a Mac Plus or higher with about 6 megabytes of storage and 1 megabyte of RAM. On the IBM PC, you'll need DOS 3.1 or higher, 640K bytes of RAM, and 14 megabytes of free space on your hard disk drive.

Price: $495.
Contact: Fisher Idea Systems, Inc., 18881 Von Karman, Suite 100, Irvine, CA 92715, (714) 474-8111.
Inquiry 1145.



IdeaFisher can prevent you from seeing red when you have a mental block.

Xerox to Add Foreign Language Options to AccuText

Xerox is adding seven foreign language options to its AccuText recognition software. Each foreign language option will have its own 50,000-word lexicon, which you can customize by adding an additional 10,000 words. Xerox says it will ship versions designed specifically for the French, Spanish, Italian, and German languages in the fourth quarter of this year. Dutch, Swedish, and Norwegian versions are expected for the first quarter of 1990.

AccuText is based on Kurzweil AI technology. With a supported scanner, you can use the program to scan text in its original format, including tabs, and the program can be set to automatically avoid graphical images. Six expert modules work on the text. The program can handle fonts from 8 to 24 points, and when scanning, it opens up the font in your word processor that most closely resembles the font of the scanned document.

AccuText now supports the Hewlett-Packard ScanJet Plus scanner and works with Microsoft Word, MacWrite, Excel, and WordPerfect for the Mac. The program works on the Mac II or SE/30 with a hard disk drive and 4 megabytes of memory.

Price: $995.
Contact: Xerox Imaging Systems, 1215 Terra Bella Ave., Mountain View, CA 94043, (415) 965-7900.
Inquiry 1146.

Scalable Fonts at 300 dpi Without Big Bucks

Express Publisher, Power Up!'s low-end desktop publishing program for IBM PCs, offers scalable fonts, support for 300-dpi scanned images, and the ability to link text frames and pour copy across multicolumn, noncontinuous pages.

AGFA Compugraphic developed the fonts, which are device-independent. You can change font styles, attributes, and type sizes (from 6 to 144 points) for everything from a single letter to an entire page on the fly, the company reports.

You can import clip art and graphical images in TIFF, PCX, EPS, IMG, and ART format into a document and then crop, flip, or rotate the image. Express Publisher can wrap text around irregularly shaped images.

The program's import filters can import text with formatting intact from Microsoft Word, WordPerfect, WordStar, DisplayWrite, and ASCII and DCA (Document Content Architecture) text. The program also works directly with Microsoft Works.

You can run Express Publisher on any IBM PC with 640K bytes of RAM, a hard disk drive, and DOS 3.0 or higher.

Price: $149.95.
Contact: Power Up! Software Corp., 2929 Campus Dr., San Mateo, CA 94403, (415) 345-5900.
Inquiry 1149.

Switch Among 100 Programs and Files

PC task switching is not a new product category, but Better Software's Switch-It program lets you switch among 100 programs on a standard IBM PC. The program itself uses only 24K bytes of RAM and doesn't require an 80286-based machine with 3 or 4 megabytes of memory to run efficiently, the company reports.

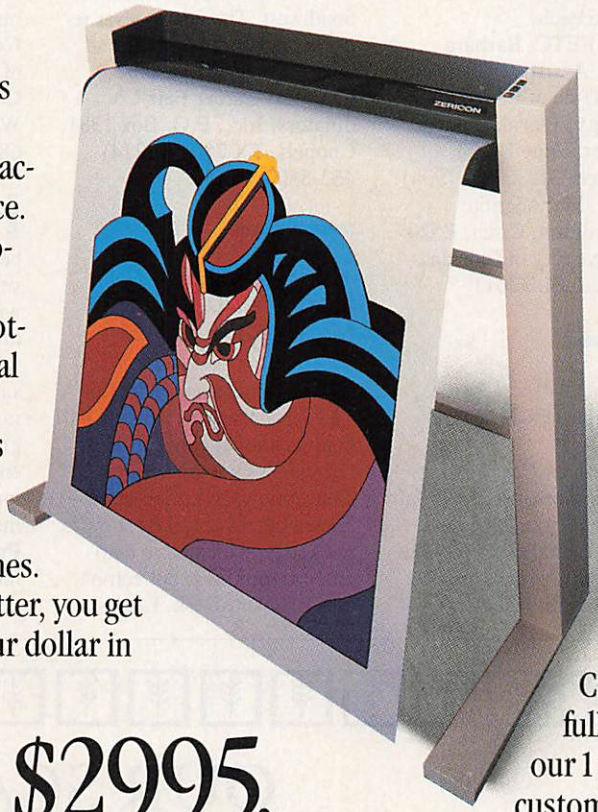
When you install Switch-It, the program automatically scans your hard disk for programs it recognizes and builds a list of applications among which you can navigate. The program is compatible with Microsoft Windows, Ventura Publisher, and OS/2 in real mode. With Switch-It, you can execute any DOS command as you run an application. It also remembers your last 30 commands, which you can recall, execute, or edit.

Switch-It supports extended and expanded memory.

Price: $79.95.
Contact: Better Software Technology, 55 New York Ave., Framingham, MA 01701, (508) 879-0744.
Inquiry 1147.

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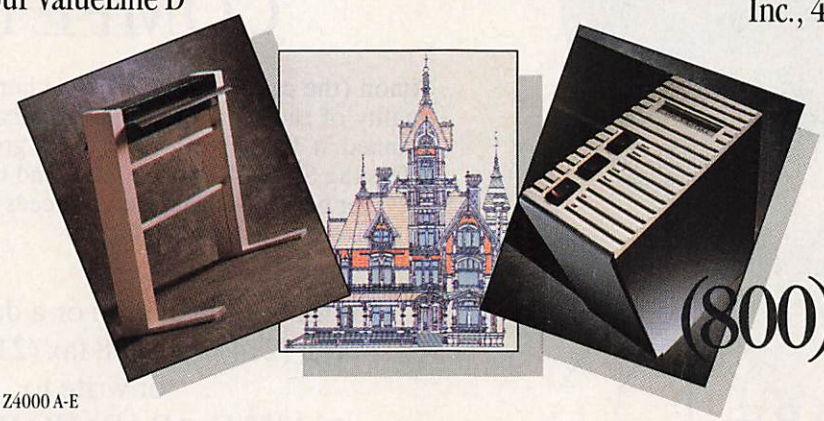
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LCD MENU			X	X
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WHAT'S NEW

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Technology and Education Conferences

Education and computers will be the subject of two concurrent conferences that will be held in Daytona Beach, Florida. Both the tenth Florida Educational Technology Conference (formerly the Florida Instructional Computing Conference) and MacAdemia Southeast '90 will be held from January 30 through February 2.

FETC will be held at the Daytona Beach Ocean Center. MacAdemia, sponsored by Florida colleges and universities and Apple Computer, is for postsecondary educational professionals. It will be held at the Daytona Beach Marriott. Attendance at MacAdemia Southeast '90 is limited to the first 500 to register.
Price: $25 each.
Contact: FETC: Barbara Ann Cox, Assistant Chair FETC, Office of Educational Technology, Florida Education Center, Suite B1-54, Tallahassee, FL 32399, (904) 488-0980. MacAdemia: Laura Kittleson, Circa, E520 CSE, University of Florida, Gainesville, FL 32611.

Career Fair for High-Tech Pros

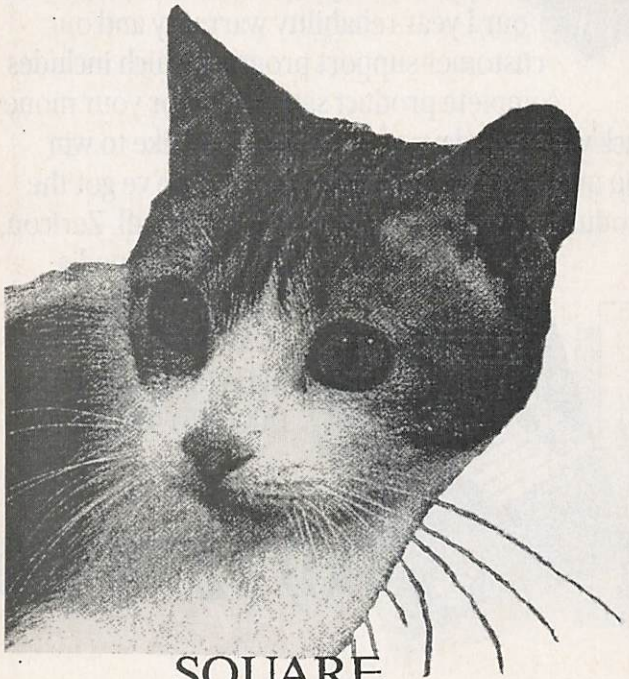
Career Fair Coordinators is sponsoring a career fair at the Infomart in Dallas, Texas, on January 15–16. The fair is for data processing, engineering, and telecommunications professionals who want to meet representatives from companies in the Southwest. The fair sponsor reports that if you can't attend, you can send in a résumé.
Contact: Career Fair Coordinators, Inc., P.O. Box 1381, Coppell, TX 75019, (214) 462-8807.

Technology Conference Nanobytes

The American Society of Landscape Architects will hold its annual convention in Orlando's Orange County Convention/Civic Center on November 18–21. The show is not solely dedicated to computer exhibitions, but companies like AutoDesk, LandCADD, and New Image will be there, according to ASLA.
Price: Members, $330; nonmembers, $405.
Contact: American Society of Landscape Architects, 4401 Connecticut Ave. NW, Washington, DC 20008, (202) 686-2752.

If you miss the ASLA convention, a similar show will be held in Orlando on November 26–30. GIS/LIS '89 will take place at the Marriott Orlando World Center. It will feature technical sessions and exhibitions on land information systems, geographic information systems, energy mapping, and automated mapping/facilities management.
Price: Before November 3: members, $185; nonmembers,

continued



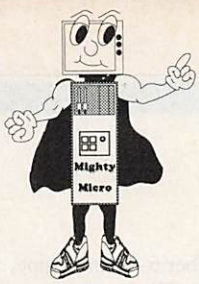
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Simon (the cat pictured at left) is here to demonstrate the quality of the Square Field SF32 image scanner. He was scanned at 300dpi with 16 levels of grey. Square Field also offers the SF42 (400dpi/16 grey) and the SG80 (300dpi/256 grey) for people with a variety of needs in desktop publishing or optical character recognition.

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FX 850 264 CPS, 54 NLQ	339
FX 1050 264 CPS, 54 NLQ	429
LQ 510 225 CPS, 75 NLQ	319
LQ 850 330 CPS, 88 NLQ	509
LQ 950 330 CPS, 88 NLQ	519
LQ 1050 330 CPS, 88NLQ	709
LQ 2550 400 CPS, 108 NLQ	899

OKIDATA

182 Plus 180 CPS, 30 NLQ	229
320/321 300 CPS, 62 NLQ	329/459
390 270 CPS, 90 NLQ	459
391 270 CPS, 90 NLQ	639
393 450 CPS, 120 NLQ	975

TOSHIBA

321 SL 216 CPS, 72 NLQ	439
351 SX 350 CPS, 100 NLQ	922
341 SL 216 CPS, 72 NLQ	589
311 EXPRESS	379
Page Laser 12	2595

NEC

2200 170 CPS, 55 NLQ	319
5200 265 CPS, 90 NLQ	505
5300 265 CPS, 90 NLQ	669
LC890	3195

PANASONIC

1124 160 CPS, 53 NLQ	319
1180 192 CPS, 38 NLQ	185
1191 240 CPS, 48 NLQ	229
1524 240 CPS, 80 NLQ	539
1595 290 CPS, 51 NLQ	449
3131 17 CPS	315
Laser KX4450	1359

HEWLETT-PACKARD

Laser Series II	1689
Laser II D	2895
Desk Jet/Desk Jet Plus	595/725
Pacific Data 1 mb/2 mb	285-435
Pacific Data 25-N-1	269
Pacific Page	439
Intel Visual Edge	449
Plotter in a Cartridge	229
Headlines in a cartridge	249

CANON

Bubble Jet 130	699
LPB8 III	1795

Network

Novell Advanced Netware V. 2.15	$1650
Novell SFT Netware V. 2.15	2499
Novell EIS Level I 4 User	419
Novell EIS Level II 8 User	929
NE 1000 Ethernet Workstation Bd	169
NE 2000	199
ARC Net PC130	119
ARC Net PC 220	149
ARC Net Active Hib/Passive Hub	215/69
Western Digital Ethernet Card	235

Input Devices

Microsoft Mouse w/windows	$135
Microsoft Mouse w/PC paint brush	109
Mousesystems Mouse	89
Logitech Series 9 Serial	69
Logitech Series 9 Bus	79
Logitech Scan Man	169
Summasketch 12x12	369
Summasketch 12x18	599
Kurta 12x12	325

Software

Lotus 1-2-3 ver. 2.01	$299
Lotus 1-2-3 Ver. 3.0/2.2	329
Lotus Symphony ver. 2.0	419
D Base IV ver. 1.0	445
Multimate Advantage II	269
Framework III	439
Paradox ver. 3.0	429
Enable o/a	409
Foxbase Plus single user ver. 2.10	189
Microsoft Work Ver. 5.0	209
Microsoft PC Excel ver. 2.1	239
Clipper	409
Peachtree II	149
Harvard Graphics ver. 2.12	265
Professional Write ver. 2.1	129
Professional File ver. 2.0	169
Q & A ver. 3.0	219
Wordperfect ver. 5.0	215
Wordstar ver. 5.5	189
Wordstar 2K Plus Rel. 3	269
Clarion Pro Developer	385

Modems

Everex 1200 int.	$69
Everex 2400 int/ext.	129/169
Hayes 1200B/2400B Hardware Only	249/389
Hayes 1200/2400 ext.	279/419
Practical Peripherals half card 2400 w/Procomm	129
US Robotics 2400/9600	139/619
Supra Modem 2400 int/ext.	89/109

Fax

Panasonic FXBM 89	$625
Toshiba 30/100	839
Toshiba 3300	1025
Toshiba 3700 EN	1189

Monitors

NEC

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Multisync III D	659
Multisync XL 19"	2080
Multisync 4D/5D	1150/2350

CTX

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AST Premium 386 Model 300C 20 mhz, 1.2 floppy, 1 mg, DOS keyboard . $2650

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Compaq III 20 mb/40mb	3495/4069
Compaq 386-S model 1/20/40	2350/2595/2999
Compaq 386-25 110/300	7195/9199
Compaq SLT w/20 mb	3850
Compaq SLT w/40 mb	4250

IBM

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Model 30 286 w/20 mb	$1950
Model 50-30/60	2499/2739
Model 55 SX 30/60	2829/3119
Model 70 Portable 60/120	5589/6029
Model 70 - 60/120	3899/5899
Model 80 - 40/70	4579/4875
Model 80 - 300	8899

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Toshiba 1000	$639
Toshiba 1200	1849
Toshiba 1200F	1395
Toshiba 3100E	2749
Toshiba 1600	3250
T3200/T5100	3395/4239
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Zenith Super Sport 20 mb	2299
Zenith Super Sport 286 20 mb	3025
NEC Multispeed HD	2275

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Genoa 5100	179
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Genoa 5400	259
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Orchid Pro Designer w/256K	229
Orchid Pro Designer + w/512K	309
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Pacific Rim ext 1.2 IBM 30/286	209
Teac 5-1/4 360K	69
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Teac 3-1/2 1.44	89
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Bernouli Box 11 5-1/4" 20 mb. int.	955
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Orchid Ramquest 16-32 w/o K	279
Orchid Ramquest XT/AT w/o K	239
Orchid Tiny Turbo 286	195
Orchid Tiny Tubro Extra	249
Orchid Tiny Turbo AT	349
Orchid Ramquest II Z w/o K	169
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AST 5251-11 + Enhanced	529
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AST Rampage 286-2 for Model 50/60	549
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$215. After: $215 and $265, respectively.
Contact: American Congress on Surveying and Mapping, 210 Little Falls St., Falls Church, VA 22046, (703) 241-2446.

ADAPSO, the computer software and services industry association, will hold a conference featuring an overview of current technology trends on November 29–30 at the Innsbrook Resort in Tarpon Springs, Florida. Last year's topics included CASE, groupware, expert systems, and cooperative processing, to name a few.
Price: Members, $495; nonmembers, $595.
Contact: ADAPSO, 1300 North 17th St., Suite 300, Arlington, VA 22209, (703) 522-5055.

The Fifth Aerospace Computer Security Applications Conference will be held at in Tucson, Arizona, on December 4–8.
Price: Members: before November 10, $295; after, $335. Nonmembers: $365 and $405, respectively. Students: $130.
Contact: Diana Akers or Victoria Ashby, Mitre Corp., 7525 Colshire Dr., McLean, VA 22102, (703) 883-5907 or (703) 883-6368.

The latest papers on fiber optics, ICs, sensors, and memories will be presented on December 4–6 at the 1989 International Electron Devices Meeting in Washington, D.C.
Price: Members of sponsoring societies, $130; nonmembers, $160.
Contact: Reedy Langevin, Courtesy Associates, 655 15th St. NW, Suite 300, Washington, DC 20005, (202) 347-5900.

LANDEX '89, the educational and technical trade show for LAN users and resellers, will be held on December 14–16 at the Hyatt Regency in Dallas. It is sponsored by the Local Area Network Dealers Association.
Price: Members, $75; nonmembers, $100. Exhibitions only, $25.
Contact: LANDA, 360 West Butterfield Rd., Suite 260, Elmhurst, IL 60126, (312) 279-2255.

The Society for Industrial and Applied Mathematics' fourth Conference on Geometric Design will be held on November 6–10 in Tempe, Arizona. The conference will focus on curve and surface design, solid modeling and manufacturing, and computer graphics.
Price: $125.
Contact: SIAM Conference Coordinator, 117 South 17th St., 14th Floor, Philadelphia, PA 19103, (215) 564-2929.

The 1989 Winter Simulation Conference will happen on December 4–6 at the Capitol Hilton Hotel in Washington, D.C.
Price: Society members, $195; nonmembers, $250; students, $30.
Contact: Kenneth J. Musselman, Pritsker Corp., 1305 Cumberland Ave., P.O. Box 2413, West Lafayette, IN 47906, (317) 463-5557.

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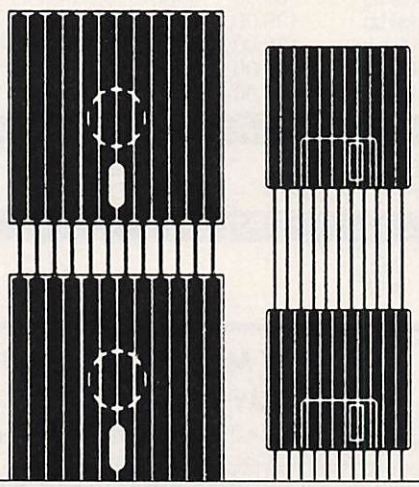
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An Ethernet/VT100 Interface in Your Monitor

The LANTerm Model E (for Ethernet) is a smart diskless workstation that includes VT100 terminal emulation and features an 8-MHz V40 microprocessor.

It comes ready to boot itself on your Novell network through a built-in, thick coaxial, multiaccess unit, the company says, although you can use it with other Ethernet-compatible operating systems.

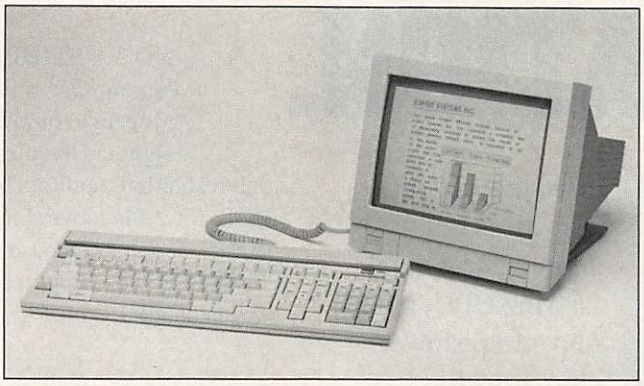
Features include 768K bytes of RAM, a 64K-byte EPROM in the white-phosphor 14-inch monitor, and an AT-style keyboard.

In PC mode, you get HGA graphics and Monochrome Display Adapter text. There's also a serial port and a parallel port.

Price: $1195.

Contact: Esprit Systems, Inc., 2115 Ringwood Ave., San Jose, CA 95131, (408) 954-9900.

Inquiry 994.



Esprit's VT100 terminal emulation with local DOS and LAN capability doesn't force you to make a choice between dumb terminals and networks.

Security System for Stand-Alone PCs

Hands Off the Program is a security utility that protects your hard disk drive, subdirectories, and files by preventing unauthorized persons from booting off the hard disk drive, using the DOS FORMAT command, and other DOS file-based access. The program also automatically locks the hard disk drive when someone boots the PC from drive A.

The program establishes a security system for up to 64 subdirectories. Each user receives a security rating between 0 and 8. Access to a private subdirectory is allowed only if you have a higher number than the private subdirectory. You can also designate important system files as read-only, or hidden, and no DOS command or utility can change the file attribute, according to Systems Consulting, the utility's developer.

Other features include an automatic or manual keyboard lock. In automatic mode, the program will freeze your keyboard after a set period of inactivity; only by entering the correct password can you regain control.

Hands Off the Program works on the IBM PC with DOS 3.0 or higher and uses about 7K bytes of RAM. The company reports that it is developing a new Toolbox program that will let you run Hands Off on a network.

Price: $89.95.

Contact: Systems Consulting, Inc., P.O. Box 111209, Pittsburgh, PA 15238, (412) 963-1624.

Inquiry 996.

Meet Marvin, the Scanning Assistant

Scanning text and graphics from documents is becoming much more commonplace with lower-cost and higher-quality scanners.

Marvin is a Windows-based utility that offers a user interface, database functions, and compression techniques to assist you in processing scanned text and graphics.

Marvin also lets you save documents in a variety of formats, including TIFF and CCITT, so you can pop documents into your scanner and send them out as faxes.

Upcoming products from ImageTech include Marvinet and Marvin Jr. Marvinet runs on Novell networks, supports 25 hand-held and desktop scanners, and exports and imports PC Paintbrush, Dr. Halo, and TIFF files, according to the company. Marvin Jr. is a single-user version of Marvin, intended for laptop users.

Marvin works with all 80286-based IBM PCs and higher and requires a document processing card or 2 megabytes of memory, EGA or VGA, and 640K bytes of RAM. A mouse is also recommended. Marvin Jr. will work with floppy-disk-drive-only systems and will also require 640K bytes. Marvin Jr. is scheduled for release in the first quarter of 1990.

Price: Marvin: $1995. Marvinet: 5-user, $9500; 10-user, $16,500; 20-user, $27,500. Marvin Jr.: price not set.

Contact: ImageTech, Inc., 1864 Northwood Dr., Troy, MI 48084, (800) 451-7566.

Inquiry 998.

Accelerate AutoCAD on the PS/2s

Panacea's DLD-8514/A for AutoCAD transparently replaces the 8514/A driver that's included with AutoCAD release 10, resulting in a performance increase of up to 15 times in redrawing, panning, and zooming, the company reports. The DLD-8514/A supports IBM's 8514/A graphics adapter at the register level and will work with any hardware that's 100 percent compatible with the 8514/A.

The DLD-8514/A also has built-in support for AutoShade and AutoSketch.

Price: $149.

Contact: Panacea, Inc., Londonderry Sq., Suite 305, 50 Nashua Rd., Londonderry, NH 03053, (603) 437-5022.

Inquiry 997.

Take a Shortcut Through the Mac

Aladdin Systems' Shortcut is for Macintosh users who want to navigate more quickly among frequently used folders, find documents and folders, and decompress documents within StuffIt archives.

The utility will also tell you how much free disk space you have, and it lets you rename, delete, and lock files or folders without requiring you to leave the application.

ShortCut runs on the Mac Plus or higher.

Price: $79.95.

Contact: Aladdin Systems, Inc., 217 East 86th St., Suite 153, New York, NY 10028, (212) 410-3080.

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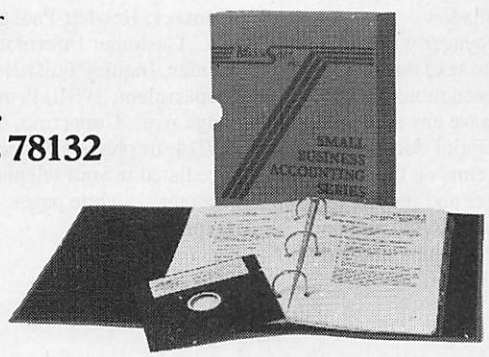
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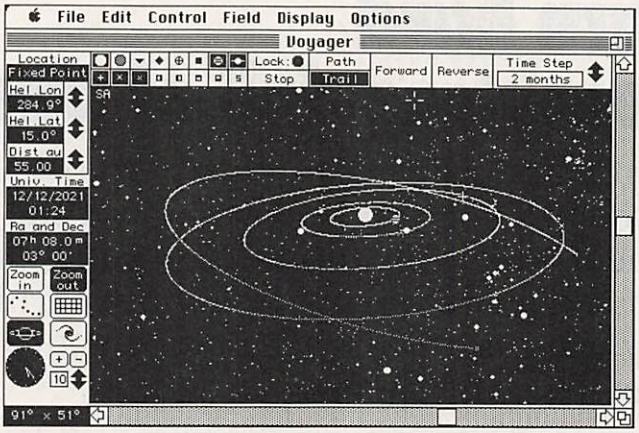
Explore the Universe on Your Macintosh Desktop

Carina Software calls Voyager 1.2 a "desktop planetarium" because it recreates the features of a planetarium on the screen of your Macintosh. With the program, you can view the sky of the past, present, and future; simulate the motion of the planets; or travel across the solar system.

Voyager gives you three views of the sky. The Star Atlas View lets you explore the heavens from pole to pole, using your screen as a window into a large star atlas. Local View displays the sky and horizon from an earthbound location of your choice. It changes with the passage of time and the seasons. Finally, the Celestial Sphere View displays an entire hemisphere of the sky.

Written in MacForth and assembly language, Voyager is the fastest commercial astronomy program available, its maker claims. At its heart is a database of some 14,000 objects, including the 9100 stars in the Yale Bright Star Catalog, 3000 deep sky objects, 88 constellations, 1600 binary stars, and 160 variable stars. A real-time rotating earth will show a solar eclipse path across the surface of the earth, and lunar eclipses can be shown with the moon passing through the earth's shadow.

The Voyager window is resizable, to take advantage of large-screen monitors, and you can save any screen display as a MacPaint document. Voyager runs on the Mac Plus and higher and requires 1 megabyte of RAM and one 800K-byte floppy disk drive.
Price: $124.50.



Pluto and the outer planets from 55 astronomical units as displayed by Voyager 1.2.

Contact: Carina Software, 830 Williams St., San Leandro, CA 94577, (415) 352-7328.
Inquiry 1003.

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You and seven colleagues can simultaneously use any of Hewlett-Packard's CD-ROM information products through a Microsoft or Hewlett-Packard OfficeShare network with the HP LaserROM/LAN.

It includes a 5¼-inch-form-factor, half-height, CD-ROM drive and Microsoft Extensions software. The drive attaches like any other peripheral device. The retrieval software must reside both at the server and at each networked PC.
Price: HP 3000 version, $3935; HP 9000 version, $3335.
Contact: Hewlett-Packard Co., Customer Information Center, Inquiry Fulfillment Department, 19310 Pruneridge Ave., Cupertino, CA 95014, or phone HP sales office listed in your telephone directory's white pages.
Inquiry 1005.

Stop Squinting at Phone Lists

Complementary Solutions developed TeleMate-Phone Book for companies that have a computer on most desktops but still distribute phone lists the old-fashioned way—on a computer printout that's often outdated by the time it reaches your desk. TeleMate-Phone Book lets you put a phone directory on your PC or network that you can pop up in an application when you need to call someone in your company.

TeleMate-Phone Book lets anyone in a company access the phone list. However, only the system administrator can make changes to it, preventing unauthorized edits. The program provides fields for name, job title, extension, department, division, cost center, company, and mailing address. Other fields are provided for alternate phone numbers and comments.

You distribute the inquiry disk on your LAN or, if your office isn't networked, via disk. The inquiry disk automatically updates only those numbers that have changed since the last update. The program can search by partial name, extension, and department.

TeleMate-Phone Book is a TSR program that needs 30K bytes of RAM on your IBM PC with a hard disk drive and DOS 3.0 or higher. The administrator module needs 340K bytes of free RAM. TeleMate-Phone Book is compatible with any DOS-compatible network and comes in two versions: a site license and a single version for a switchboard operator.
Price: Single-user version, $299; site license, $799.
Contact: Complementary Solutions, Inc., 4470 Chamblee-Dunwoody Rd., Suite 202, Atlanta, GA 30338, (404) 454-8033.
Inquiry 1007.

Banyan Makes VINES/386 MCA-Compatible

A new version of VINES/386, which includes Unix under the VINES 3.10 network operating system, lets you use Micro Channel–based systems as file servers. Banyan simply added Micro Channel architecture device drivers.

The immediate technical advantage of VINES/386 on MCA is better 16-Mbps Token Ring performance than is possible by using IBM PC ATs with 16-Mbps Token Ring hardware, Banyan says. VINES/386 for ATs (as well as the version for Banyan's proprietary file-server hardware) already takes advantage of 32-bit central processing *and* 32-bit memory addressing—something only NetWare/386 can do.
Price: $4995.
Contact: Banyan Systems, Inc., 115 Flanders Rd., Westborough, MA 01581, (508) 898-1000.
Inquiry 1006.

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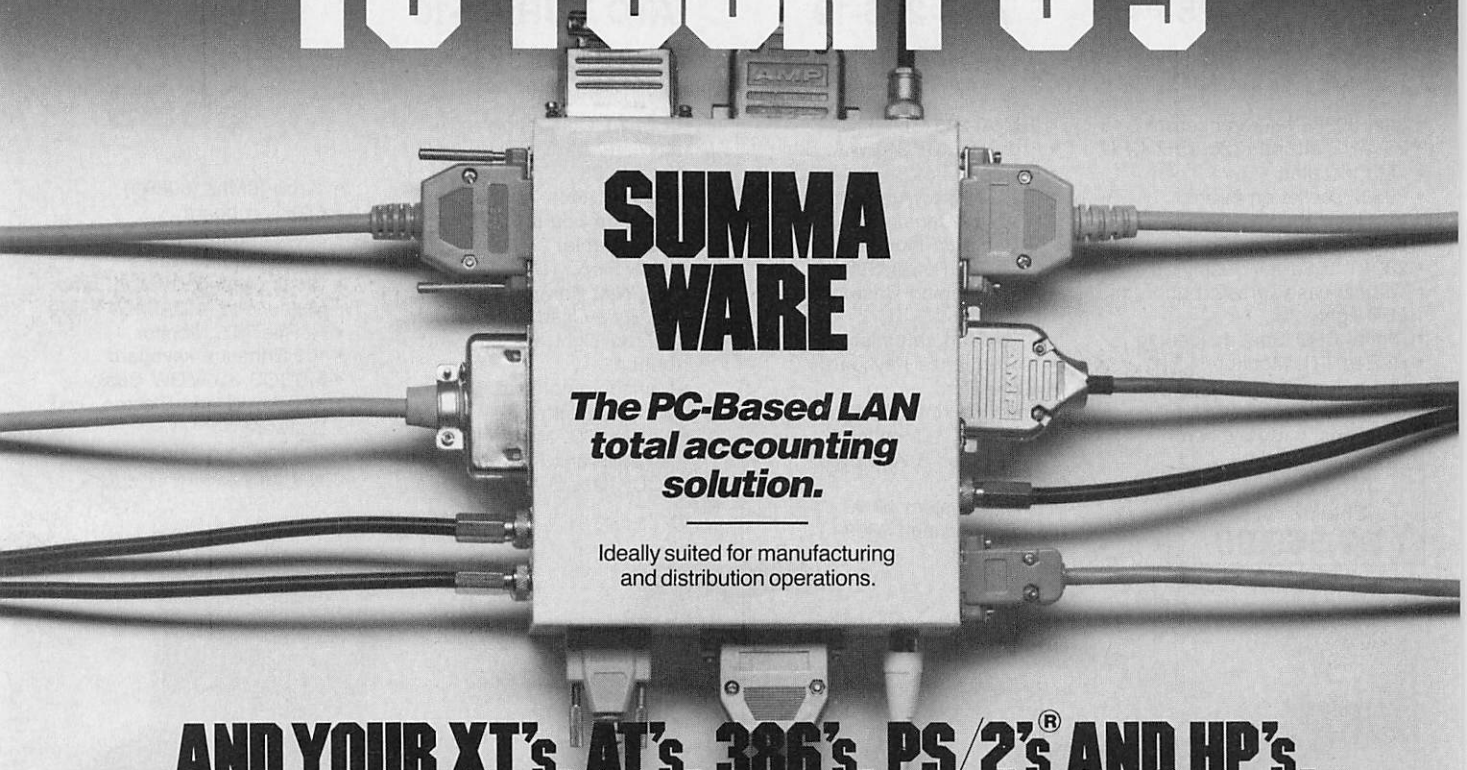
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SHORT TAKES

BYTE editors' hands-on views of new and developing products

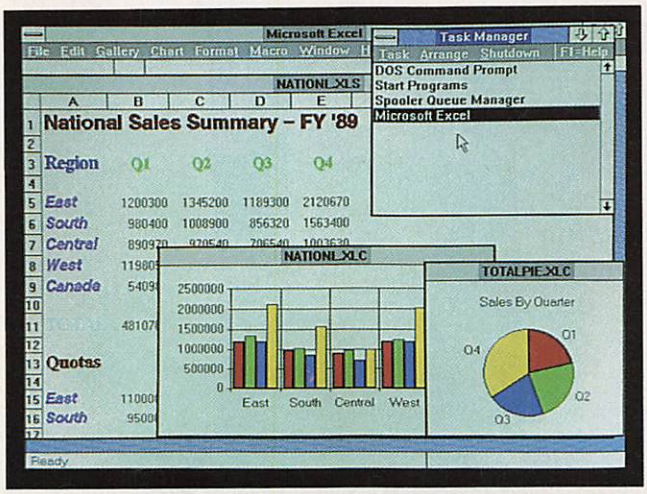
Excel for OS/2 with Presentation Manager

Cornerstone SinglePage XL

Prograph 1.2

TekColor for the Macintosh

FormWorx System 2



OS/2 Gets a Spreadsheet

The new Excel, an upgrade to the powerful spreadsheet, joins the OS/2 bandwagon. After testing a prerelease version, I came to the conclusion that **Excel for OS/2 with Presentation Manager** is distinguished from its DOS ancestor less by its feature set than by the underlying benefits of OS/2.

Among those benefits are large memory addressing, support for virtual memory, built-in Dynamic Data Exchange (DDE), multitasking, and a richer graphical environment, including more fonts, more accurate screen representation, and an IBM common-user-access-compliant interface. Large memory permits a different working style, in which many spreadsheets are loaded and open at the same time. With multitasking, you can be sorting a database and printing a file in the background while working on Excel in the foreground.

However, operating in single-user mode on an AT-class machine, and without many other PM applications with which to share data, the advantages of OS/2 are not immediately apparent. In fact, even the larger memory addressing (I had 3 megabytes installed, plus room on my disk for virtual memory) didn't prevent me from getting warning messages that some of my operations were too big and would require giving up Undo in order to proceed.

Excel for Windows is a fine application, distinguished by its graphical power and, through Windows, its ability to link spreadsheets to one another and to other documents. The PM version carries on this tradition, adding support for up to 256 fonts (in both a faster, less-accurate screen mode and a slower but more WYSIWYG representation) and a new Data Consolidate feature that emulates the three-dimensional capabilities that are found in competing spreadsheets.

The new Excel doesn't permit a single file to contain multiple worksheets, as does Lotus 1-2-3 release 3.0. However, with Data Consolidate, you can "summarize" worksheets by pointing and clicking on areas in each sheet that are then dynamically linked to a summary sheet. To my disappointment, this feature was not intuitive nor well documented.

Other additions in Excel PM are quite minor. A nice menu item called Window Show Clipboard lets you see the contents of the clipboard, and modifications to existing commands permit greater customization of the work environment. New commands necessary to interact with OS/2 (e.g., a menu item to call the Control Task Manager) have been added, while several macro functions have been modified to comply with PM. The file load and save commands will support the 32-character filenames in OS/2 1.2. And Q+E, Microsoft's new SQL querying tool for Excel, will ship with every copy of the PM version.

In performance, the beta version of Excel PM that I tested was comparable to the Windows version in recalculations—sometimes faster, sometimes slower, but never by more than 10 percent—but its speed was substantially slower in two key areas: file loading and saving, and screen movement. Loading a 600K-byte file under OS/2 took 70 percent longer than under Windows, and a test of scrolling right took 31 percent longer. In all comparable benchmarks, Excel PM was much slower than the 2.x DOS versions of Lotus 1-2-3 (using the same files converted to .XLS format) and was a little slower than Lotus 1-2-3 release 3.0.

Is Excel PM worth it for DOS/Windows users looking to upgrade? When you consider that you will need an 80286 machine or higher (an 80386 really helps), at least 2.5 megabytes of RAM, a large hard disk drive with 12 megabytes of free space, OS/2, and the application itself, the cost may not be justified now. But when OS/2 becomes a standard, and more applications that use multitasking and DDE enter the market, this new Excel will likely be a must-have program. □

—Andrew Reinhardt

continued

THE FACTS

Excel for OS/2 with Presentation Manager
$495; upgrade from Windows, $50

Requirements:
IBM PC AT, 80286, PS/2, or compatible with 2.5 megabytes of RAM, OS/2 1.1 Standard Edition or higher, a hard disk drive with 3 megabytes free (not including the space used for OS/2), and EGA or VGA graphics.

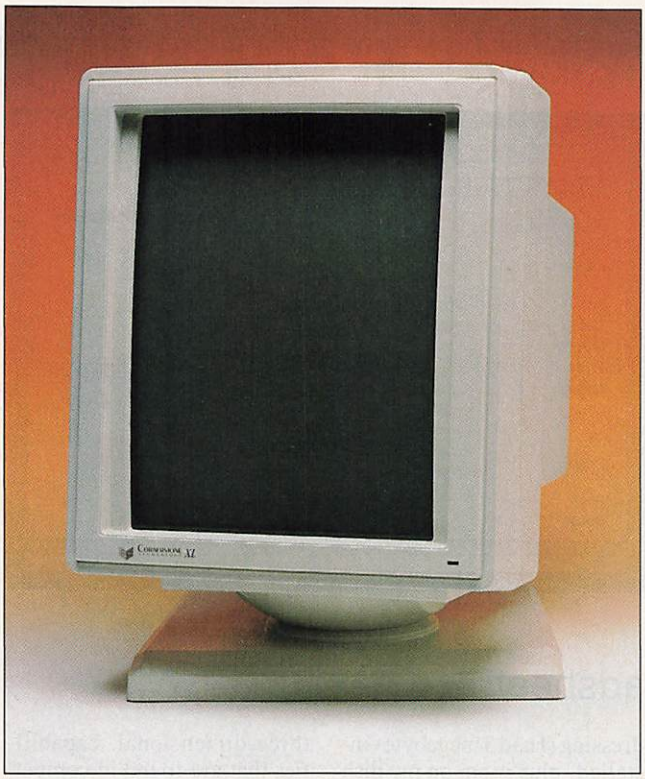
Microsoft Corp.
16011 Northeast 36th Way
P.O. Box 97017
Redmond, WA 98073
(206) 882-8080
Inquiry 988.

A Cornerstone for Building Documents

After writing for years about the advent, and finally the arrival, of the new age of desktop publishing, it was time to install a DTP program of my very own. But my old-faithful IBM PC AT clone was slow, lacked sufficient memory, and had a tiny amber monitor—definitely not suited for the rigors of Windows/286 or PageMaker. The solution to that problem was to increase speed with a new motherboard, beef up the memory with an expanded memory board, and add a full-page monitor.

I chose the **Cornerstone SinglePage XL** subsystem, complete with a four-shade gray-scale portrait monitor that measures 15 inches diagonally and includes a Hercules-compatible add-in card and associated software. TrueFonts, Cornerstone's proprietary screen fonts, include Helvetica, Times Roman, Courier, and Symbols. My four-shade system uses smoothing for crisp on-screen characters. However, a less-expensive two-shade monochrome system is also available.

The installation was easy. There's only one jumper on the two-thirds-length add-in card (for single or multiple monitors), which, although it requires an AT, fits into any 8- or 16-bit expansion slot. From there, I just hooked up the video cable and power and turned the computer on.



THE FACTS

Cornerstone SinglePage XL
$1295 for two-shade monochrome version; $1495 for four-shade gray-scale version

Basic system:
A 15-inch monitor, video interface, video cable, 110-V AC power cord, display drivers, and gray-scale fonts (on gray-scale monitor only).

Cornerstone Technology
1883 Ringwood Ave.
San Jose, CA 95131
(408) 453-9800
Inquiry 990.

Software installation is also uncomplicated. Drivers are included for Microsoft Windows, GEM/3, Ventura Publisher, AutoCAD, AutoSketch, AutoShade, Lotus 1-2-3, Symphony, WordPerfect, and WordStar. A DOS driver allows other DOS applications to run in full-page mode. But because many programs bypass the BIOS and write directly to the screen, don't expect wonders. For example, Norton Commander and XyWrite refused to run in anything but their normal 25-line configuration.

After I finished installing Windows/286, its custom driver, and PageMaker, I was eager to see how a full page looked on-screen, and I wasn't disappointed. The screen surface is flat, with no obvious glare or distortion, and the noninterlaced resolution (768 pixels horizontally by 1008 pixels vertically) more than meets my DTP needs.

Cornerstone is an apt name for this monitor. It measures 16½ inches high and 12 7/10 inches wide, with a depth of 13 7/10 inches. It looks great on my desk and has attracted the curiosity of many (jealous) fellow editors. The only small complaint I have about the SinglePage XL is the contrast, which I haven't been able to adjust to my liking. But that's something I can live with, and I realize it's not completely the fault of the monitor, since it's competing with the extensive light in my office.

If you need to work with text and graphics, as in DTP, and can do without color, the Cornerstone SinglePage XL is for you. □

—Anne Fischer Lent

Pictorial Programming on the Mac

Prograph 1.2 from Gunakara Sun Systems is a pictorial development system that radically changes the rules of the game. You build Prographs with a pictorial diagram editor similar to what many computer-aided software engineering tools provide. However, while CASE diagrams typically specify code, Prographs *are* code.

An application builder, an interpreter, and a debugger support the pictorial language. The key elements of Prograph are object orientation, data flow, and a well-integrated environment. The object orientation is, in some respects, not too different from what you find in C++ or Object Pascal.

Class icons have left and right mouse-sensitive regions. Double-click on the left one, and an object editor reveals attributes that belong to the class at large and to the current instance of the class. Double-click on the right one, and another editor shows the methods in the class. The System Classes window is where you create new classes and—by rubber-banding them to existing ones—specify inheritance relationships.

There's virtually nothing in the system that corresponds to the normal concept of a variable. Thus, there are no variable names to invent, type, and misspell. It also means, however, that you'll spend much time in object editors unpacking attributes—since that's the

continued



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THE FACTS

Prograph 1.2
$195

Requirements:
Mac Plus with 1 megabyte of RAM.

Gunakara Sun Systems Ltd.
1127 Barrington St., Suite 19
Halifax, Nova Scotia
Canada B3H 2P8
(902) 429-5642
Inquiry 989.

place where the data lives in Prograph.

The flow of data through an application begins with Prograph's transformation of the Macintosh event loop. It packages Mac events as instances of one or another of the System Classes, and these flow as data into the handling methods you've specified in the application builder.

Simple data types include strings, integers, reals, Booleans, and lists. Instances of a class carry the class as their type. There's also the Mac type. Prograph provides direct or indirect hooks to all the Mac internals.

Prograph's application builder works nicely, and the smooth transition from window and menu prototyping to coding is remarkable. The design editor is a joy to use and is wonderfully suited to an incremental style of development. Newly created operations arrive unformed, and you then shape them to your needs.

Prograph works hard to document itself. Class methods and attributes, Prograph primitives, and Mac primitives are documented within the environment. Classes that you create are automatically included here as well. Several HyperCard stacks accompany the system, providing additional detail.

When you're developing in Prograph, you spend a lot of time in the debugger. It animates programs: As control flows into a method, a method execution window opens, and you can step through its operations, inspecting the data on terminals and roots. When control flows into a method (which is the Prograph equivalent of a function call), another method execution window opens, and the process continues. I ran into a few problems getting all this to work properly—particularly when switching between development and execution modes—but these were known bugs in the beta release I was reviewing, and they will undoubtedly be fixed in the final version.

Gunakara Sun Systems is working on a Prograph compiler that will be included in the next version. Assuming that the compiler works efficiently, this should place Prograph in direct competition with more traditional development systems.

Prograph's fate then will be determined by how people respond to the unique style it offers. I found the experience both fascinating and frustrating. The language takes much effort to learn, and the dataflow orientation of the system requires an even larger conceptual leap. On the other hand, my experience is with programming with text rather than with pictures, so, learning curve aside, I'd say it's the most fluidly integrated environment I've worked with. □

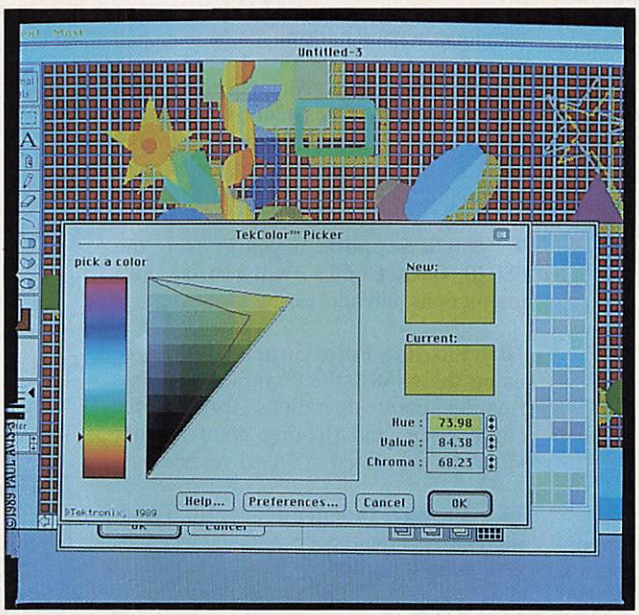
—Jon Udell

TekColor Lets You Really See What You Get

If you own a color printer, chances are you've been disappointed on occasion by the lack of similarity between the screen colors created by your RGB monitor and the output of your color printer. What appeared on-screen to be a violet flower, for example, may appear to be blue on paper. Unfortunately, the colors on your monitor often can't be reproduced exactly by your color output device. CRTs, electronic printers, scanners, and film recorders produce colors from electronic signals based on mathematical models, but devices vary considerably in their ability to produce color.

To solve this problem, Tektronix has introduced its **TekColor for the Macintosh** color-matching system. TekColor is designed to help you pick screen colors that your printer (or other output device) can duplicate. While color-matching systems aren't new, Tektronix says that TekColor is the first device-independent color-matching system to appear on the market.

TekColor will provide color-matching information for most Mac-compatible RGB monitors and any color output device (e.g., printers and film recorders). However, your printer must be compatible with the TekColor color-matching system. Currently, only the Tektronix low-end $2499 ColorQuick ink-jet printer includes the necessary TekColor software, although Tektronix plans to bundle TekColor with its higher-end printers in the coming months.



Included with TekColor is the Picker, a color-selection and color-editing interface that lets you select a "hue leaf" showing a range of shades within a given color set.

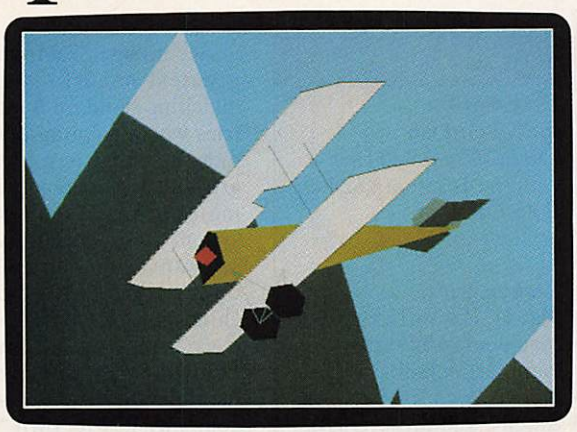
The TekColor interface includes two color boxes. One shows you the original color; the other shows the effects of your color editing. The interface, as you would expect for a Mac application, is intuitive and easy to use. If your monitor can't reach a selected color, TekColor will display the nearest color in the current color box and flag it for you.

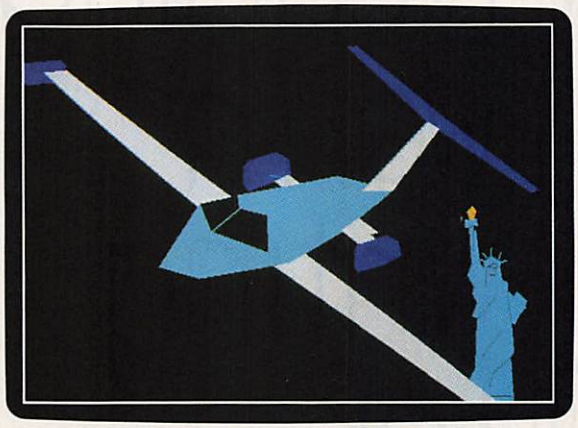
To develop a truly device-independent color model, Tektronix linked its color-matching system with the standards outlined by the CIE (Commission Internationale de l'Eclairage, or International Commission on Illumination).

TekColor is based on the Tektronix TecHVC (for Hue-Value-Chroma) color model. It's designed to accommodate

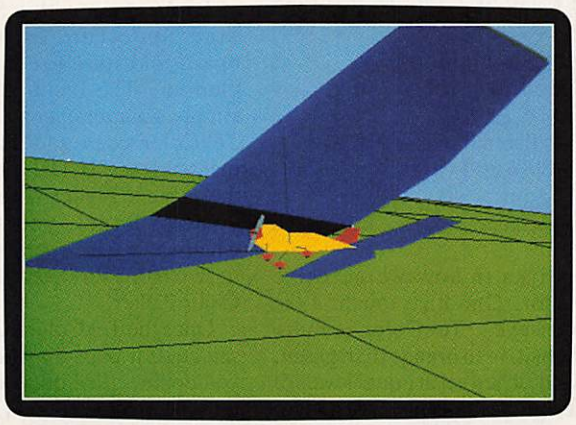
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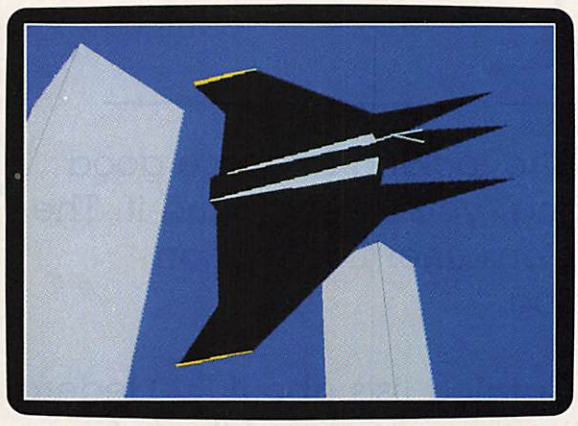




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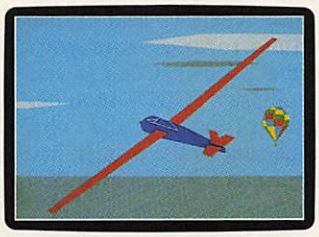


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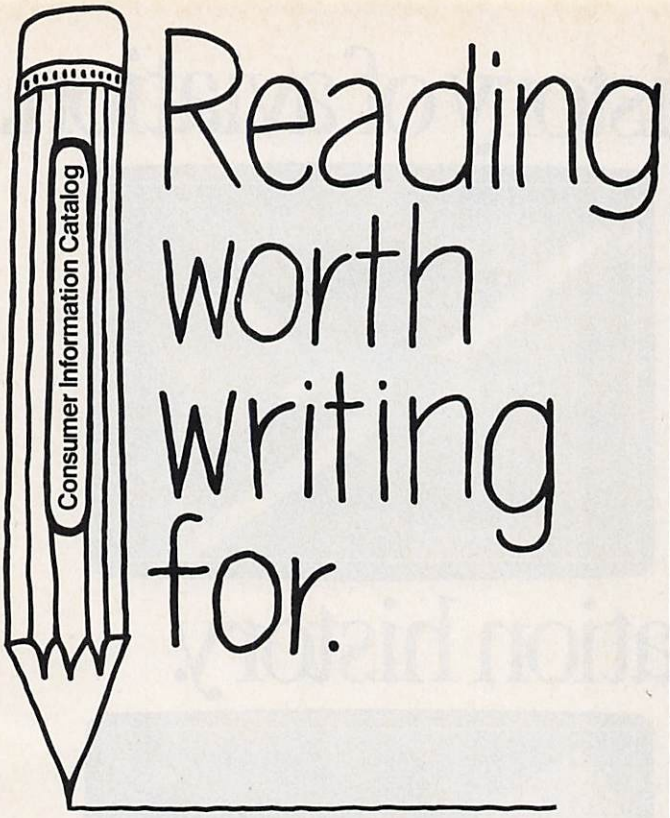
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THE FACTS

TekColor for the Macintosh
$50 (also bundled free with the Tektronix $2499 ColorQuick ink-jet printer)

Requirements:
Mac II, IIx, or IIcx with a Mac-compatible color monitor (including models from E-Machines, Radius, and RasterOps), and a Tektronix ColorQuick ink-jet printer (other Tektronix printers will support it before the end of the year).

Tektronix, Inc.
P.O. Box 1000,
M-S 63-630
Wilsonville, OR 97070
(800) 835-6100.
Inquiry 991.

quirks in how we perceive color. One nice touch: Like our eyes, TekColor is more sensitive to orange than green, and, when set at equal levels of brightness, yellow will appear brighter than blue.

TekColor's set of algorithms creates a three-dimensional color space for a graphics device. This color space outputs and receives RGB values to and from your display monitor and does the same with CMYK (cyan, magenta, yellow, and black) values to and from your printer. The TekColor Device Database (TCDD) includes data to transform the color value sent to the printer into the printer color value that best matches the screen.

According to Tektronix, the greatest need for a color-matching standard is in industries where color hard copy is most essential (e.g., graphic arts and professional publishing). Currently, the TekColor system is supported by Mac software and hardware developers like Aldus, E-Machines, and RasterOps. However, creating a computer industry standard is tricky business these days—every company has its own "standard" it's trying to push.

We tried a beta version of TekColor for the Mac on a Mac II equipped with 5 megabytes of RAM along with a SuperMac Spectrum/24 video board and its 19-inch color monitor. The installation is simply a matter of copying the TekColor cdev and a folder that holds the TCDD files into the System Folder. From the Control Panel, you select whether to use Apple's standard Color Picker or the TekColor Picker.

Once the TekColor Picker is selected, it pops up whenever you double-click on a color to modify it. Two curves, which represent the hue leaves that plot the color range of the printer and monitor, appear. At a glance, you can see if the color you're working with will reproduce properly on the printer. TekColor worked inside PixelPaint 2.0 and PhotoMac 1.1 without problems.

TekColor for the Mac looks like a good product. It's well designed, inexpensive, easy to use, and certainly very helpful if you find color matching essential. □

—Jeffrey Bertolucci and Tom Thompson

FormWorx Goes GUI

Forms-processing packages have simplified the previously painful process of designing and filling out forms. One of the first such packages was FormWorx.

FormWorx System 2 is an impressive package. While the beta version that I tested was lacking some planned final features, it made the process of both laying out and (more important) filling out forms a real pleasure.

While many companies say

continued

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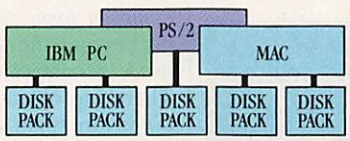
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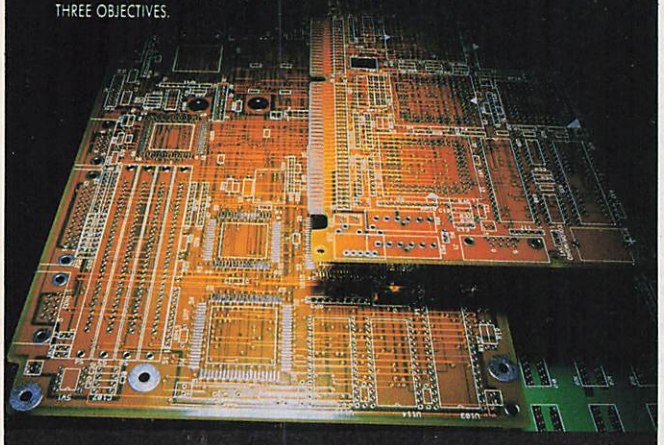
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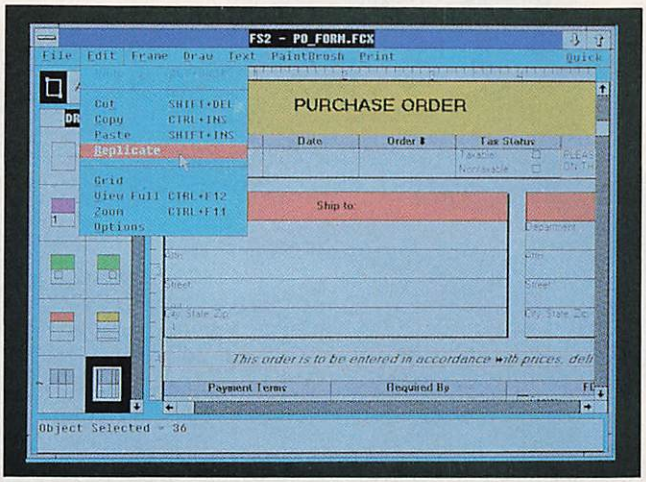
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that they use object-oriented constructs, the reality is often different. With FormWorx System 2, "object-oriented" is more than a buzzword. Objects are the key to the package's surprisingly literate user interface. Laying out a form is simplified because the company has included about a dozen constructs that it calls *common form objects*. These go beyond the simple grids used in competing products. There are objects for all the common form areas (e.g., headers, lists, and signature blocks). I found that I could quickly design a form without the steep learning curve that was needed with other packages I've used.

A form in FormWorx System 2 consists of four planes: draw, edit, paintbrush, and data. This separation of powers makes a great deal of sense, and it's one of the main reasons why the package is so easy to use. After I worked with the individual planes, they all came together in a finished product.

Another stunning feature of the package is its forms-filling abilities. Other forms packages let you import data from dBASE (or delimited ASCII) files, letting you print out a bunch of finished forms at one time. But FormWorx System 2 takes the concept much further. The company has essentially designed an easy-to-use front end to dBASE III Plus (or dBASE IV), and you don't even need dBASE to use it.

But FormWorx System 2's biggest surprise came when I exited the program. Because it stores forms as a combination of pointers to objects, the amount of space needed to store your finished forms is minuscule. For example, a standard invoice file took up only 548 bytes of storage. This is a far cry from other forms packages, which store forms as bit-mapped images, often taking up as much as 300K bytes for a single form.

FormWorx System 2 is a package that shows what careful design coupled with the latest wave of object-oriented programming technology can do for software. And for only $299, it's a software system that delivers even more than it promises. ■

—Stan Miastkowski

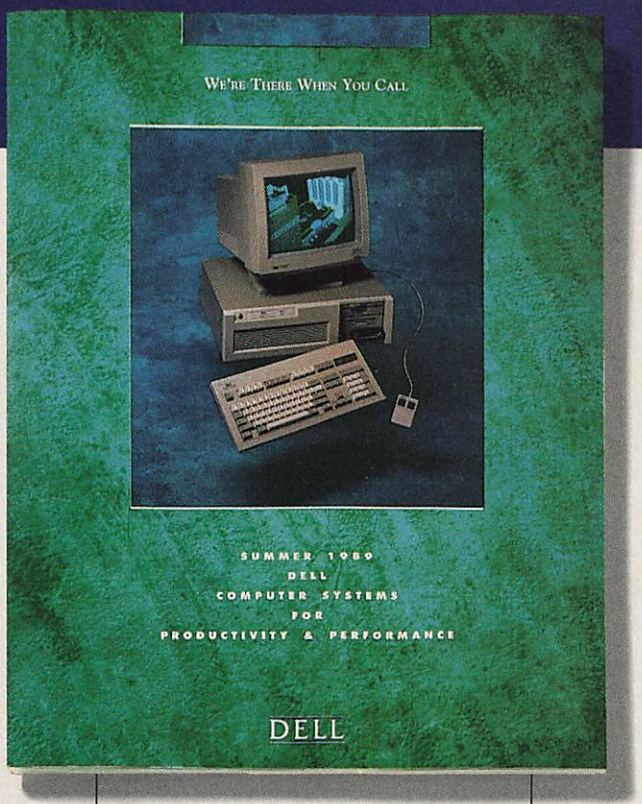
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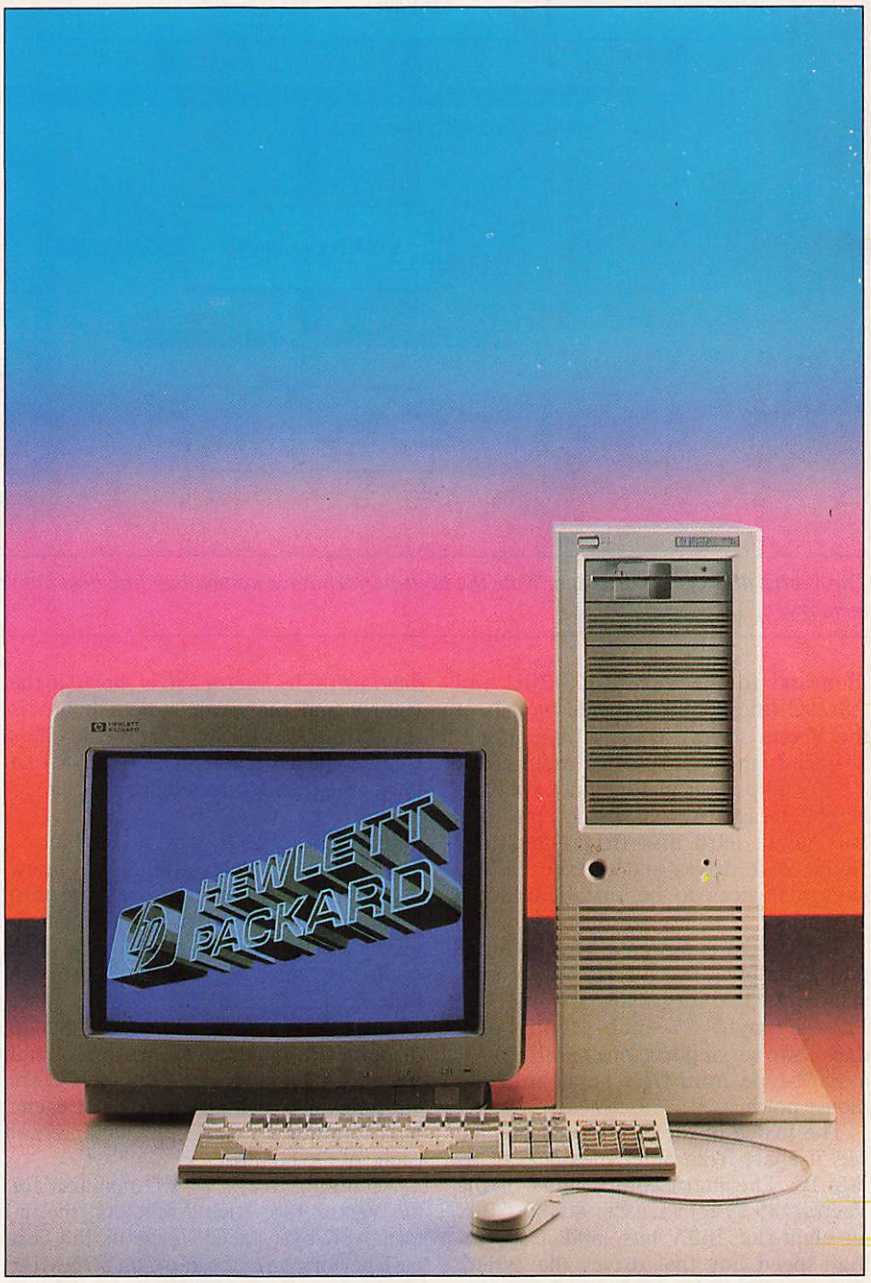
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FIRST IMPRESSIONS ■ Nick Baran

EISA Arrives

HP leaps to the forefront with an 80486-based system built around the controversial EISA bus



After its unsuccessful attempt to take the lead in the PC market with its touchscreen HP-150 back in 1983, Hewlett-Packard settled for the role of builder of solid, reliable PC clones, while leaning heavily on its entrenched positions in the minicomputer and electronic equipment markets. Now, however, the company is embarking on a new strategy of product innovation and market leadership.

On the software side, HP has taken the lead in developing the Unix-based Motif user interface for the Open Software Foundation. It has also started shipping its innovative NewWave user environment for Microsoft Windows.

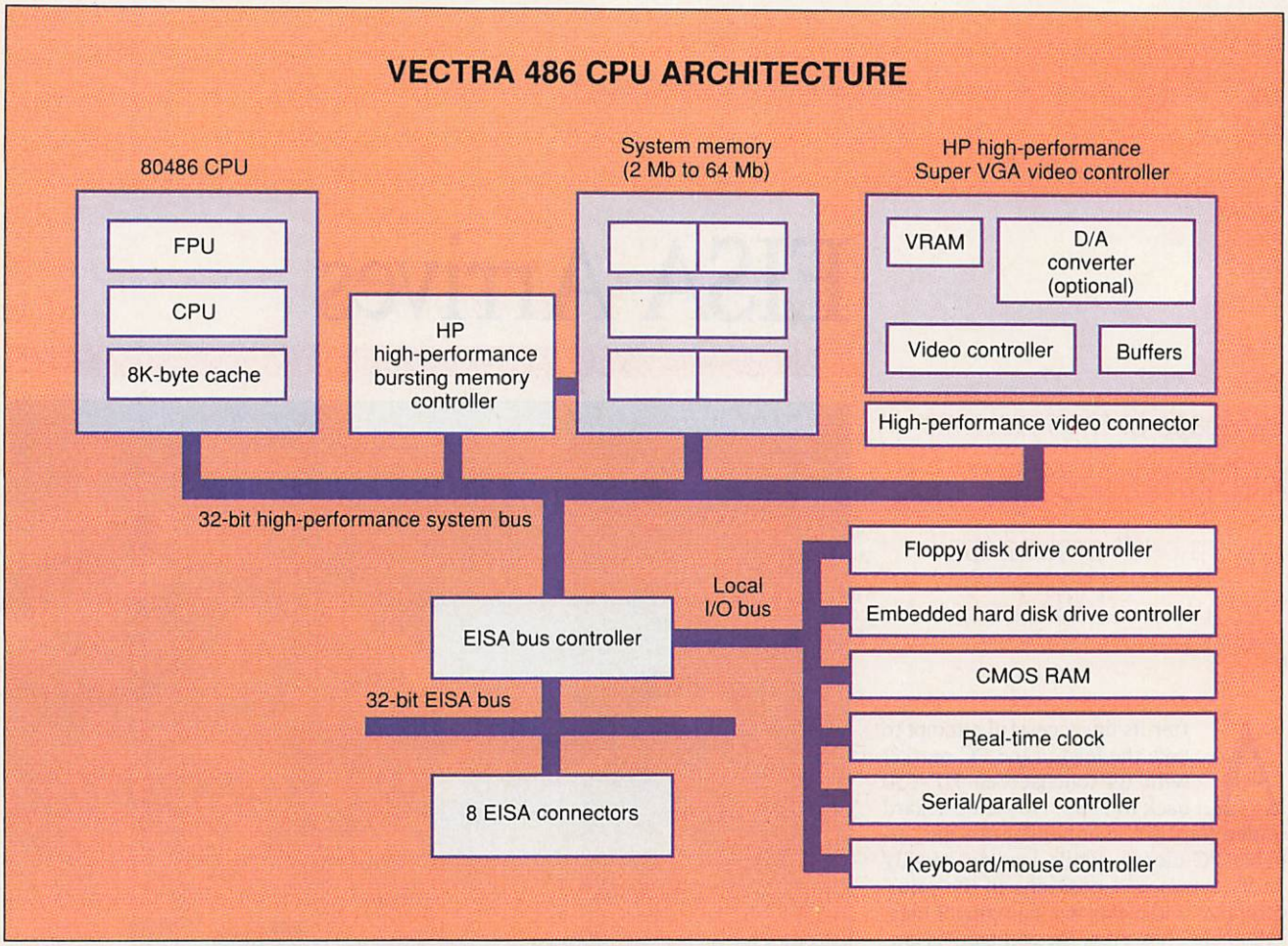
On the hardware side, the first evidence of HP's new strategy is its Vectra 486 PC, a powerful 80486-based deskside system that may be the first machine on the market to feature the long-awaited Extended Industry Standard Architecture bus. (For more details on the EISA bus, see this month's Under the Hood column.)

HP gave BYTE an early look at a preliminary version of the Vectra 486, and it is indeed an impressive machine, offering excellent performance and broad flexibility. The Vectra 486 is equally well suited for use as a high-performance CAD workstation, a network server, or a host for a multiuser system. And, as you'd expect, it can run Unix, DOS, and OS/2.

From the outside, the Vectra 486 looks

continued

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The Vectra 486 system diagram. Note the high-performance system bus (the host bus) that drives the system and video memory.

identical to the Vectra RS/20C and RS/25C (the 80386 deskside models of the Vectra series). The floor-standing, 24-inch-high system cabinet weighs in at a hefty 60 pounds and includes six half-height storage bays, allowing up to two full-height hard disk drives and four floppy disk drives and/or tape backup storage devices to be installed in the system.

The system is powered by a 360-watt power supply. The Vectra 486 comes standard with 2 megabytes of RAM, one 1.2-megabyte 5¼-inch floppy disk drive, two serial ports, one parallel port, a PS/2-type mini-DIN keyboard, and mouse ports.

The inside of the Vectra 486 is what sets it apart from other members of its family. The main components of the Vectra 486 system are the 80486 CPU, an eight-slot EISA bus, and a special high-speed bus that drives the system memory and the high-performance Super VGA video controller. The system diagram of the Vectra 486 is shown in the figure, and the main system board is shown in photo 1. Note that the 80486 is located on a separate CPU board that plugs into the high-speed bus.

The 80486 CPU

The heart of the Vectra 486 is Intel's new 80486 CPU, which features on-chip floating-point and memory management units, as well as an internal 8K-byte cache (for an overview of the 80486, see Microbytes, June BYTE). Unlike some of the other recently announced 80486 machines (e.g., those from Apricot and Advanced Logic Research), the Vectra 486 does not include an external cache but relies entirely on the 8K-byte internal cache of the 80486.

According to HP's R&D manager for the Vectra 486, Rich Archuleta, the internal 8K-byte cache "gave us the best cost/performance trade-off on a 25-MHz system." Archuleta added that a "pretty big" external cache is needed to obtain a significant gain in performance. I'll discuss the performance of the Vectra 486 later in this article.

I should mention that the system board does not include a socket for an auxiliary floating-point coprocessor such as the Weitek 4167, which supports the 80486 and is reportedly much faster than the FPU built into the 80486 (see Microbytes, July BYTE, page 26). According to Archuleta, the system board was already in its final design stages when Weitek announced the 4167; HP will support the 4167 in a later version of the system board.

High-Performance Host Bus

The Vectra 486 uses a custom, 32-bit high-performance system bus, or "host bus," to access system memory as well as HP's Super VGA video controller. The host bus operates synchronously at the clock speed of the CPU, allowing a theoretical data transfer bandwidth of 100 megabytes per second (25 MHz, or mil-

lion cycles per second multiplied by 4 bytes per cycle). Of course, the actual bandwidth is limited by transfer protocols, CPU resets and interrupts, and other performance penalties. But HP claims that the host bus can access system memory with a bandwidth of 50 megabytes per second using the burst mode of the 80486.

The system memory comes on a separate memory board (see photo 2), which plugs into the host bus. HP custom-designed its own memory controller chip that takes advantage of the burst mode of the 80486. System memory is available in 80-nanosecond, 1-megabit single in-line memory modules, allowing a maximum of 32 megabytes of RAM (in 1- or 4-megabyte packages), or in 4-megabit SIMMs (8-megabyte packages), which allows a maximum of 64 megabytes of RAM.

HP's New VGA Controller

As I mentioned earlier, the Vectra 486's host bus supports high-speed access to HP's new Super VGA video controller. The video controller plugs directly into the host bus but also takes up one EISA bus slot (the board extends across one of the EISA slots). The new VGA adapter is actually a "superset" of the VGA standard, supporting resolutions of 800 by 600 pixels and 1024 by 768 pixels, as well as the standard VGA resolution of 640 by 480 pixels. The controller displays 8 bits per pixel for a maximum of 256 simultaneous colors (16 colors in 1024- by 768-pixel mode) and includes 512K bytes of video RAM.

I did not have a chance to see the new video controller because it was still in production at the time of this writing. However, HP's Archuleta told me that it would offer about 10 times the performance of a standard VGA controller. The machine I saw used a standard 16-bit, AT-type VGA board plugged into the EISA bus.

Before moving on to other features of the Vectra 486, I want to point out that the high-speed host bus is a critical component of this system, particularly because of its high-performance graphics capabilities. Unlike the EISA bus—or other I/O buses, for that matter—HP's host bus offers a much faster and more efficient path to the CPU because it does not have to bother with bus arbitration protocols and other performance penalties associated with bus I/O. Thus, the system can support much higher block transfer rates from system and video memory. In high-resolution graphics sys-

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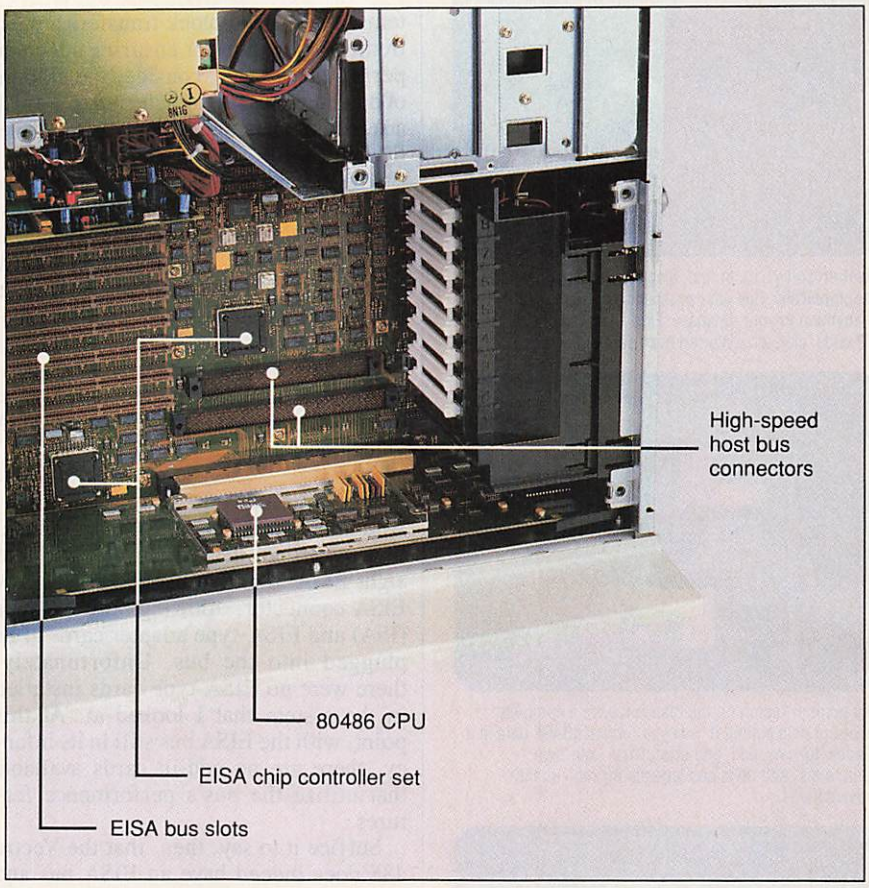


Photo 1: *The main system board of the Vectra 486. Note that the 80486 is located on a separate CPU board that plugs into the high-speed host bus. The two large connectors above the CPU board are host bus interfaces for the memory and Super VGA board. The EISA bus slots are on the left side of the main system board (seven of the eight slots are visible in the photo).*

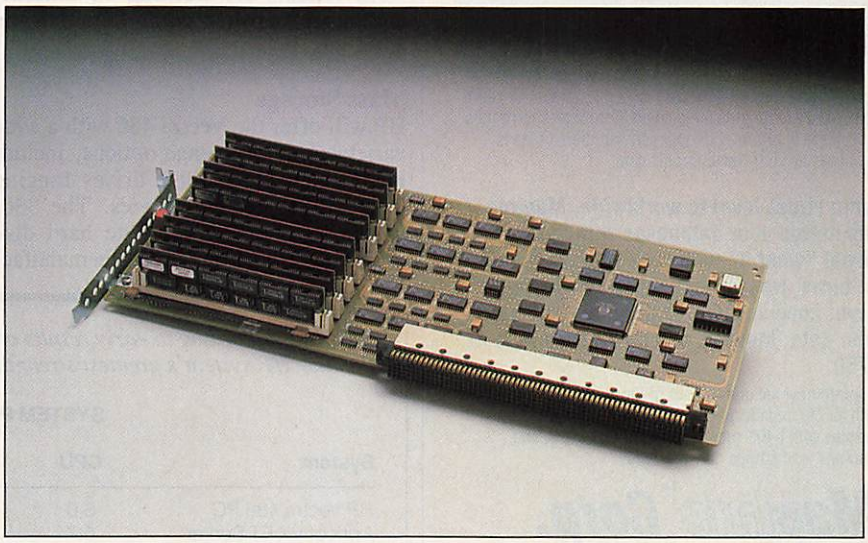


Photo 2: *The Vectra 486 system memory board. Memory can be configured with 1-megabit or 4-megabit single in-line memory modules, allowing up to 64 megabytes of system memory. The large chip on the right side of the memory board is HP's custom memory controller (the bursting memory controller shown in the figure).*

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tems, high-speed block transfers are extremely important for ensuring adequate performance (e.g., consider the amount of data that must be transferred to refresh a screen displaying a 1024- by 768-pixel CAD model).

The Vectra 486 designers claim that the host bus will be able to support sustained block transfer rates of 25 megabytes per second, a performance figure in the class of the graphics engine used in Sun's SPARCStation. In addition, because the host bus is 32 bits wide, high-performance color boards and three-dimensional accelerators are sure to be offered as options instead of the VGA video controller.

The EISA Bus

And then there's the EISA bus. As mentioned earlier, the Vectra 486 includes eight EISA slots that use the double-row EISA connector, allowing both AT-type (ISA) and EISA-type adapter cards to be plugged into the bus. Unfortunately, there were no EISA-type cards installed in the system that I looked at. At this point, with the EISA bus still in its infancy, there are no add-in cards available that utilize the bus's performance features.

Suffice it to say, then, that the Vectra 486 does indeed have an EISA bus and that 32-bit EISA cards will become available for it within the next year. According to HP's product manager, Steve Keilen, HP will offer a high-performance EISA hard disk drive controller board within the next year. And several network vendors are working on Ethernet and other network controllers for the EISA bus.

Mass Storage

HP will offer the Vectra 486 with a wide variety of mass storage options, including a line of hard disk drives ranging from 108 to 670 megabytes. The 330-megabyte and 670-megabyte hard disk drives are brand new and are manufactured by HP. The lower-capacity hard disk drives are available with embedded ESDI controllers that plug directly into the Vectra 486 system board, saving a bus slot. However, an ESDI controller card (AT-type) is also available for running the 330- and 670-megabyte hard disk drives. The ESDI hard disk drive controller features a data transfer rate of 20 megabits per second. The hard disk drives offer an average access time of about 16 milliseconds.

The Vectra 486 system board also includes a built-in floppy disk drive and tape drive controller, which can support up to four tape drives or floppy disk drives. The controller supports 5¼-inch and 3½-inch drive formats, including the HP-150's 710K-byte format.

Performance

I had an opportunity to run BYTE's low-level benchmarks for 80286 machines on a Vectra 486 equipped with 4 megabytes of RAM, the 330-megabyte hard disk drive, and a standard 16-bit VGA board. The results are shown in table 1. It must be emphasized that the machine I tested was a preproduction model using an early version of the 80486 CPU and a beta version of HP's new hard disk drive. According to Archuleta, the performance of the 80486 should improve substantially in its final production version. He also said that HP's hard disk drives will run faster in the final version. And, as I mentioned earlier, I was unable to test the new high-speed VGA controller that will ship with the production version of the machine.

In any case, the Vectra 486 yielded results comparable to those of other 80486-based systems BYTE has tested. The CPU index is somewhat lower than the results for the Apricot because the Vectra does not include an external cache. But the Vectra is faster than IBM's Power Platform 486.

The hard disk and video numbers were

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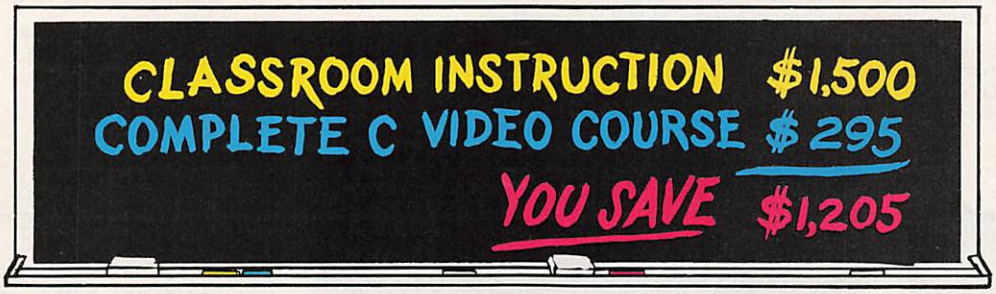
Table 1: *According to early results on BYTE's low-level benchmark tests, the new HP system's greatest strength appears to be its disk performance.*

	SYSTEM PERFORMANCE			
System	**CPU**	**FPU**	**Disk I/O**	**Video**
HP Vectra 486 PC	6.0	21.6	3.4	4.5
Apricot VX FT Server	6.7	21.8	2.3	5.2
IBM Power Platform 486	5.3	21.4	1.8	4.3

Note: Indexes show relative performance. For all indexes, an 8-MHz IBM PC AT = 1. For a full description of all the benchmarks, see "Introducing the New BYTE Benchmarks," June 1988 BYTE.

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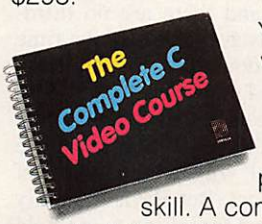
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among the fastest of any of the 80486 systems that we've tested so far. And the video test does not reflect the performance of the high-performance video controller.

A High-End System for High-End Applications

It's probably clear by now that the Vectra 486 is aimed at the high end of the PC market and is actually capable of replacing much-higher-priced minicomputers as a network server or multiuser host. The 32-bit EISA bus opens up possibilities for high-performance networks and hard disk drive controllers, which would make the Vectra 486 ideal for multiuser and network environments. The high-speed host bus and the new VGA controller make the machine an excellent choice as a high-performance CAD and engineering workstation.

But in spite of its promise, the Vectra 486 is a little ahead of its time. As BYTE goes to press, the 80486 is still being tested for bugs and there are no third-party EISA cards available. By the time you read this, I doubt that this situation will have changed much.

In my estimation, it will be the middle of 1990 before the 80486 and EISA are fully operational with a good base of third-party support. But HP is certainly to be congratulated for taking such a bold step with its release of the Vectra 486. With HP's reputation for reliability and strong customer support, the Vectra 486 is sure to be one of the strongest competitors in the Intel-based workstation and high-end PC markets.

At the time of this writing, HP had not finalized prices for the Vectra 486. It was willing to give an approximate price range of about $10,000 for a system with 2 megabytes of RAM and one floppy disk drive, about $15,000 for the same system with a 330-megabyte hard disk drive and the high-performance VGA controller, and about $18,000 for a system with a 670-megabyte hard disk drive and the VGA controller. ■

Nick Baran is the BYTE bureau chief in San Francisco. He can be reached on BIX as "nickbaran."

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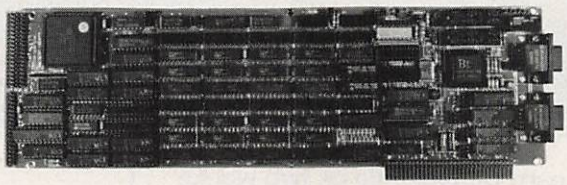
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Cheetah Gold 33:
An Economical Powerhouse

Michael E. Nadeau



Photo 1: *The Cheetah Gold 33. The image on the screen is an AutoCAD rendition of the Cheetah GPX-486 CPU board.*

My first impression of the Cheetah Gold 33 was that it is a well-engineered system that uses top-shelf components. Its designers also added thoughtful extras, such as a detachable wide plastic base and a speed-adjustable cooling fan. In short, it looked like a good $8000 to $10,000 system. Cheetah, however, seems perfectly happy to sell its new 25-MHz 80486 tower computer for $4995.

This is not a "stripper" system. The price includes 4 megabytes of 1-megabyte- by 1-bit-SIMM (single in-line memory module) RAM, a 1.2-megabyte 5¼-inch TEAC floppy disk drive, a 60-megabyte Mitsubishi hard disk drive and Adaptec controller, a Trutec VGA controller, one serial and one parallel port, and a Samsung monochrome VGA monitor. You wonder how Cheetah can sell the system for so little and make a profit.

Several factors are working in Cheetah's favor. Hardware prices, most notably memory prices, have been going down recently, and Cheetah is keeping its profit margin small. The 80486 itself, with its built-in cache and math coprocessor, is actually cheaper than a 33-MHz 80386 with those options added. (See the text box "ALR's Other 80486s: the PowerCache 4 Duo" on page 112 for more information about the 80486 versus the 80386.)

Cheap, But No Slouch

The prototype system we saw had a 106-megabyte Imprimis hard disk drive, an optional DPT SmartCache controller with 4.5 megabytes of RAM, a second 1.44-megabyte 3½-inch floppy disk drive, another serial port, a beta version of Video Seven's 1024i VGA adapter, and a Seiko CM-14 VGA monitor (see photo 1). Cheetah prices this configuration at a modest $8495. The DPT controller dramatically improves disk I/O speed and, consequently, its overall application performance. The BYTE disk I/O index was 9.49, the fastest we've seen, but you pay a hefty premium for that speed.

Since the 80486 CPU in the Cheetah was itself a prototype, the BYTE CPU index of 6.52 should be considered tentative (see table 1). That rating is not the

continued

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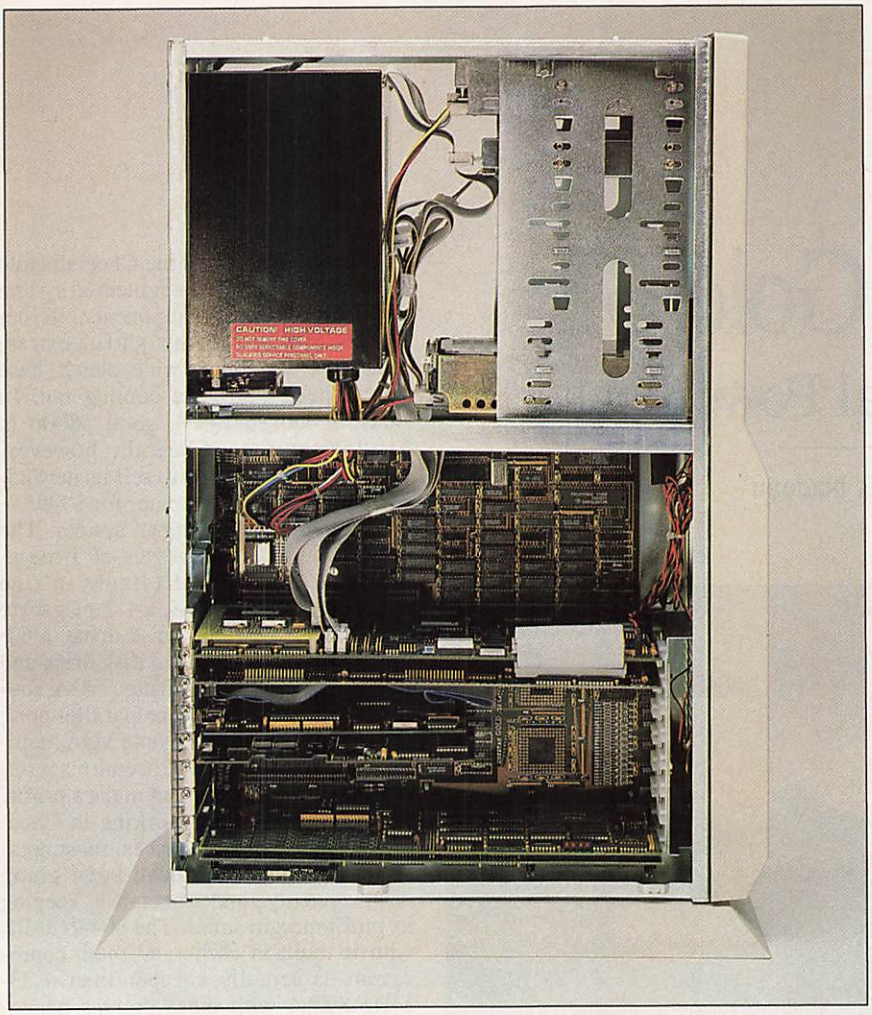


Photo 2: *The inside of the Cheetah Gold 33 reveals a sturdy steel frame, a hefty power supply, and ample room for expansion. Note the detachable base.*

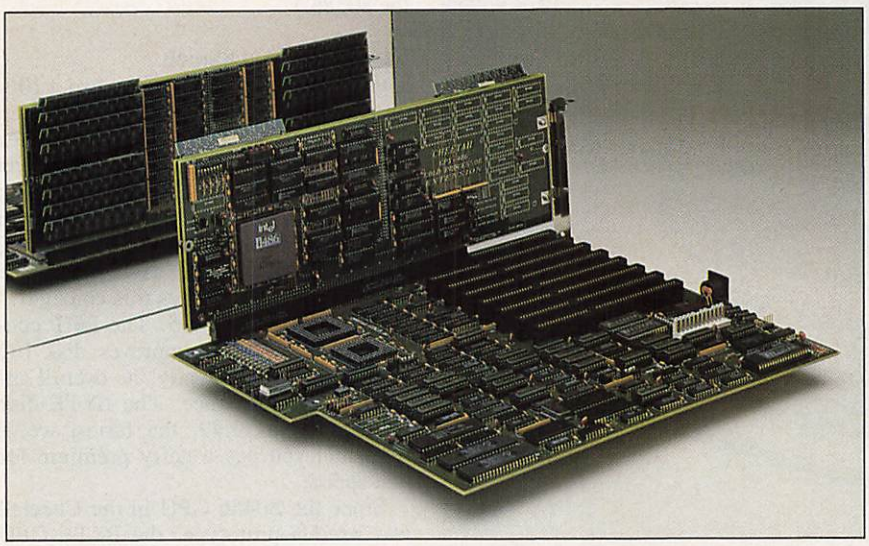


Photo 3: *The GPX-486 CPU board, burst-memory-array memory board, and main system board. The system design supports up to 33-MHz 80386 or 80486 operation.*

fastest—ALR's PowerCache 4 tower system holds that honor—but it is respectable. The BYTE FPU index of 21.49 is consistent with those of other 80486 systems we've tested, and the BYTE video index of 5.57 is very good.

We did not run the BYTE application benchmarks on the Cheetah, but judging from the low-level indexes, we estimate that it would easily beat the current champ, the SIA 386/33, which also used the DPT controller with 4.5 megabytes of RAM. The SIA's cumulative application index is 32.64.

Cheetah takes advantage of the 80486's burst mode. The burst mode keeps the 8K-byte on-board cache filled, making memory accesses faster. Cheetah chose the burst-mode route over an external cache; ALR and Apricot have used external caches in their 80486 prototypes and seem to achieve better CPU speed as a result. With 8 megabytes of system RAM, the burst mode allows for zero-wait-state operation. (For more information on the 80486's burst mode, see "The 80486: A Hardware Perspective," *IBM Special Edition*, Fall 1989.)

Lots of Chips

The Cheetah's entire cover lifts off in cowl-like fashion, revealing all the system components and the tower's rugged frame (see photo 2). The main system board takes up the bottom half of the unit. The 80486 CPU card, which also holds all the 70-nanosecond SIMM memory—up to 16 megabytes—installs in its own 32-bit slot at the bottom of the system board (see photo 3). Eight more 16-bit slots are available for expansion, although one is for internal use only.

A 250-watt power supply and fan (the only fan in the system) reside in the upper rear corner, behind the six mass storage device bays.

The system board has a high chip count. Cheetah prefers the flexibility of designing its own discrete logic over using ready-made third-party chip sets; this allows for more experimentation while designing the system and for making mid-production changes if necessary. Cheetah also claims that using a third-party chip set would be more expensive.

Cheetah uses the Award BIOS, modified for the 80486 CPU. The BIOS is cached in memory to boost performance. A power-on self test utility in the BIOS feeds a two-character LED readout on the system board; if the system fails, the code on this LED indicates where the problem lies.

The CPU board is actually two boards

continued



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sandwiched together: The GPX-486 CPU board is on one side, and the BMA (for burst-memory array) memory board is on the other. Cheetah engineered the two-board unit to minimize distance between components, providing a small performance gain. This design will become more significant as the clock speed on the 80486 increases.

An important feature of the Cheetah design is its flexibility. Installing a faster CPU or slower memory requires changing a DIP switch—adding a wait state. This allows all the various components to synchronize to the faster clock speed.

Although the Cheetah has eight slots, you have only five free once you've installed the serial/parallel I/O board, the VGA controller, and the hard disk drive controller. But for most applications, five slots will be adequate.

The case itself is a clean, attractive design, but with one potential flaw. The on/off switch is located on an extended portion on the front and is vulnerable to errant legs, feet, or other moving objects. Cheetah said that the switch design is not final and might be changed in the production version.

Power to the Proletariat?

The high end of the Intel-based personal computers have served mainly the most power-hungry users: engineers and architects using CAD, financial analysts, software developers, and so on. But Cheetah has priced its state-of-the-art screamer within reach of small-business users.

Small-business folk generally don't need 80486 power; given the software that they tend to use and their applications, small businesses won't see enough productivity gain to justify buying the top of the line. But once the Cheetah and other low-priced 80486 systems become available, developers might see an opportunity for more powerful software on the low end of the application scale. In short, consumer acceptance of a low-cost high-end system would raise the lowest common denominator for basic computer applications software.

Oddly enough, the low price might be Cheetah's biggest problem. The concept of "perceived value" comes into play; potential customers might think that it isn't as good as Brand X's personal computer because it costs less. Judging from what we've seen, that would be an unfortunate assumption.

Michael E. Nadeau is BYTE's associate managing editor for reviews. He can be reached on BIX as "miken."

PowerFlex:

A Versatile, Upgradable AT Clone

Frank Hayes



Photo 4: *The ALR PowerFlex Model 40. This low-cost system features a clean design and an easy upgrade path.*

The PowerFlex Model 40 is an IBM AT compatible that uses a 12.5-MHz 80286 CPU—hardly big news in a world glutted with AT clones. What's news is that you can upgrade this inexpensive system to either a 16-MHz 80386SX or a 25-MHz 80486. With prices starting at $1495 and running up to about $4500 for an 80486 system, the PowerFlex is the most versatile system on the market.

The entry-level version of the PowerFlex is a standard small-footprint AT clone (see photo 4). It comes with 1 megabyte of RAM standard, upgradable to 5 megabytes on the motherboard and a maximum of 16 megabytes using memory boards. The Model 40 also has a socket on the motherboard for an 8-MHz 80287 math coprocessor, and it has built-in parallel and serial ports and floppy and hard disk drive controllers.

The system comes with a high-density 3½-inch floppy disk drive and a 40-megabyte, 40-millisecond hard disk drive. The built-in controllers can handle a second drive of each kind—there is space for a total of four. ALR offers optional floppy disk drives (5¼- or 3½-inch) and a 150-megabyte tape backup system.

There are six expansion slots—one 8-bit and five 16-bit. You'll have to fill one with a video card, leaving five free for additional expansion.

But the PowerFlex also has a slot for plug-in processor cards. For $395 you can get a 16-MHz 80386SX card, which includes a socket for an optional 16-MHz 80387SX math coprocessor (which costs another $300 to $350). Once the 80486 is available in quantity (probably by the end of this year), ALR will also offer a 25-MHz 80486 plug-in card for $2995 (see photo 5). That's twice the price of the computer itself, but the total cost of about $4500 will still make it one of the least-expensive 80486s on the market. If you decide to upgrade to the 80486 card from an 80386SX card, ALR will buy back the 80386SX card for the full purchase price.

The No-Cache Catch

There is a catch, though: Being an AT clone, the PowerFlex has a standard AT-style 16-bit bus. That doesn't hurt the machine's performance with the SX upgrade, of course; the SX was always intended as a 16-bit version of the 80386. The BYTE benchmarks (see table 1) show that with the 80386SX upgrade, the PowerFlex is a reasonable, though not spectacular, performer.

However, the benchmarks also show how the narrow bus bottles up much of the 80486's power. Compared to the other 80486 computers and upgrade boards we've seen, the PowerFlex with an 80486 runs the BYTE CPU benchmarks slower than any other 80486, and barely half as fast as its larger cousin, the PowerCache 4.

There are two reasons for this. First, every memory access through the PowerFlex's 16-bit bus takes twice as long as through a 32-bit bus. Second, the PowerFlex has no external cache; it depends entirely on the 80486's 8K-byte internal cache. Although the on-board cache helps performance, we've found that 80486 machines with a large external cache simply run faster than those without, especially when working on real-world applications in which all data won't fit in the 8K-byte on-board cache.

But although it's the slowest 80486, its CPU index is still higher than those of most 25-MHz 80386 machines. FPU performance, which isn't significantly affected by cache size, is more than twice as fast as a 25-MHz 80387—and 40 percent faster than the 33-MHz version.

Table 1: *ALR's two PowerCache 4 models take the number 1 and number 2 spots for the fastest CPU index. The indexes for the 80286 and 80386SX versions of the ALR PowerFlex are also included. The Cheetah Gold 33's excellent disk index is courtesy of a DPT SmartCache controller with 4.5 megabytes of RAM. We've listed the Apricot, IBM, and Everex systems for comparison.*

BENCHMARK RESULTS

Computer	CPU	FPU	Disk	Video
Cheetah Gold 33	6.52	21.49	9.49	5.57
PowerFlex 486	4.18	21.85	4.54	3.80
PowerCache 4 (desktop)	7.34	21.62	2.40	5.16
PowerCache 4 (tower)	7.37	21.80	2.63	5.16
PowerFlex 286	1.59	1.85	3.26	1.35
PowerFlex 386SX	1.89	4.09	4.05	1.61
Apricot VX FT	6.72	21.95	2.66	5.40
IBM Model 70-A21/486	5.29	21.39	1.75	4.34
Everex 386/33	6.84	15.48	2.45	4.26

For a full description of all the benchmarks, see "Introducing the New BYTE Benchmarks," June 1988 BYTE.

Plug and Play

The PowerFlex CPU upgrades are, for the most part, remarkably simple to in-

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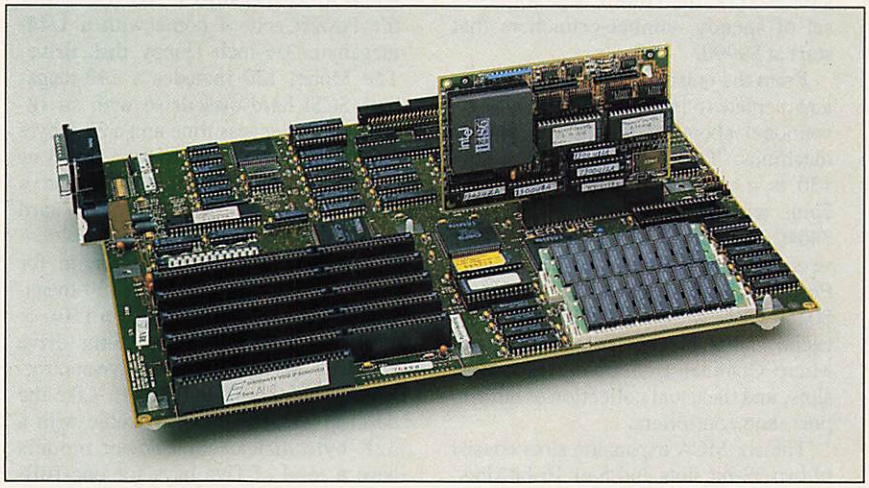
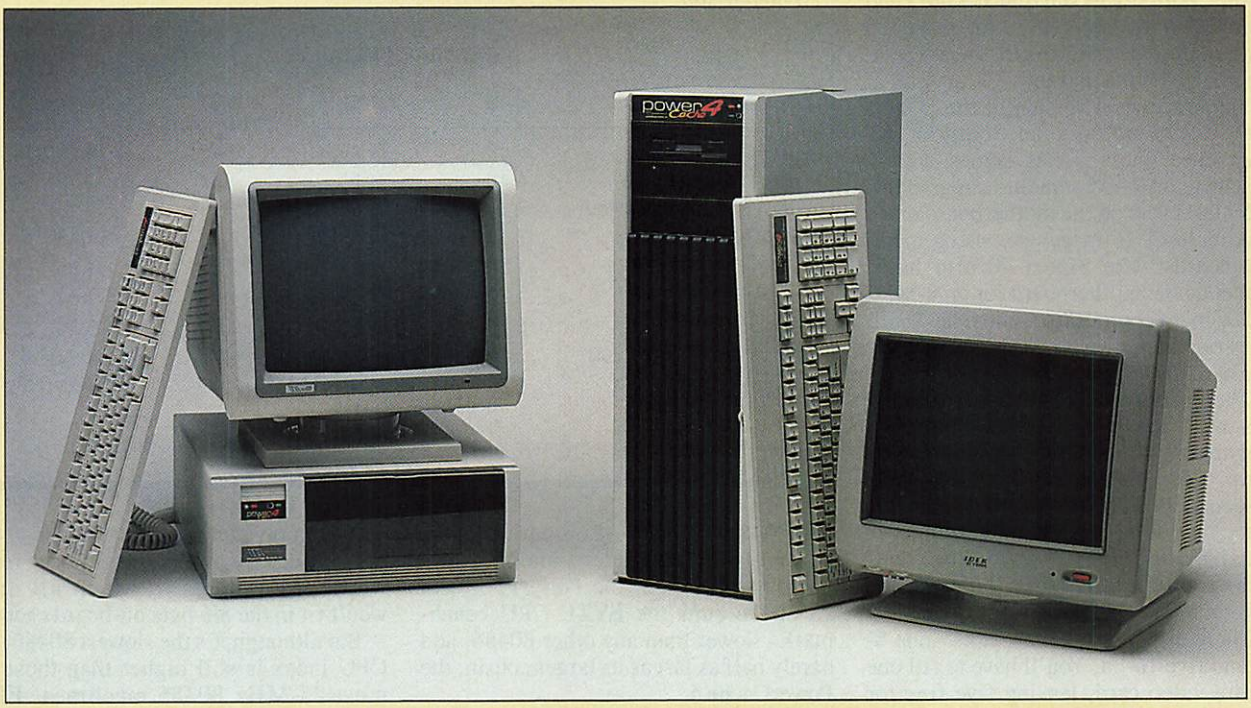


Photo 5: *The PowerFlex 80486 CPU upgrade module, installed on the motherboard. The hardest part of installing this card is removing the 80287 math coprocessor, if necessary.*

ALR's Other 80486s: the PowerCache 4 Duo



The 80486 screamers are beginning to pile up. First, IBM showed its Power Platform upgrade for the Model 70-A21. Then British computer maker Apricot demonstrated an 80486-based machine with prices starting at around $18,000. Now, we've seen Advanced Logic Research's first entries in the sweepstakes, the PowerCache 4 line—a set of speedy number-crunchers that start at $9990.

From the outside, there's nothing but a nameplate to indicate anything unconventional about ALR's PowerCache 4 machines. The PowerCache 4 Model 130 is a small-footprint desktop machine with PS/2 styling; Models 150, 340H, and 650H are larger, tower-style versions (see photo). Inside, all the PowerCache 4 models use a 25-MHz 80486 CPU with a 128K-byte external cache and 2 megabytes of RAM, six Micro Channel architecture expansion slots, and the usual collection of built-in ports and controllers.

The six MCA expansion slots consist of two 32-bit slots and four 16-bit slots. Two of the 16-bit slots are taken up by a VGA video card (640- by 480-pixel graphics in 16 colors) and a disk drive controller card; the rest of the slots are free. On the motherboard are ports for a printer, a mouse, a keyboard, and one serial device (e.g., a modem or a graphics tablet).

ALR's proprietary memory-expansion slot lets you expand the system RAM to 32 megabytes. All versions of the PowerCache 4 come with a 1.44-megabyte 3½-inch floppy disk drive. The Model 130 includes a 130-megabyte SCSI hard disk drive with an 18-millisecond access time and a 32K-byte disk cache. There's room for as many as three removable-media drives, and a total of four bays for floppy and hard disk drives.

The tower versions have room for larger hard disk drives: a 150-megabyte, 18-ms ESDI drive (Model 150), or a 340- or 650-megabyte, 16-ms drive with a 15-MHz ESDI disk drive controller (Models 340H and 650H). Like the desktop version, these all come with a 32K-byte disk cache. Tower models have a total of five bays for one full-height, two half-height, and two 3½-inch drives. In short, these PowerCache 4 models look like conventional IBM PS/2 clones until you run software and the 80486 CPU starts working its magic.

When the Magic Begins

That magic showed up when we ran the BYTE benchmarks. The PowerCache 4 tower models ran the CPU benchmarks with an index of 7.37, while the desktop version ran with a CPU index of 7.34.

That makes them the fastest PC-compatible computers we've ever clocked—about 10 percent faster than any other 80486-based machine, and 7 percent faster than the previous speed champ, Everex's 33-MHz 80386 machine. As we've seen in the past, the 80486 difference is even more dramatic with floating-point benchmarks. The tower version achieves an index of 21.80 on the FPU tests, while the desktop version has an FPU index of 21.62. That's more than 35 percent faster than any 33-MHz 80387 we've seen.

How does the PowerCache do it? Like the 80486-based Apricot VX FT, the PowerCache gets its speed advantage from a large external cache—something

that, six months ago, neither Intel nor computer makers thought they'd need with the 80486. Here's why: The 80486 has an 8K-byte on-chip cache that, Intel says, can handle 85 percent to 90 percent of normal memory reads.

Software typically accesses memory on an 85/15 basis—that is, 85 percent of memory accesses involve reading the contents of memory, and only 15 percent involve writing to memory. Most memory accesses are reads. But if the 80486's on-chip cache handles most of the reads, the percentages break down differently. Out of every 100 software memory accesses, about 13 will be memory reads, 15 will be memory writes, and the other 72 will be handled by the on-chip cache.

In other words, with the 80486, there are far fewer actual memory accesses, and reads and writes are much more balanced. Intel originally thought that would make an external cache unnecessary, but designers are finding that an external cache can give 80486 performance a significant boost. However, they're also finding that the more balanced read/write ratio changes the rules for designing an efficient cache. ALR's solution is a "write-back" cache that uses a pair of custom cache-controller chips working in parallel and 128K bytes of 25-nanosecond static RAM.

Combining this cache design with the 80486's burst mode, the PowerCache 4 machines are fast enough to outrun everything else we've ever tested.

Just Another Fast Clone?

At $9990 for the desktop version with a 130-megabyte hard disk drive, the PowerCache 4 is more affordable than some 33-MHz 80386 machines, and it offers much better floating-point performance—making it a good choice for many scientific and CAD applications. And the tower versions (with a 150-megabyte hard disk drive for $11,490; with a 340-megabyte drive for $14,490; with a 650-megabyte drive for $16,490) should be good choices as network servers. It's odd to describe one of the first 80486 machines as "just another (extremely) fast 80386 clone," but that's what the PowerCache 4 is: a conventional PC with a very speedy CPU inside.

It looks like ALR's commitment is to putting that speed on (or next to) lots of desktops, and that suits us just fine.

stall. The 80386SX upgrade card is about the size of a short expansion card; the slot that it plugs into is keyed and the card is notched, so it's impossible to put the card in backward. A small plastic support runs through a hole in the card, helping to hold it in place. The prototype 80486 card we saw is similar, though longer—but still much smaller than IBM's Power Platform upgrade.

The CPU cards go in and come out of the computer quickly. With the cover off, it took just seconds to convert from a plain-vanilla AT clone to an 80386SX or an 80486 semi-screamer—with just one exception.

The most complicated part of the upgrade process is installing or removing the 80287 math coprocessor, if that's necessary. The 80287 goes into a DIP socket on the motherboard. Although the socket is not completely inaccessible, the math coprocessor still requires a good eye and a steady hand to install, and a chip-puller to remove—more equipment than the CPU upgrades require. However, ALR recommends removing the 80287 if you're using an 80386SX upgrade card with an 80387SX math coprocessor installed, or with an 80486. (You can also use the 80386SX upgrade without an 80387SX and with an 80287 installed on the motherboard.)

Except for removing the 80287, swapping CPUs took about 10 seconds—less time than it took to change video cards. ALR claims that its CPU upgrades are "plug and play," and we think that's a fair description. You probably won't want to do it every day—but when you need to, it won't take long.

The Ferrari Syndrome

These days, an AT clone isn't considered a high-performance number-cruncher. It's more like the Volkswagen Beetle of desktop computers—cheap and reliable, but not exactly a thrill machine. Adding an 80486 is like dropping a Ferrari engine into that VW—it runs faster, but it'll never be a Ferrari.

On the other hand, the PowerFlex offers the widest upgrade path that's currently available. You can start with an AT clone and—without major surgery on your computer—work your way up to a much more powerful system. The idea—an ambling AT clone that can be upgraded to a rocket-on-a-desktop—may be crazy. But it's the kind of craziness we like to see. ■

Frank Hayes is BYTE's West Coast news editor. He can be reached on BIX as "frankhayes."

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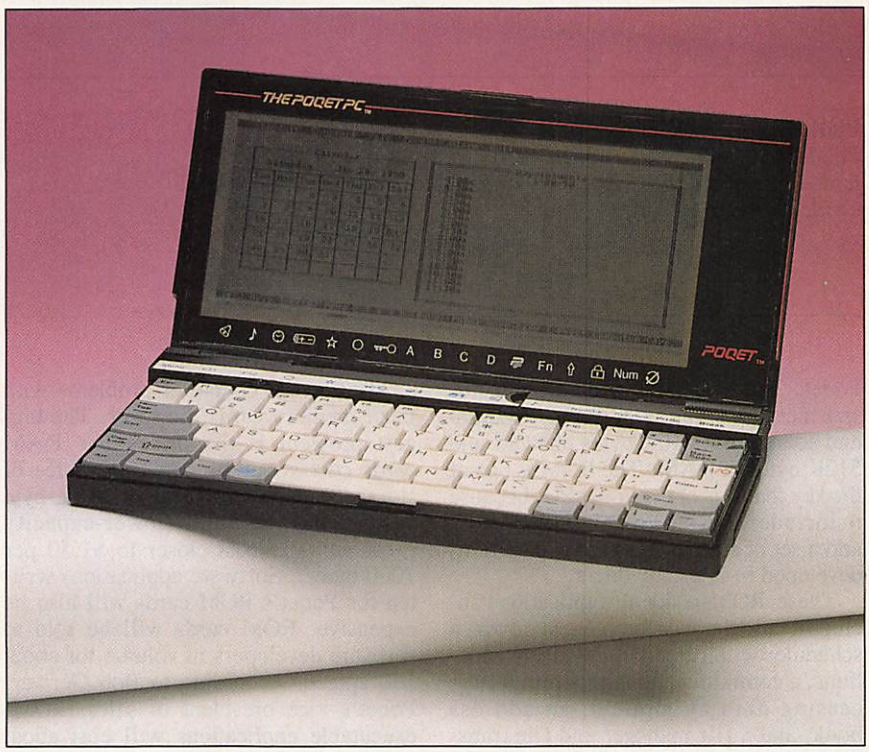


Photo 1: *The Poqet PC, shown unfolded. The small nonbacklit LCD screen can display 25 rows of 80 columns and CGA-compatible graphics. The keyboard features 77 keys, with each key measuring about one-half inch square, and has an embedded numeric keypad.*

Last August we featured the latest in portable machines from Zenith and Agilis. In fact, the title on the cover of that issue was "Small Wonders." But wonders never cease. Recently, a new start-up company called Poqet Computer introduced a full-fledged equivalent of an IBM PC that is small enough to fit into your coat pocket. Despite its size, the Poqet PC includes 512K bytes of memory, a 7-inch monochrome LCD screen, and a power supply reportedly capable of powering the system for about 100 hours.

The Poqet PC's power supply is one of the most interesting parts of the system. It consists of just two ordinary AA alkaline batteries. The 100-hour battery life translates into an average power consumption of only about 60 milliwatts—a truly remarkable accomplishment, considering that the Poqet PC powers a considerable amount of memory and a fairly high-resolution LCD display.

According to Poqet's vice president of engineering, John Fairbanks, who came to Poqet from Texas Instruments' calculator design group, the major breakthrough in the design of the Poqet PC was an order-of-magnitude (10 to 1) reduction in the amount of power required to drive the display, as compared to other laptop computers (about 10 mW versus the 100 or more mW required in other laptop designs). Poqet is in the process of applying for patents on its power management design and declined to disclose to us the technical details behind the design of the display power driver.

In appearance, the Poqet PC has the basic clamshell design used by most laptop systems (see photo 1). The machine folds up to about the size of a VHS tape cartridge (see photo 2). Its dimensions when folded are 0.925 by 8.75 by 4.3 inches. The price tag for the 1-pound system is about $2000.

The nonbacklit monochrome display measures 6.8 by 2.7 inches and has a fairly flat aspect ratio. It supports 80 columns by 25 rows with 640- by 200-pixel resolution in both CGA and MDA modes.

The machine has a 77-key keyboard with 12 function keys. The keyboard includes an embedded numeric keypad, which is accessed via a special "Poqet" function key. The keys are about one-half inch square and have a springy tactile response.

Inside is an Intel 80C88 microprocessor running at a clock speed of 7 MHz (40 percent faster than that of the original IBM PC). The BIOS and processor-support chip sets were custom-designed by

continued

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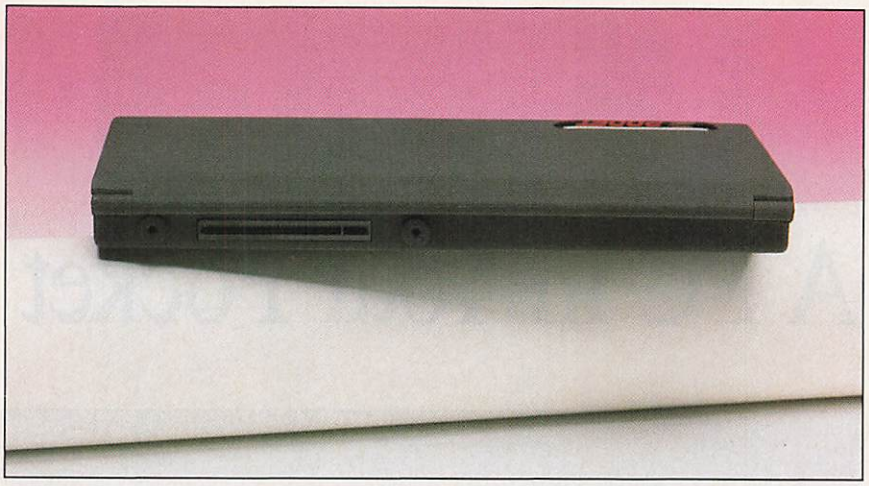


Photo 2: *Rear view of the Poqet PC, folded for traveling. When folded, it's about the size of a videocassette.*

COMPANY INFORMATION

Poqet Computer Corp.
650 North Mary Ave.
Sunnyvale, CA 94086
(408) 737-8100
Inquiry 1163.

Poqet. The Poqet PC uses credit-card-size memory cards as its storage medium and comes with 640K bytes of ROM and 512K bytes of RAM. The ROM is one of the key features of the Poqet PC, because it includes MS-DOS 3.3, GWBASIC, and a set of simple software applications developed in-house by Poqet.

These ROM-resident applications include a calculator, a simple text editor, a scheduler with calendar and alarm functions, a communications program for accessing data by modem, an address book, and a file manager and file transfer program. Because this software is all in ROM, it runs at the speed of the memory bus (there is no performance loss due to disk access). You can access the built-in applications via a hot-key sequence, which activates a pop-up menu.

Memory cards are the primary storage medium for the machine. The machine has two slots for sliding in cards, providing the equivalent of two floppy disk drives, with memory capacities ranging from 32K to 512K bytes. The memory cards come in two versions—RAM cards for storing data, and ROM cards for running software applications.

An important feature of the system is that software applications supplied on ROM cards will execute directly from the ROM cards. Conventional PCs load the applications from disk into RAM, but the Poqet PC leaves most of its 512K bytes of RAM available for data storage.

There are a couple of problems with these memory cards, however. The biggest problem is the price. The RAM cards cost about $1 per 1000 bytes of storage capacity, making a 512K-byte card cost over $500 (lower-capacity cards actually cost closer to $1.50 per 1000 bytes). Software applications written for Poqet's ROM cards will also be expensive. ROM cards will be sold to software developers in volume for about $50 apiece. According to Bob Gerwer, Poqet's vice president of sales, ROM-executable applications will cost about 15 percent more than their floppy disk equivalents.

The Poqet PC's power supply is one of the most interesting parts of the system. It consists of just two ordinary AA alkaline batteries.

Another hitch is that software developers must rewrite their applications to run on the ROM cards. Although you will be able to run standard DOS applications off RAM cards, which load the code into the Poqet PC's RAM, you won't get the performance and memory-saving benefits of ROM-executable software.

However, Poqet's chief software engineer, Ian Cullimore, told me that third-party software vendors are enthusiastic about porting their applications to the Poqet PC. He also said that applications written with "modern C compilers" or in assembly language are easy to port, requiring "basically a recompilation." An inside source at Lotus Development confirmed that Lotus "has been working very closely with Poqet." One advantage to ROM-card applications from the point of view of software developers is that they are automatically copy-protected (you can't run a program that has been copied from ROM into regular memory).

The Poqet PC includes an 80-pin XT-bus card connector and comes with a special cable for connecting the connector to another PC or peripheral. The bus connector can attain RS-232C serial communications at up to 19,200 bits per second. The special cable has a Y connector at one end, with both DB-9 and DB-25 serial port connectors.

The Poqet PC's $2000 price includes the 640K bytes of ROM, the 512K bytes of RAM, the special bus and peripheral connector cable, and the built-in DOS, GWBASIC, and ROM-resident desktop applications. For an additional $395, Poqet is offering an external, battery-powered 1.44-megabyte 3½-inch floppy disk drive, with a battery life of about 20 hours.

Poqet is working on a memory-card reader that will plug into PC compatibles so that data can be copied directly onto the memory card from the host machine. The memory-card reader was scheduled to be available shortly after the Poqet PC began shipping in September and will cost a "few hundred dollars," according to Bob Gerwer.

The Poqet's memory is powered all the time to conserve data. Much of the system, however, stays in "sleep mode." According to Poqet, its special BIOS puts most of the system to sleep between keystrokes. The screen stays powered and the user doesn't notice anything unusual, but the CPU is put to rest until the next key is pressed. The only really active circuit is the keyboard scanner. After 2 minutes of inactivity, the display is

powered down as well. A red key labeled "I/O" powers up the microprocessor and display when you want to use the computer again.

The screen has a set of visual indicators at the bottom, which include a low-battery warning indicator, as well as memory-card access, alarm clock, and function-key indicators. The system also includes a capacitor that keeps the system powered up for about 5 or 10 minutes while you change batteries. The memory cards have their own lithium backup batteries, which have a life expectancy of one to two years.

I had a chance to work with a prototype version of the Poqet PC. The screen on the unit that I tried was readable but suffered from lack of contrast. This should be improved on the final production unit by a tighter-fitting screen overlay. The keyboard was remarkably easy to use considering the size of the machine. Not all the built-in ROM applications were working in the unit that I tried, but a version of Lotus 1-2-3 ran normally. (In the near future, BYTE will follow up this article with a full review of a production version of the system.)

This machine has enormous potential for business travelers and others needing computing power on the road, in the field, or in the classroom. Basically, the Poqet PC brings the power and capabilities of a personal computer into the realm of pocket calculators. Indeed, the design of the Poqet PC is the result of a joint design effort involving specialists in consumer electronics, semiconductor packaging, and computer systems design.

Having worked with only a prototype, I find it difficult to pass judgment on the Poqet PC's reliability and performance. The high cost of memory cards, the machine's primary storage medium, is certainly a drawback. But this machine breaks new ground in portability and power consumption. And, as volume increases, memory-card prices will drop.

The Poqet PC could be a smashing success. This is, after all, a consumer electronics product. As with other breakthrough products, however, the keys to success are the degree of consumer acceptance and the time it takes to gain that acceptance. Although $2000 seems a fair price for the Poqet PC, it may not be cheap enough to attract large sales volumes. But we wish Poqet the best of luck. The Poqet PC is certainly the result of some brilliant engineering. ■

Nick Baran is the BYTE bureau chief in San Francisco. He can be reached on BIX as "nickbaran."

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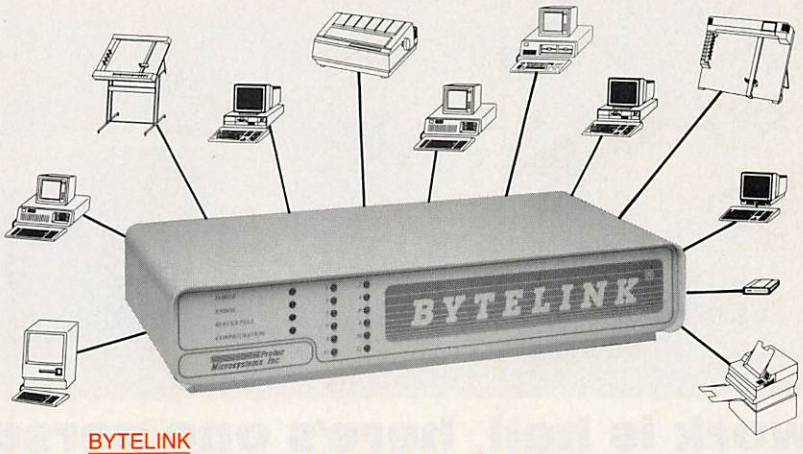
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*Base System with Single Floppy Drive, No Video

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Disk Drive Options	12-Inch Mono	Color Graphics CGA	EGA
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Parallel Ports	1	1
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Circle 193 on Reader Service Card (DEALERS: 194)



THE INSTALLATION BLUES

The quest for on-line reference materials is never smooth

Long ago, I reviewed a CP/M database program called Vulcan that caused me to invent the rating "infuriatingly excellent"; meaning that the program did something I very much wanted done, but I had to fight it every step of the way. The algorithms were far better than the user interface. Incidentally, that was the first review of the program that became dBASE II. George Tate once told me he bought Vulcan (and renamed it) as a result of my review.

This month I have another program I can only call infuriatingly excellent. I don't expect it to become another dBASE II, but showing why it's infuriating may prove to be a good object lesson for program designers.

Dictionary on a Disk

It started in Boston at the National Education and Computers Conference. There wasn't much good educational software. With few exceptions, what we saw either wasn't impressive for its educational value or wasn't well designed as software. I'm not sure why.

One thing that did impress me was a dictionary program. It ran on a hard disk, rather than a CD-ROM, and thus needed a lot of hard disk space; on the other hand, it was very fast. Better yet, it had a whole raft of dictionaries, including *Funk & Wagnall's Standard Desk Dictionary*, with all the auxiliary stuff (e.g., the *Secretary's Handbook*); a 26-language dictionary; and the McGraw-Hill science dictionaries, including computers, physics, chemistry, biology, and various engineering disciplines. All this information takes up disk space, but since I have a Priam 330-megabyte hard disk drive, I *have* disk space.

I didn't have time to spend looking at the demonstration, but that hardly mattered, because, as I explained to them, I don't write about stuff I don't have running at Chaos Manor. They collected my card, and I went on to the next booth.

A few weeks later there arrived a dozen boxes: one for each of the dictionaries. Each proclaimed itself part of the Inductel Reference Series, and on the back cover each had in boldface type the sentence, "So easy to use, you don't have to refer to the manual." All I need, it says on the box, is 5 megabytes of disk storage, 256K bytes of RAM, and DOS 2.0 or higher. Wonderful.

It wasn't clear whether the various special dictionaries worked alone or were add-ons to one of the main dictionary programs, but that didn't seem important. (It turns out they will work together, but each is a separate stand-alone product.) I knew where to start: I opened the Funk & Wagnall's box. Inside was a reasonably thick manual. There were also 16 5¼-inch floppy disks, which wasn't too surprising—the box did say I needed 5 megabytes of disk space—but it was a bit intimidating.

A quick look through the manual made one thing clear: they'd better be right when they claim you don't need the manual to work the programs. The first 15 pages or so are in legalese and proved to be the license agreement, one so long that I doubt anyone but me has ever read it. Underneath all the jargon, it's pretty reasonable. After pages of legalisms, there were two pages about the theory of knowledge acquisition. The manual insists on explaining inductive and deductive reasoning before it tells how to use the program. It doesn't explain why I would want to know this stuff. If the purpose was to discourage me from reading the manual, it nearly accomplished that.

Finally, way back in the manual were the installation instructions: take the first of the 16 floppy disks, put it in drive A, log onto that, and type `Install`. The program would do the rest.

Install produces a couple of screens of inquiries about colors and then gets down to business. What hard disk drive do you want this installed on? I told it drive D. What floppy disk will you install it from? Since Big Cheetah has only one 5¼-inch drive, that had to be A. Then Install displays a screen with four choices: standard-density 5¼, high-density 5¼, standard-density 3½, or high-density 3½. You choose one. Looking into the manual yields this advice: "Use the cursor key to highlight the desired entry, then hit the Enter key to select it."

Well, all right, Big Cheetah has a high-density 5¼-inch drive, so that's what I selected.

The Install program trundled for a while, in the process displaying the message, "Consult the license agreement in your user's manual to be sure you are not violating it." I thought that a rather unfriendly thing to say, but what the heck. After a while, it told me to insert disk 2. Then disk 3. Then disk 4. When it finished disk 4, it dropped me out of the Install program and into the new D:\KAS (Knowledge Acquisition System) directory it had created. No error message. No "finished" message. There I was, with 12 disks left over.

Try again. You have to start all over, of course. The Install program is not a batch file, so you can't even get inside and inspect it. Just start over.

That worked no better than the first time.

Well, I thought, maybe it knows something I don't. Might as well install the physics dictionary. It's only six disks.

The physics dictionary package had a manual identical to the one in the Funk & Wagnall's package. Obviously the instructions for installing it were also the same: insert disk 1, log onto it, and type `Install`.

It asked the same questions. This time

continued

it wanted only two of the six disks before it dropped me out of the program and back to DOS. Curiouser and curiouser.

It was time to try the program.

Lockup Time

I thought I'd see what definition the physics dictionary had for the word *force*. First I had to figure out how to ask. The KAS program interface is strange. It uses terms I don't understand and isn't well explained in the manual. There are no error messages. I did what I thought was appropriate—and locked up the machine. Thoroughly. No way out but reset. Hardware reset.

I tried again. Same thing. No error messages. Just no results, and the machine hangs.

I got out the manual and tried following its instructions. Unfortunately, the example in the manual is for the 26-language dictionary, and I didn't much feel like installing that, so I had to infer what to do with the dictionaries I did have installed. It was pretty clear I was doing things right, but the program hung the machine anyway. Three more resets, and I gave up.

Could They Have Meant...

I was ready to put the program away when an idea struck me. Suppose—just suppose—when the Install program asked me about floppy disks, it didn't want me to describe my drive at all? Suppose it was asking what kind of disk I was using to install the dictionaries? Suppose it had no way of knowing that I hadn't loaded the entire 16 disks' worth?...

"Naaah," I thought. No one would be *that* stupid. But just in case, I got out the physics dictionary and went through the tedious Install program again. This time I told it I was installing from standard-density 5¼-inch floppy disks.

Voilà! This time it wanted all six disks. Quickly I reinstalled the chemistry and computer science programs, noting that each time it copied the access program and then what it called "the decompression code" before copying the database.

When I tested the program, the machine hung again.

Well, I thought, there is that partial Funk & Wagnall's dictionary on there; best to reinstall that, although the prospect of feeding the machine 16 floppy disks wasn't very appealing. Still, it had to be done, so have at it.

I got out the box, put disk 1 into drive A, and began the imbecile Install program. It went along for five disks, flashed an error message about being unable to open a data file, and dropped me back into DOS. Now what?

Try Again

The Inductel manual says installation might fail for one of several reasons. First, you might not have enough memory. That wasn't a problem. Second, not enough disk space. That wasn't a problem either. Third, "the computer's disk head is out of alignment." I have never had any problem with my high-density drive *reading* a standard 360K-byte floppy disk. You can get into difficulties trying to write to a 360K-byte disk with a 1.2-megabyte floppy disk drive, but reading always worked before.

Finally, the manual states that if all else fails, "then chances are you have a 'marginal' or 'faulty' disk in your software package." You can return it and get an exchange. The only problem is, this

continued



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Circle 226 on Reader Service Card (DEALERS: 227)

When You're Buying A Personal Computer, Make Sure You Know What's Built In And What's Left Out.

Circle 34 on Reader Service Card (DEALERS: 35)

column is due Monday morning and it's Saturday night.

I have a 360K-byte floppy disk drive on my Zenith Z-386. Moreover, I've got a WORM (write once, read many times) drive on both the Z-386 and Big Cheetah; I figured that if I got it all installed on the Z-386, I could make a safety copy onto the Maximum Storage WORM and then bring that WORM cartridge over to Big Cheetah and transfer the files.

It took about an hour to install all those dictionaries on the Z-386. I had a mild moment of panic: after going through the 16 disks of Funk & Wagnall's dictionary, the program very briefly flashed an error message and dropped into DOS. Of course, it also erased the error message, so I didn't know what it was; and I wasn't interested in feeding 16 floppy disks in yet one more time. This was getting as tedious as trying to install Microsoft Windows.

Fortunately, the program seemed to work. I decided this was just another imbecility of the Install program: it detects some kind of error to tell it that it's done with its job. Why not? I got out the other boxes of dictionaries. Eventually they were all installed. By then, it was 5:00 a.m. I'd used up hours installing the thing. Now to test the program.

Look It Up

It works surprisingly well. Once you tell it what you want it to do, the program is *very* fast. The problem is telling it what to do: it has as awkward a user interface as I have ever seen. Inductel's KAS manages to make the Oxford English Dictionary on CD-ROM (see my October column) look positively user-friendly.

What you must do is use the arrow keys (there's no mouse capability) to move among menus until you select a mode of operation. Then you go down into another part of the screen to select which dictionary you want to consult. Then you input the word you want looked up. That can also be a complex job using arrow keys, but fortunately you can shorten it: you type in the word with wild-card characters, get a list of terms it understands, and use the arrow keys to select the term; or, you can just type in the term yourself.

Once that's done, the answer is almost instantaneous. This thing is *fast*.

There's also a TSR mode: load the KAS as a TSR program and then go into your favorite word processor, put the cursor on a word, and press Alt-M. You will find yourself in the KAS command system. Now select a dictionary and input your word; or, possibly, it will already have a dictionary selected. That may be the wrong one, but as long as you're in the KAS command system, you can change the "active" dictionary to another. This is important because some terms will have quite different definitions depending on whether you are looking them up in the physics, biology, Funk & Wagnall's, or 26-language dictionary.

This all works very rapidly and very well on the Z-386.

Blowups Happen

By now I was almost ready to forgive Inductel for their imbecile Install program. I have paper copies of many of those science dictionaries, and I use them; this looked very useful. Moreover, I sometimes have a need to look up foreign words, and the foreign-language dictionary aspect of this thing is *neat*:

continued

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COMPARE FOR YOURSELF

Feature	**AST Premium 386SX/16**	COMPAQ DESKPRO® 386s	COMPAQ DESKPRO® 286e	IBM® PS/2™ Model 55
Processor				
Type	**386SX**	386SX	286	386SX
Speed	**16 MHz**	16 MHz	12 MHz	16 MHz
Available Slots	**5**	4	4	3
EMS Support Software Included	**4.0**	3.2	4.0	No
Landmark Benchmarks*	**23.1**	15.4	11.6	15.3
List Price** One-Floppy System	**$2,695**	$3,299	$2,699	$3,895***

** Landmark Software version 1.1 benchmarks — a generalized index used to compare one machine to another. The higher the number, the better.*

*** List price is MSRP.*

**** List price with 30 MB hard drive; one-floppy system not available with this model.*

So, if you're considering an 80286- or 80386SX-based computer from a manufacturer like Compaq® or IBM®, make sure you compare it to the AST Premium 386SX/16. After all, if your needs require a workhorse, shouldn't you buy a thoroughbred?

AST® RESEARCH INC.

Circle 36 on Reader Service Card (DEALERS: 37)

when you look up a word in, say, French, it gives you the translation to not only English, but Spanish, Finnish, Esperanto, Greek, and 20 other languages simultaneously! I was actually enthusiastic as I saved this huge subdirectory off onto the WORM cartridge. It took quite a while—there are over 14 megabytes of dictionary files—but eventually it was done. I put the cartridge into Big Cheetah's WORM drive and copied the whole mess into the D:\KAS subdirectory.

The program didn't work. It said it couldn't find any database files. None. Zero. I mean, there they were, 14 megabytes' worth of them, but the program couldn't find any. Some kind of "copy protection"?

Nothing for it, then: back to Install. I selected the computer science dictionary, since it was the smallest. Put disk 1 into drive A. Answer the dumb questions. Swap disks. Get done with it, and test the program.

It worked. Try it in a DESQview window. It worked there, too. Now try it in TSR mode.

The machine hung. Time to reset.

For the next hour, I tried to get the program to work in TSR mode on Big Cheetah. I tried with and without DESQview. I tried doing things to the CONFIG.SYS file. I tried everything I could think of, each time having to fight the dumbest Install program in the free world. Then I'd try TSR mode, and the machine would hang. Finally, in desperation, I decided to reinstall the original Funk & Wagnall's dictionary, all 16 disks of it. This time I was able to get it to read them all, so the job was merely tedious.

With every disk swap came the message, "Consult the license agreement in your user's manual to be sure you are not violating it." The problem was, by then, I *wanted* to violate the license agreement. Then I wanted to find and beat senseless the person who invented that horrible Install program.

So...

The bottom line is this: the program works wonderfully on the Z-386. It works in direct command mode on Big Cheetah, including within a DESQview window; but for some reason, it will not work in TSR mode on Big Cheetah, with or without DESQview. Perhaps Big Cheetah is too fast for the program. Perhaps QEMM is interfering with it. Perhaps I haven't properly installed something. Perhaps any number of things; but frankly I am too weary of fighting that moronic Install program to care.

If you want a very large and incredibly fast set of on-line dictionaries, this program will do the job. The user interface is horrible, and the Install program is worse; it might not work in TSR mode on your machine.

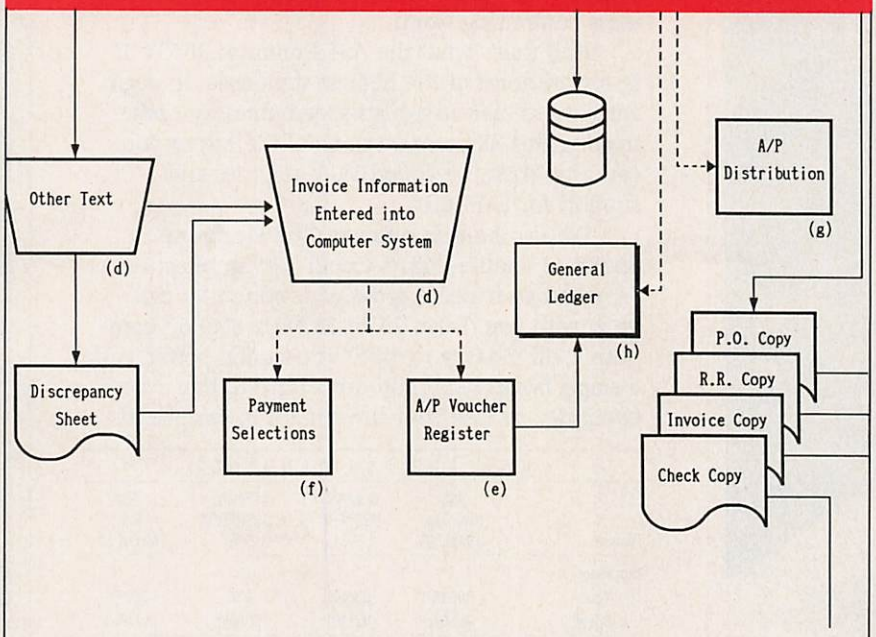
But once you do have it up and running, it's little short of amazing. If they'd put the work into user convenience that they did in developing those access algorithms, they'd have a wonderful program. As I said earlier, infuriatingly excellent.

Bribes

The most interesting bribe I've received recently was a package containing a split of champagne, a package of pumpernickel, a jar of pâté de foie gras, cookies, and a CD-ROM of over 7000 public domain, freeware, and shareware programs, every one of them tested by the Chicago RBBS-PC. Quanta Press sells

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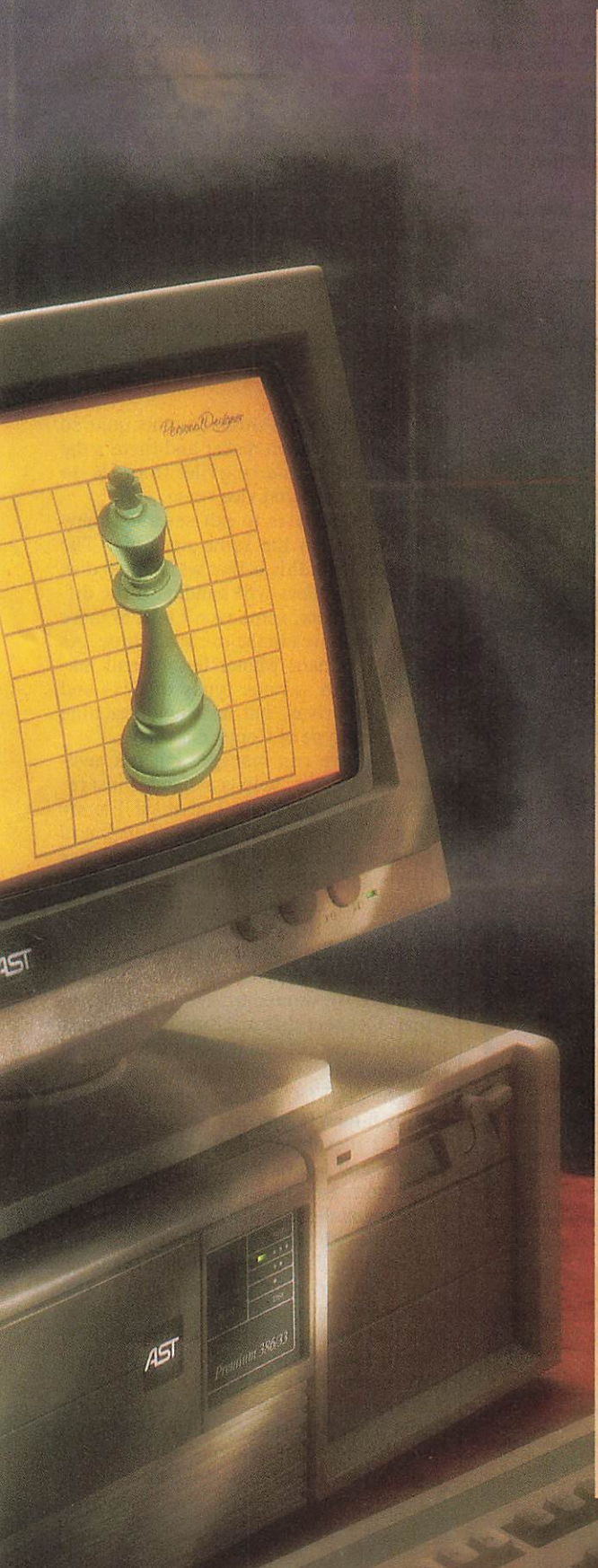
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In a recent InfoWorld magazine report card, the AST Premium 386/33 overwhelmed a selection of 33 MHz computers from vendors like Compaq®.

INFO WORLD BEST IN ITS CLASS

We weren't surprised. After all, the AST Premium 386/33 offers exceptional performance in a feature-packed, stylish chassis. Features like: zero wait-state cache, support for up to 36 MB of memory, support for 80387 and Weitek 3167 coprocessors and much more.

It's too bad that InfoWorld doesn't have a category for upgradeability. With a natural upgrade path to i486™ power using AST's Cupid-32™ architecture, the AST Premium 386/33 would be sure to earn even higher marks.

That's because Cupid-32 is AST's enhancement to the Industry Standard Architecture (ISA) that allows you to upgrade to new technology without buying a new computer.

So, if your company is looking for a 33 MHz computer, why not take a lesson from InfoWorld. Go straight to the head of the class.

REPORT CARD — INFO WORLD

	AST Premium 386/33	COMPAQ DESKPRO® 386/33
CPU speed	**Excellent**	Excellent
Expandability	**Excellent**	Excellent
Hardware compatibility	**Excellent**	Excellent
Documentation	**Excellent**	Good
Technical support	**Very Good**	Unacceptable
Value	**Good**	Satisfactory
Final Scores	**8.5**	7.1

Source: InfoWorld, July 24, 1989

AST® RESEARCH INC.

Circle 38 on Reader Service Card (DEALERS: 39)

this for $149 and "guarantees" the disk to be "virus free," although what such a guarantee means I don't know.

In any event, the Quanta Press RBBS-PC in a Box CD-ROM certainly contains the shareware of the month: word processors, games, communications stuff (including programs to let you run your own BBS), databases—you name it, it's all in there. I've had more fun digging through the programs on the disk than I did eating the cookies.

Disk Drive Blues

Back in CP/M days, we were plagued by an enormous variety of floppy disk formats. Not only were there 5¼- and 8-inch drives, but each hardware vendor had its own proprietary data format and density. Then came IBM, and whatever else you could say about the PC, at least there was some standardization of the disk formats.

Now it's a mess again: we have double- and high-density 5¼-inch formats, and ditto for 3½-inch. There are even a few oddball variations, like the Twister format for Atari 3½-inch disks, a trick that will get a bit more on each disk, although at the cost of being unreadable to those who don't have the tricky little program.

The worst mess is in the 5¼-inch size: as I noted above, while a high-density (AT-style, 1.2 megabytes per disk) drive can read double-density floppy disks (PC and XT style, 360K bytes per disk), when you use a high-density drive to *write* to a 360K-byte disk, the results are unreliable. It works, in that the file is written in 360K-byte format and often can be read by the machine that wrote it; but transferability to any other machine, high- or double-density, is something else again.

The situation is similar but not quite so bad with 3½-inch disks; and there's the problem of transferring files from 5¼- to 3½-inch disks and vice versa.

One remedy is to put several floppy disk drives in the same machine. The problem with this is that while most disk drive controllers will handle all the different formats, some won't talk to more than two drives in the same machine. As a result, Chaos Manor has several machines with various types of 5¼- and 3½-inch drives, but no single machine has every type of floppy disk drive.

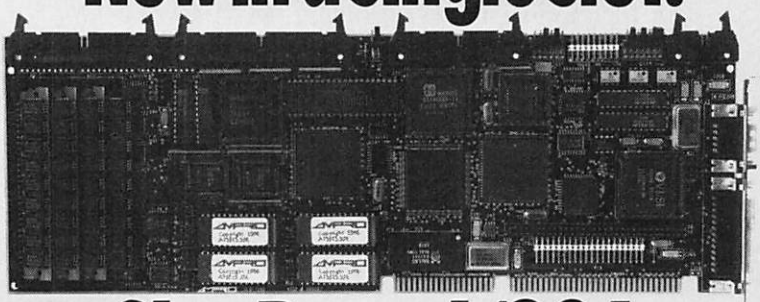
Thus, we can manage, but it's awkward. However, help is at hand: I just received the Northgate Universal Floppy Drive Controller (NUFDC). This board takes a separate slot from your hard disk drive controller; but once it has done that, it will run as many as four different floppy disk drives, and each one can be different; thus, we could have a machine with one of each of the four kinds of drives if we wanted to, and I may just do that. Connect that machine to the others with a network, and it won't matter what format I've got to read or write to.

The NUFDC is also capable of handling 8-inch floppy disk drives formatted as 1.2 megabytes; that takes a special cable, and I have not set that up yet, but I've no reason to assume it won't work. The manual doesn't say whether this will read the old "standard" single-sided single-density 128K-byte 8-inch disks some of us started with. I guess I don't care: when I really need an 8-inch disk read, or for that matter need files off an old CP/M weird-format 5¼-inch disk, I let Barry Workman take care of it.

The NUFDC works about as you'd expect it to. The setup is fairly tedious—I won't say complicated—but it comes with a well-illustrated booklet that shows

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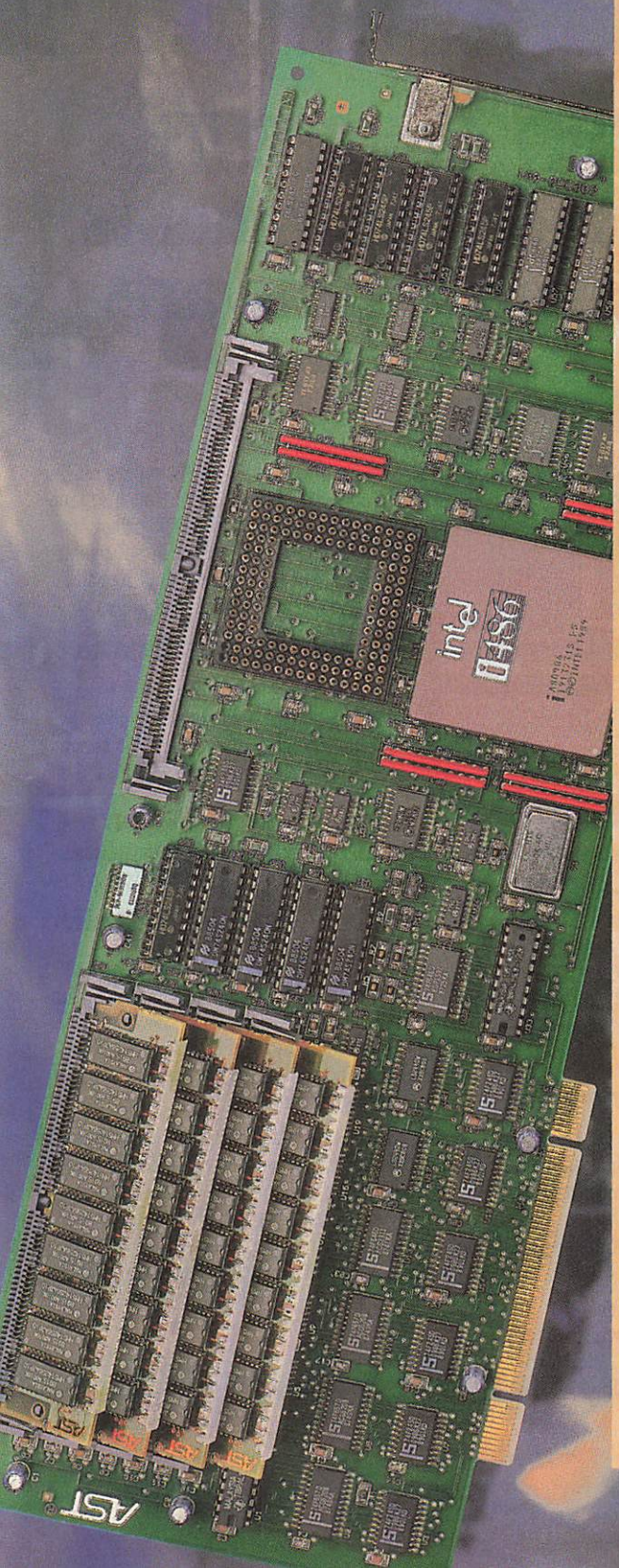
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More Tools are Coming

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Circle 306 on Reader Service Card

exactly how to set it up. After that, it's a mere matter of installing the board and drives and connecting the cables. I expect what I'll do is put this into the generic XT so that we can transfer from any disk to any other.

If you're still having disk format problems, Northgate has the answer.

Keyboards

The latest shipment from Northgate also included a big box of keyboards.

I have said for years that the best key layout ever invented was on the old IBM Selectric typewriter. Unfortunately, no one made a proper PC keyboard with that layout. First, IBM had their peculiarly dumb design, with extra keys between the Z and Shift keys, but with the function keys grouped on the left side. Then they changed to a keyboard with a reasonably standard layout, but the function keys were across the top, where you couldn't get at them easily. Then they changed to something else.

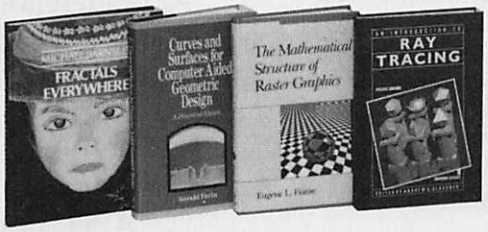
Somewhere along the line it got frozen into concrete that the Backspace key is way up in the upper right, where you cannot reach it from the home keys; while the bracket and brace keys were put just above the Return key, where they are in the way if you go after Backspace. There were various other tomfool "innovations," all caused by the fact that IBM engineers are not touch-typists. And IBM being the kind of company it is, no one ever bothered to ask the customers what they wanted. Meanwhile, other companies followed IBM's lead.

The result is a series of miserable keyboards all designed to make extra work. Every one of them, for example, has the less-than and greater-than keys as Shift-comma and Shift-period, which has the effect that when you're writing, you end up with U>S>A> instead of U.S.A., and stuff like that; and when you go to

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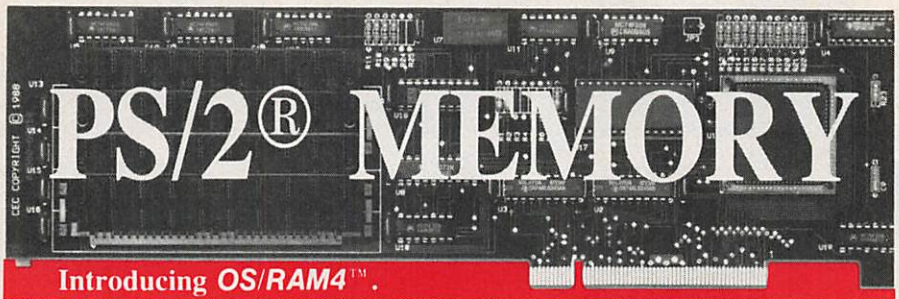


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backspace, you get]]]]] and once again have to go back and fix that. This breaks one's train of thought and makes small computers a bit less useful for creative writers than they otherwise would be.

Various companies have worked on this problem. DataDesk International makes very good after-market keyboards that many users like a lot, and which I used to swear by; but the keys didn't have the positive feel that the old Selectric did, nor was the layout the Selectric's.

Finally, Art Lazere of Northgate Systems designed a keyboard just for me. The function keys are grouped on the left side. The Control key is to the left of the A key, where God intended it to be. The Escape key is in the upper left, where it was on the old terminals we all started with. The keys have a wonderful positive click to them. There's a separate arrow-key cluster and a numeric keypad.

Best of all, the Backspace key is oversize and just above Return, so I reach it handily with my fingers on the home keys; and the bracket and brace keys are in the upper right, where I can get at them if I want them, but aren't in the way. There's an asterisk key next to the reverse backslash and vertical rule key; and while less than and greater than remain shifted comma and period, Lazere commissioned a 20-byte TSR program called POURVOUS.COM that fixes that (I do Alt-Shift-comma and -period to get less than and greater than). The result is the perfect keyboard—for me.

Apparently I am the only one who thinks so; Northgate hasn't sold many of the "Pournelle" layout keyboards. They sell a lot of their standard ones, which, I have to say, would be my favorites if I didn't have the "Pournelle" layout. Anyway, it works out well for me: because almost no one bought the keyboards configured the way I like them, there were a number of them in the Northgate warehouse; and I now have five of them, which you can pry away from my cold dead fingers.

The Gadget War

In *The Mote in God's Eye* (Larry Niven and Jerry Pournelle, Pocket Books, 1974; now in the thirty-sixth printing, he said preening), the characters all carry pocket computers that have a great deal of on-board capability and also link by radio to the rest of the world. These gadgets keep track of schedules, record conversations, and generally do the kind of management that makes life simpler.

Our book takes place in the far future; the fictional supercomputers have few limits on their performance. Back in reality, we ought to have about half that capability before the end of the century. Today, reasonably useful pocket computers are available, with more coming all the time; and thanks to Traveling Software, you can link them to your PC, meaning to the rest of the world.

The two leading pocket computers at the moment are Sharp's Wizard Electronic Organizer and Casio's BOSS (Business Organizer Scheduling System). Both are intriguing, although neither is what I'd like it to be; indeed, what I really wish is that I could combine features of the two.

Sharp's Wizard has the neat capability of accepting program cards, which lets third-party developers add features to the Wizard. It's slightly larger than the BOSS, and it makes good use of the extra space: there's a numeric keypad, and the function keys are very well labeled. On the other hand, the Wizard has a serious (some would say fatal) flaw: the alphabetic keys are laid out in ABCDEF fashion, so that people used to a typewriter find it between difficult and impossible to make entries on it.

Casio's BOSS, by contrast, has a QWERTY key layout; but, alas, there is no separate numeric keypad, and I find it extremely difficult to use as a simple calculator. The Wizard is very easy to use as a calculator. The BOSS's screen is a bit larger than the Wizard's, but despite the BOSS's contrast control, I find that its screen is not as easy to see as the Wizard's, no matter what the lighting. Neither has a backlit screen, of course.

Some of the calendar and schedule software seems subjectively easier to use on the BOSS than on the Wizard; and when you're on the road, it's a lot easier to get data into the BOSS than the Wizard. At home you use Traveling Software's link system to connect it to your PC and put data in that way.

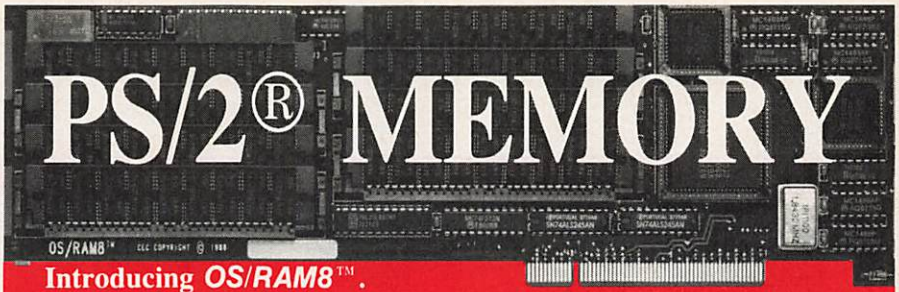
My—purely subjective—conclusion is that unless you're quite devoted to gadgets, you may not use either the Wizard or the BOSS; but if you are, you'll probably like either one. I'm mildly used to the Wizard and will probably go on carrying it; but I'm not sure, and besides, Roberta will probably inherit the BOSS, so we'll have that with us anyway.

One thing is certain: if you get either of these gadgets, get the Traveling Software link system for it.

Electric Chemistry

One of the most impressive educational programs I've seen was also on display at the National Education and Computers Conference. The Electric Chemistry Building package from Snowbird Software calls itself "a large-scale microworld simulation of a group of chemistry

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laboratories, each representing a major subdiscipline such as inorganic, physical, or organic chemistry." Each "laboratory" has various rooms, including a storeroom, the lab itself (complete with equipment and hoods and Bunsen burners), and a library.

The user interface is simple, if a bit cute: you use the arrow keys to move a block representing yourself through a vestibule into the laboratory. You can then go to the storeroom and get chemicals—only three at a time—and take them to the lab, where you can add them to a flask. You can then heat or cool the flask or go get more chemicals. Since this is inorganic chemistry, I wasn't able to make nitroglycerin.

The chemistry stocks are fairly complete compared to the top-of-the-line chemistry set I was given for Christmas. Anyway, you get your chemicals and go mix them. If you're a bit puzzled about some of the chemicals, you can look them up in the library. Once you start mixing, the program takes over and shows the result.

Sometimes there isn't a result, as when I put hydrochloric and nitric acids in with some mercury. However, you can also light the Bunsen burner under your reaction flask. I did, and sure enough, as the stuff got hotter, I got mercuric chloride.

The Electric Chemistry Building isn't as much fun as a real chemistry lab, because you can't do anything with what you make. I recall that we poured a couple of quarts of nitrogen tri-iodide into the manicured grass in front of Central High, so that we spelled out words; when the stuff dried, it gave off clouds of purple smoke and considerable heat, so that not only did "Go CBC" appear briefly in the smoke (for my high school alma mater, Christian Brothers College), but a week later the words were spelled in dead grass. Of course, that was a foolishly dangerous stunt, and I don't advise anyone to try it.

Like nearly all educational software, this one is copy-protected: they use the key-disk method, which is considerably more acceptable than one of the miserable schemes that partially reformat your hard disk. Educational software publishers tell me they have no choice: there are just too many teachers out there who persuade themselves their students "need" programs the school can't afford to buy. If the programs weren't copy-protected, they'd be distributed everywhere within a week of publication. Snowbird features a scheme whereby many students can use the program one at a time, each student having a disk to record results.

I haven't seen Snowbird's physical chemistry program. An organic chemistry program will be available in May 1990. I have been very impressed with the inorganic chemistry simulator.

Humit

Dr. Petr Beckmann is professor emeritus of electrical engineering at the University of Colorado, and he publishes one of the most interesting newsletters in the country: *Access to Energy* ($25 for 12 monthly issues). Fair warning: Beckmann is committed to both science and free enterprise. He is relentlessly logical and writes in a polemic style that spares no one. When he states a fact, it's a fact; when he catches an enemy in a falsehood or misunderstanding, he nails him.

A recent sample: "Like a rain dance that does not bring any rain, Bush's clean air proposals do have one characteristic that, in the dearth of positive features, deserves to be mentioned: they are not going to degrade the environment significantly." On ethanol as fuel: "If only 10 percent of U.S. fuel needed to be ethanol, the necessary corn would have to be grown on 500 million acres . . . a cool 105 percent [of the total arable land in the U.S.]."

Beckmann is a former resident of Czechoslovakia, the home of the original legend of the golem, which is likely why he calls his publishing venture The Golem Press. It has produced such works as *A History of PI* and *The Health Hazards of Not Going Nuclear*.

Now Beckmann has turned to software. The blurb for Humit asks, "Can you hum the Minuet of Mozart's 40th symphony? You will recognize it when you hear it, of course . . . but in the meantime, let your computer whistle it for you." Humit will do that; indeed, there are some 800 classical themes "from Bach to Dvorak." The musical quality isn't much because the PC isn't capable of much; but the tunes are definitely recognizable.

On the same disk are the Play and Whatisit programs. Play converts your PC into a keyboard instrument, sort of, with the middle row of keys corresponding to white keys, and the row above it to black. Whatisit does the same thing, except that if you can manage to play the first 10 notes of one of the classical themes in Humit, the program will tell you which tune you just played. At least it says it can do that. Since I can't possibly manage to play 10 consecutive notes and the program doesn't guess, all I got was a series of "Not on file" responses.

I don't quite know what to make of these programs. Humit does what it says it will, but I confess I wouldn't pay $60

continued

ITEMS DISCUSSED

Cardiovascular Systems and Dynamics.....$150
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Electric Chemistry Building
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physical $249.50
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all others $49.95
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Inquiry 984.

Mac Gallery $49.95
Dream Maker Software
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(213) 221-6436
Inquiry 985.

Northgate Universal Floppy Drive Controller $99
Northgate Computer Systems
13895 Industrial Park Blvd.,
Suite 110
Plymouth, MN 55441
(800) 548-1993
(612) 553-0111
Inquiry 986.

RBBS-PC in a Box CD-ROM $149
Quanta Press
2239 Carter Ave.
St. Paul, MN 55108
(612) 641-0714
Inquiry 987.

for it, especially since similar programs (though with far less of a library) are available on BBSes as shareware. On the other hand, it can sure startle someone to hear "The Ride of the Valkyries" burst out of Big Cheetah.

Beckmann's policy is consistent with his philosophy: to buy the program, you are supposed to sign a declaration that you undertake not to make copies for use by others (there is no copy protection), and when you bring up Humit, there's a not very subtle reminder of that. His pricing is predictable: Humit is available from The Golem Press (P.O. Box 1342, Boulder, CO 80306) at $60 for individuals, $120 for private corporations, and $240 for tax-subsidized institutions like governments and state universities.

Experts on Codes

The IDS NYCode Two is another program I'm not really competent to evaluate, since the heart of the program is a database of the New York State Fire Prevention and Building Code that comes on five disks. IDS has been developing programs for architects and builders for a number of years; I'm told they began with an Osborne computer and JRT Pascal. Most of their software is intended for use by municipalities, particularly building departments. Their two hottest items are IDS NYCode and IDS NYCode Two, the first being an expert-system program that asks the same questions about your building that a code official would ask when conducting a code review. It's written in Turbo Pascal.

IDS has other architect and contractor programs, including pcTRAQ: Building Permits, a database management program that generates information and reports about building permits; it's intended for use by a building department, and it generates the reams of forms and reports, like the monthly C404 Federal Bureau of the Census Building Activity Report. There's another program to handle property complaints.

Since until recently the New York Code wasn't indexed at all, and the index now provided by the state isn't very complete, IDS NYCode Two with its absolute index—every word except conjunctions and prepositions—makes access to the code fairly easy. I can't recommend what I don't understand; that is, the program works fine in that it lets you browse around the code and find anything you're likely to want, but I can't testify as to how complete it is, just as I can't of my knowledge tell you how well IDS NYCode simulates a building inspector. I like what I see, though, and if you're in the building business, you ought to be aware of this stuff.

Winding Down

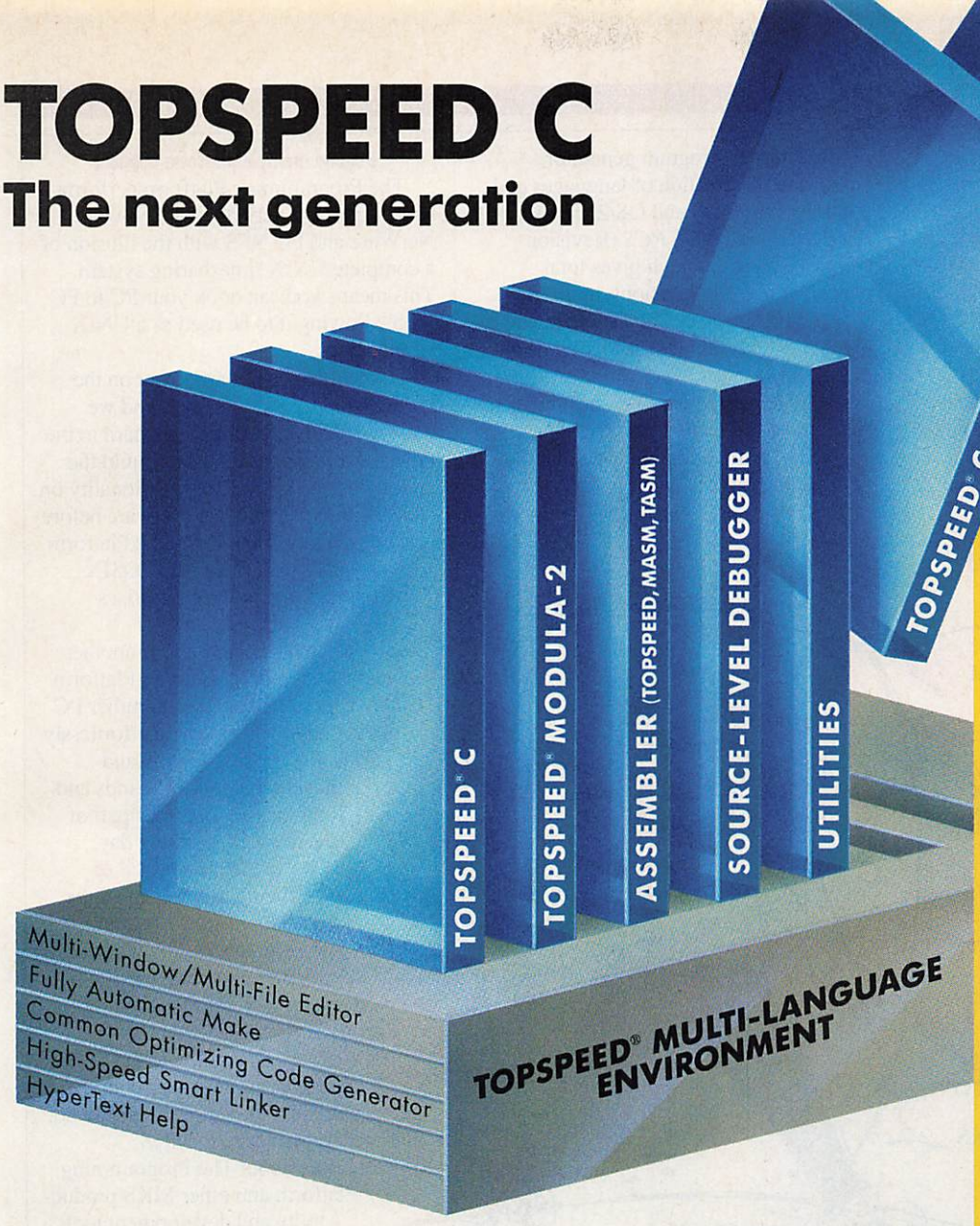
I'm out of space, and there's still a huge stack on my desk. I didn't get to Borland's Reflex 2, but if you have Reflex, you know how good that was; the upgrade is even better. There's Dream Maker Software's Mac Gallery, some 400 Macintosh clip-art images ranging from dinosaurs to Santa Claus, including a neat haunted house. It sure dresses up party invitations.

I have some new medical-simulation software from Learning Tools; their Cardiovascular Systems and Dynamics program is in use in about 200 medical schools, and by me it ought to be in all of them: students will learn more from experimenting with this than by cutting up animals, and it's cheaper to boot.

There are two books of the month: *Deception* by Edward J. Epstein (Simon & Schuster, 1989), perhaps the most important book I've read about international conflict since *Survival Is Not Enough* by Richard Pipes (Simon & Schuster, 1984); and *The Control of Nature* by John McPhee (Farrar, Straus & Giroux, 1989). McPhee writes about efforts to save New Orleans now that the Mississippi wants to wander elsewhere; cooling lava with fire hoses in Iceland; and flood control in the Los Angeles mountains. It's good classic McPhee, and as soon as I get this column on the wire, I'll finish it. While I'm at it, I'll open my split of champagne and munch on pâté with pumpernickel. ■

Jerry Pournelle holds a doctorate in psychology and is a science fiction writer who also earns a comfortable living writing about computers present and future. Jerry welcomes readers' comments and opinions. Send a self-addressed, stamped envelope to Jerry Pournelle, c/o BYTE, One Phoenix Mill Lane, Peterborough, NH 03458. Please put your address on the letter as well as on the envelope. Due to the high volume of letters, Jerry cannot guarantee a personal reply. You can also contact him on BIX as "jerryp."

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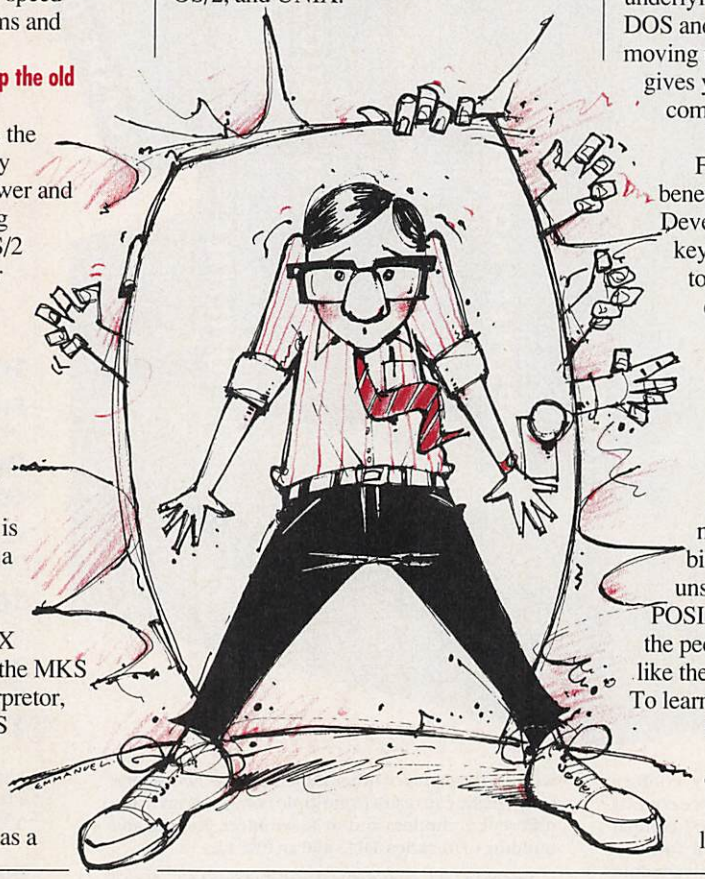
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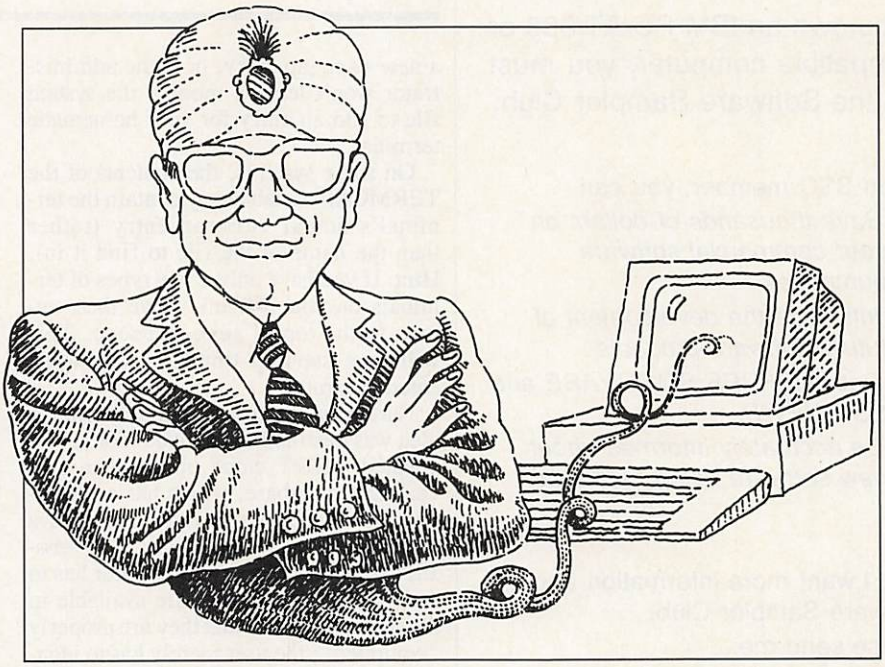
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Begin by finding out what you already have. Execute the command `env` (it may be `printenv` on some systems; `set` should also work, though slightly differently). This command displays a list of environment variables (which might be startling in its length) that you can set at any time. Application programs, including the shell itself, can read these variables and modify the way they operate as a result of the environment that you specify.

Often, the information about the environment variables is hidden somewhere deep in the Unix documentation. For example, if you read the manual page for the `lp` command carefully, you'll find a reference to the LPDEST environment variable. You can set this to designate *your* printer as the default printer, as opposed to the system default (which is set by the system administrator or print spooler administrator). You set it once when you log in and forget it.

Listing 1 is the result of running `env` on my system. It shows some of the environment variables that have proved useful for the programs that I run. Naturally, some of these reflect my personal taste (such as the contents of the EXINIT variable, which consist of the start-up commands for the vi editor).

More commands and programs than you might think check for the presence of such variables as EDITOR, MAILER, PAGER, SHELL, TERM, and TERMCAP. The first four of these inform applications of your favored programs for use as an editor, a mailer, a screen pager, and a Unix shell. Some people might prefer EMACS over vi as an editor, or `more` over `pg` as a paging program. While I generally use `csh` rather than the standard Bourne shell, the SHELL variable is generally used when "escaping" out of a program, and at such times I don't want the extra overhead time of starting up `csh`, so I specify the Bourne shell instead.

Why They Call It Curses

If you're new to Unix, you might have a bit of a problem running screen-oriented programs. Unlike a personal computer with its own dedicated screen software, a Unix system can have almost anything plugged in as a terminal. To answer the problems of running screen-oriented programs in a world of variable and unknown screen controls, a standard set of terminal-independent driver routines, known as the curses library, exists. The idea is to define a specific terminal's capabilities and to control the codes to a curses-compatible program. The terminals are described in the `/etc/termcap` file. Many Unix and most Xenix systems use the name `ansi` to refer to the console on an IBM compatible; this can generally be used by IBM PC users dialing into a Unix machine.

The TERM variable should contain the proper name for your terminal; the TERMCAP variable generally should contain the name of the `termcap` file. While (as noted above) this is generally the system file `/etc/termcap`, you can also make it point to the name of your own file. This is useful if you are testing

continued

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Listing 1: *The* env *command lists all your environment variables and their values.*

```
EDITOR=/bin/vi
EXINIT=set beautify nomesg showmode wm=6 ai shell=/bin/sh|ab u UNIX
LPDEST=oki
MAILER=mail
NAME=David Fiedler
ORGANIZATION=InfoPro Systems, publishers of ROOT and UNIQUE
PAGER=less
PATH=:/bin:/usr/bin:/usr/games:/usr/local:/usr/lbin:/own/david/bin
ROGUEOPTS=jump,autorun,flush,noterse,fruit=prune,name=Fafhrd
SHELL=/bin/sh
TERM=ansi
TERMCAP=/etc/termcap
```

a new termcap entry, or if the administrator won't let you modify the system file to add an entry for your homemade terminal.

On some systems, the contents of the TERMCAP variable may contain the terminal's actual termcap entry (rather than the name of the file to find it in). Hint: If you have only a few types of terminals on your system, move their entries to the top of /etc/termcap. This will save start-up time for screen-oriented programs.

Naturally, such a beautifully simple idea was destined to be made more complicated. AT&T came up with its own terminfo database, which has each terminal's termcap-type information in a separate file under the /usr/lib/terminfo directory. The administrator has to make sure that the files are available in the right places and that they are properly "compiled"; the user merely has to identify his or her terminal to the system with the proper name using the TERM variable. This design for terminal information loads more quickly than termcap entries but is more difficult to set up and maintain.

Setting Environment Variables

Let's say you're ready to actually do some of this. If you're just sitting at the regular Bourne shell prompt ($), then you can simply type

```
TERM=foobar
```

and the contents of the TERM variable will be set to the string foobar. You can verify this by typing set.

But wait! The value will *not* be automatically inherited by other commands spawned from this shell. To prove this, type env, which prints the values of the variables actually set in the environment. It will show your TERM variable as still set to "ansi" (or whatever it was previously). To reflect your change in the shell's environment, you must explicitly export it:

```
export TERM
```

Now when you type env, foobar will show up as your TERM type. This little exercise is meant to show how important it is to remember to export all the changes that are made to the Bourne shell environment.

Setting the variables is usually relegated to your session initialization when you log in. If your default shell is the Bourne shell, then you put the desired commands in your .profile file in your home directory, like this:

```
PATH=$PATH:/u/david/bin
TERM=ansi
NAME="David Fiedler"
PAGER="more -c"
LPDEST=laser
export PATH TERM NAME PAGER\
  LPDEST
```

If your default shell is the Berkeley/C shell (%), then you put this in your .cshrc file:

```
setenv PATH "$PATH":\
  /u/david/bin
setenv TERM ansi
setenv NAME "David Fiedler"
setenv PAGER "more -c"
setenv LPDEST laser
```

(C shell users also have the option of creating both .login and .logout files, which are executed when you log in and out, respectively.)

Notice that strings with spaces in them have be surrounded with the double-quote character. Also notice the syntax of the first line, which takes the current default value of PATH (the system's idea of the order of directories to search for executable files) and tacks on a reference

continued

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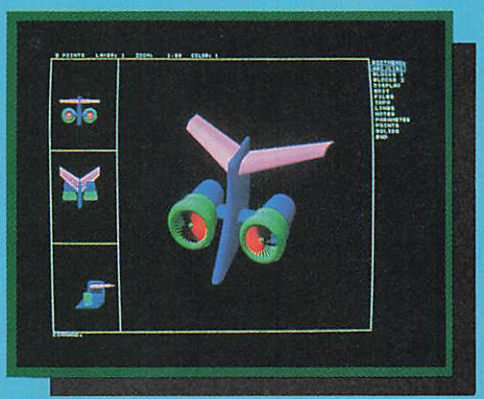
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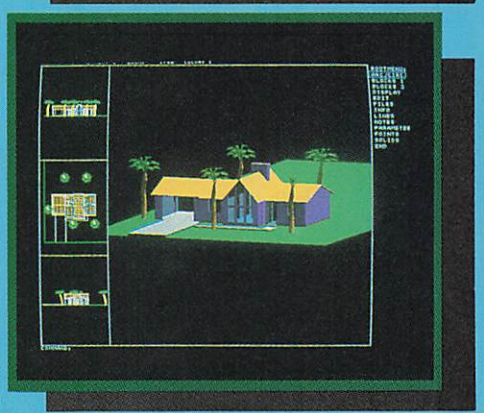
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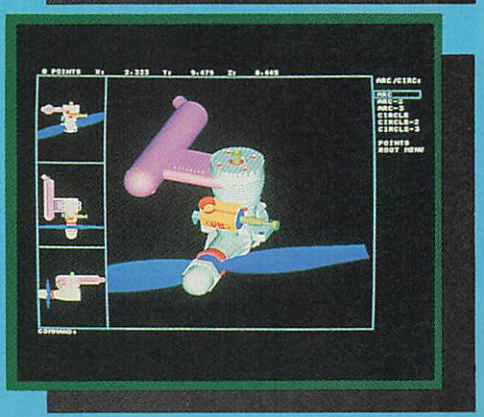
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to the /u/david/bin directory at the end.

In this way, I can add commands to my own private directory at any time, and they will be executed just like system commands. A colon is used to separate directory names, and two colons (or a colon as the first character after the equals sign) means "search the current directory now."

System Administrators and the Environment

You can use many of these same ideas as a system administrator. For instance, if you wanted to add another directory or two to the default search path, you would just do this in the one place where users will execute it when their shell starts up: in the /etc/profile file, which is examined *before* the user's own .profile. I suggest that you name the full directory path to be searched, just to avoid any confusion:

```
PATH=/bin:/usr/bin:/usr/local::
PAGER=more
TZ=PST8PDT
export PATH PAGER TZ
```

A similar entry must be made in /etc/cshrc for the C shell users. All systems should have at least one directory for "home-grown" commands (/usr/local in the example above). This makes it easy to keep them separate for backup and maintenance purposes. And this directory should appear in the search path *after* the system directories, to prevent confusion in case someone names a local command the same as a system command.

Why did I set PAGER and TZ above? The PAGER variable will allow certain programs to use the more command when it's necessary—something that unsophisticated users will thank you for. And explicitly setting the TZ variable (to whatever your local value should be) will prevent certain time-related bugs from appearing. Setting other variables can also save you a great amount of user support time; think of how you can set EXINIT to some reasonable defaults, for instance.

The "search current directory now" feature mentioned above should be *turned off* when you are logged in as root, since it makes the "Trojan Horse" security hole possible. You just explicitly change this in the /.profile file (root's initialization file), and while you're at it, you should add the /etc directory to root's PATH to make your life easier. Some versions of the C shell take care of both of these security measures automatically.

Me and My RC

Just as each user has a file that is executed when he or she logs in, so the system has a way of changing its default behavior when it's booted up. The system executes the /etc/rc file when it first comes up into multiuser mode. For years, this has been the place to put system-specific code (e.g., loading special device drivers at start-up). If you're running into strange problems with a new system, it doesn't hurt to make sure that this file is setting important environment variables properly. Things like TZ, PATH, HZ (do *not* set this to your powerline frequency!), and even SHELL can be set here for the system.

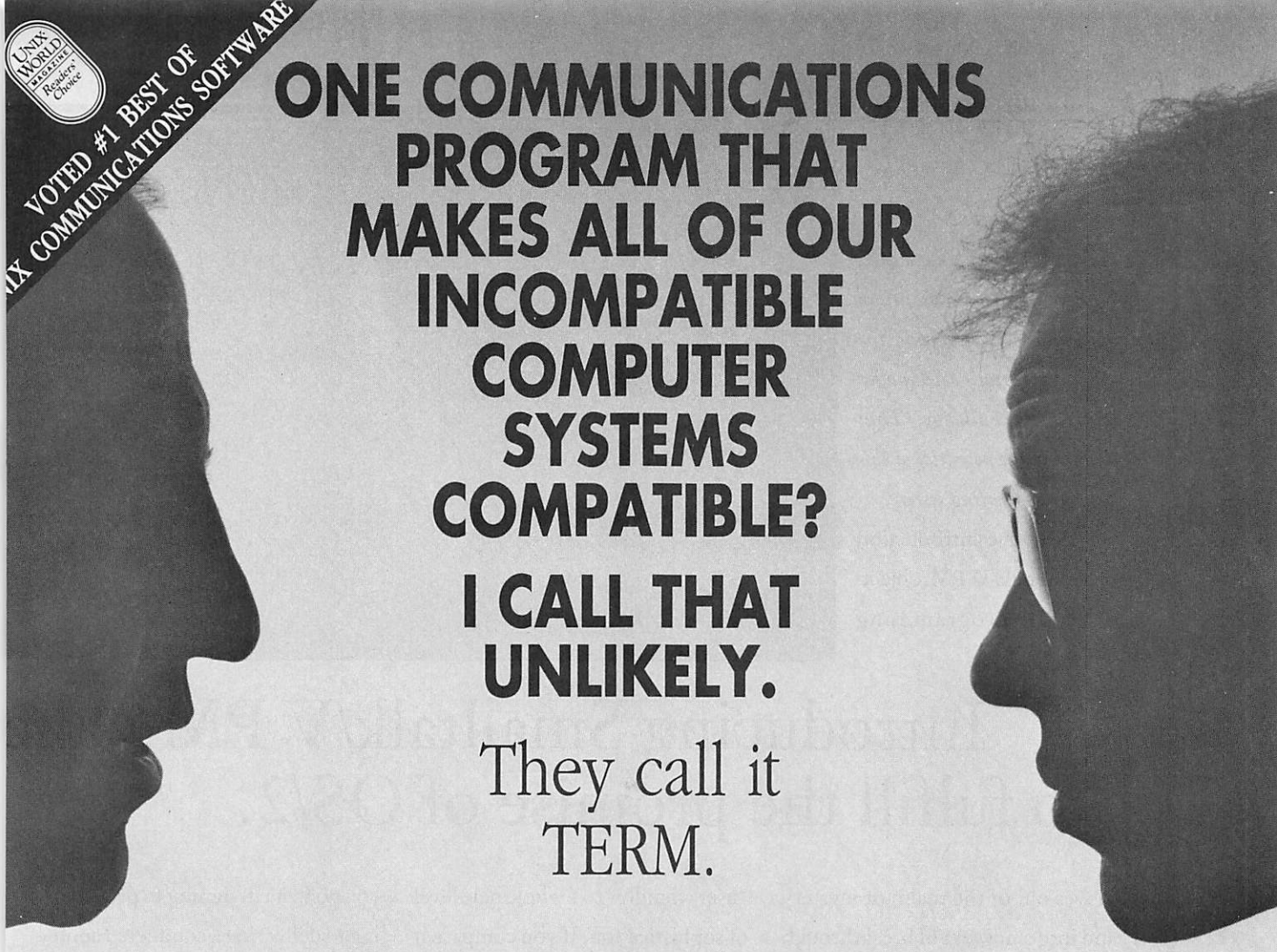
Setting variables can save you a great amount of user support time.

In the most recent releases of Unix, /etc/rc does little more than go into a set of numbered subdirectories under /etc/rc.d and execute all the files it finds. Each of these directories has a designated function. But you find that the file /etc/rc.d/8/userdef has been reserved just for you!

The only thing left to do to customize the system is to set up the cron facility using the /usr/lib/crontab file (on newer systems, this is now a set of files in the directory /usr/spool/cron/crontabs) for events that should repeat at specific times. If you're running UUCP (Unix-to-Unix copy), make sure that at least one of the daemon programs found in the /usr/lib/uucp directory is being executed once per hour or so, or your E-mail may never get sent. ■

David Fiedler is editor and publisher of the Unix newsletters Unique *and* Root *and coauthor of the book* Unix System Administration. *He can be reached on BIX as "fiedler."*

Your questions and comments are welcome. Write to: Editor, BYTE, One Phoenix Mill Lane, Peterborough, NH 03458.



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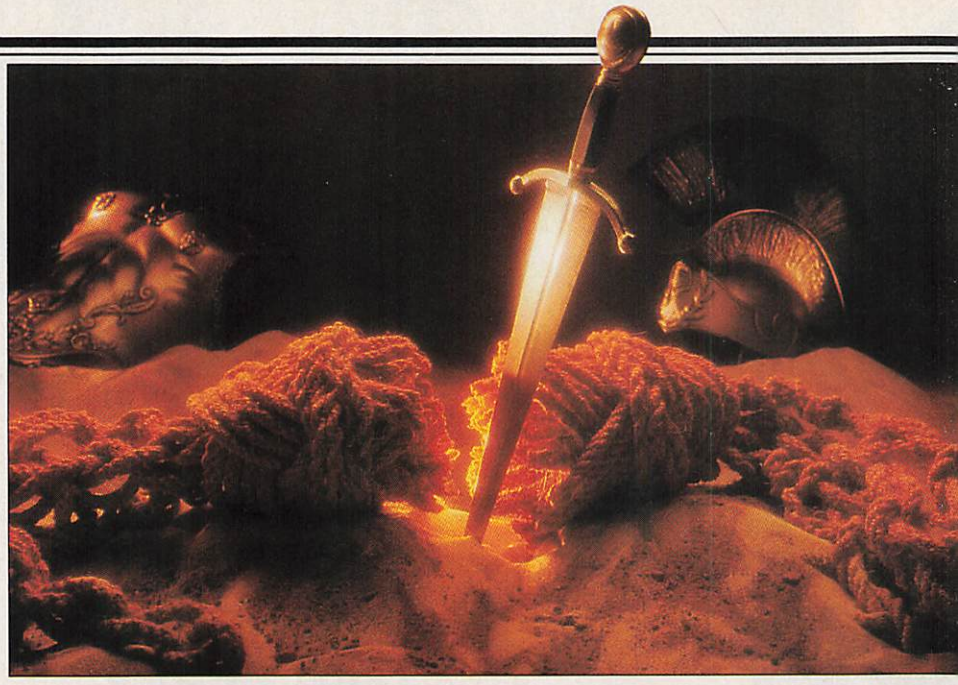
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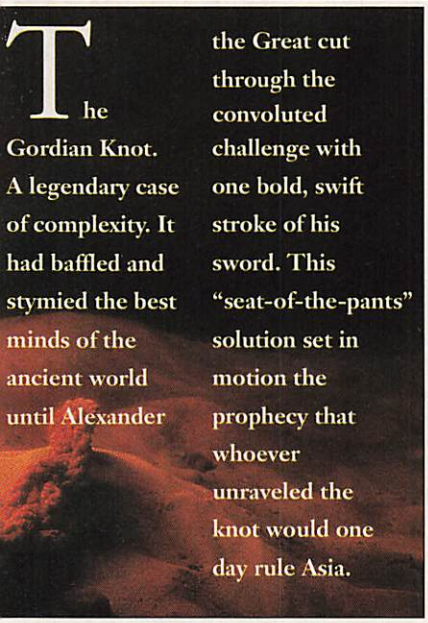
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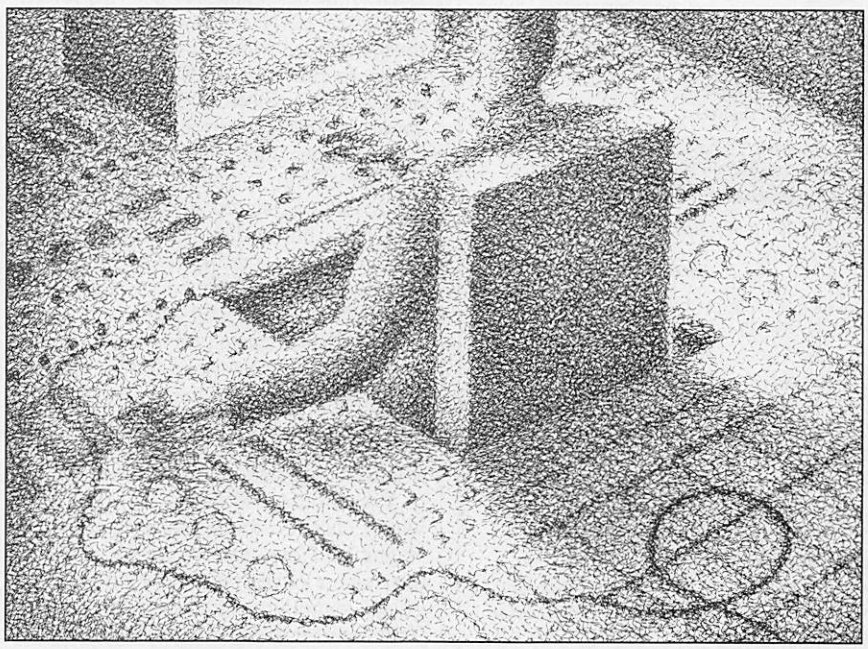
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SERVING BUSINESS

Networks let dedicated database servers bring SQL power to personal computers



In last month's column, I discussed the role that IBM's OfficeVision and Systems Application Architecture (SAA) will have in the corporate world. As you will recall, IBM's plans for your future are based on a mainframe acting as a Structured Query Language server. (SQL is a "truly" relational database system tracing back to circa 1970 IBM.)

This solution works, of course, only if you have such a mainframe. Although IBM will be pleased to sell you one, for many small businesses this just doesn't make sense.

What *does* make sense is to use the guts of SAA—that is, the user interface and the SQL server—without using SAA itself. This way, you can still have the communications, the data handling, and the centralized data storage, while using equipment that may otherwise meet your needs a lot better.

Serving You Right

In essence, the corporate database is simply a collection of information. Many companies place this information on a mainframe. This decision is often made more for reasons of capacity and security than for performance. Company data is much of what makes the company, and it must be protected.

With the maturing of LANs, these same benefits can now extend beyond the mainframe world into the realm of the personal computer. This is made possible by the introduction last year of SQL database engines that reside on dedicated database server machines attached to the networks. No longer is database work on microcomputers restricted to a single machine. The database software waits for the workstation software to ask it for a task.

As a user, you may never know that there is a SQL (pronounced "sequel") server out there. The workstation software presents the screens, performs initial edits, and validates entries. Once the user of the workstation software completes a screen, that screen is changed into a SQL query, which is then sent down the LAN to the database server. The server, in turn, finds the requested information and returns the results to the user.

This method of working has two advantages. First, it reduces the workload on the workstation, allowing that computer to be less powerful and, therefore, less expensive. Second, it also reduces traffic on the LAN significantly over software such as dBASE, which requires data, not just commands, to flow both ways.

The SQL Approach

The past year has seen the development of several SQL database server products. All offer the same flexibility IBM offers in the SAA world. The difference is that they don't require IBM hardware. Each product approaches the task of being a SQL server in a slightly different way.

Gupta Technologies' SQLBase server, for example, will work with nearly any network. Gupta also makes other software that provides connectivity to mainframe SQL databases and other external database products. Gupta gives you a complete solution.

Microsoft, on the other hand, offers only the database engine—that is, the part of the SQL server that actually receives queries and provides answers. Other companies, including Ashton-Tate, provide the front end that allows the database engine to be used.

Novell even manages to do without the dedicated database server. Its database

continued

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server product runs as an additional process in the file server and supports the data files there. This has the advantage of not requiring you to buy a separate machine for the database server, but it does add an additional load to the file server, which can be a problem in the case of a busy LAN where there is a lot of disk activity. In that instance, you might find yourself waiting for your database query while someone else plays Novell's SNIPES game.

Competing with SAA

Each of the three approaches will work to support a LAN with workstations that must share information for their applications. In the case of Novell's NetWare SQL and Microsoft's SQL Server, that's about all you can do right now. Gupta Technologies has provided capabilities that come close to competing with SAA. Microsoft has stated its intention to do this, also, but to date, the software support is lagging, and Microsoft's LAN restrictions make an immediate remedy for this unlikely.

Gupta has arranged for a variety of options for the user interface and for applications interfaces. This means you may be able to use all or most of your current application, or you can design a Microsoft Windows application that can be upgraded to Presentation Manager (PM). Gupta wisely chose to make arrangements with Nantucket Corp. and Wordtech Systems, the makers of the two major dBASE language compilers, to create workstation front ends for its SQL engine.

Gupta was likewise perceptive to choose Microsoft Windows as its graphical user interface. This gives SQL users a path to the future with a DBMS that's available now. Unlike much of what is planned for SAA, you can run Gupta's SQLWindows under MS-DOS on IBM PC AT–class machines that you already have. You don't need to wait for IBM or anyone else to deliver on promises in the coming years.

Gupta says that its Windows product will be upgradable to PM in the future. Whether that will ever happen remains to be seen, but it seems likely. Gupta is already working in the OS/2 environment with its database engine, and the company seems to understand the operating system.

What Gupta means is that the applications created by using SQLWindow's fourth-generation language will be upgradable to OS/2. Gupta's language for use with its database server is unusually complete, allowing users to create the full range of Windows screen devices. In other words, you can have dialog boxes and radio buttons to your heart's content.

Microsoft's Contribution

Microsoft has taken a different tack in the effort to bring a SQL server to market. Instead of designing the user interface itself, the company has arranged with Ashton-Tate and Borland to create versions of their DBMS products that will work with SQL Server. These products are expected around the end of this year.

In the meantime, SQL Server suffers

continued

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SQLBase
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from some significant limitations. Because of Microsoft's approach, few development tools are available now. If you plan to do work with SQL Server, you'd better plan to be a C programmer. While this might be acceptable for new project development, conversion of mainframe systems to work with a SQL server usually involves the use of COBOL, and that's not something that is well supported by Microsoft.

Perhaps more critical, Microsoft's SQL Server works only with Microsoft's LAN Manager. Considering that network operating system's minor position in the LAN marketplace, the limitation can be crippling. The majority of LAN installations (approximately 60 percent, according to a BYTE survey) are running Novell NetWare. Most of the rest are running 3Com.

In its current incarnation, Microsoft's LAN Manager is a poor choice, both because of its limited use and because of its significant security problems. While this may change someday, it's unlikely that moving this way now would be a wise business decision.

Novell's Dual-Purpose Server

If you already have a Novell LAN and it's not heavily taxed, Novell's NetWare SQL will save you the cost of another machine. This is because it runs as a value-added process in the file server itself.

That means, of course, that you can't use any other network operating system besides NetWare. It also means the file server will have to split its time between serving files and serving the database.

To make matters even less attractive, you have very little choice of how you will use the database server. Wordtech Systems has a version of its DBMS software that will work as a front end, but you'll have to program it yourself.

Gupta's language for use with its database server is unusually complete.

Wordtech's Role

Wordtech Systems doesn't sell a SQL server product, but it has found a way to provide workstation software that will use the dBASE programming language and still work with SQL databases. Because Wordtech's products allow the creation of some very acceptable user interfaces, and because dBASE programmers are easier to find than C programmers, this makes system implementation easy to accomplish. In addition, conversion from applications written for dBASE is simplified.

At this writing, Wordtech's products are in the final testing stages. They should be released by the end of the year.

A Replacement for SAA?

As you can see, none of these solutions is as well integrated as IBM's SAA is supposed to be. On the other hand, at least some of it is available now, and none of it requires you to buy an IBM mainframe or minicomputer. If your business is based on personal computers or on a non-IBM minicomputer, at least you have the option to gain most of the benefits that IBM promises. You will have to do more work, of course, but you won't have to run a mainframe, and that's a considerable savings in hardware and personnel.

At this point, the only realistic solution to the needs of a business that is moving to SQL is Gupta's SQLBase. For one thing, it's a complete solution. You don't have to wonder when your user interface is going to be available. For another, it allows great flexibility in the operating environment, supporting an AT-based database server on the low end and IBM's DB2 on the other. In other words, you can use the low-cost solution even if you *do* eventually end up in the IBM mainframe world. ■

Wayne Rash Jr. is a contributing editor for BYTE and a member of the professional staff of American Management Systems, Inc. (Arlington, VA). He consults with the federal government on microcomputers and communications. You can contact him on BIX as "waynerash," or in the to.wayne conference.

Your questions and comments are welcome. Write to: Editor, BYTE, One Phoenix Mill Lane, Peterborough, NH 03458.

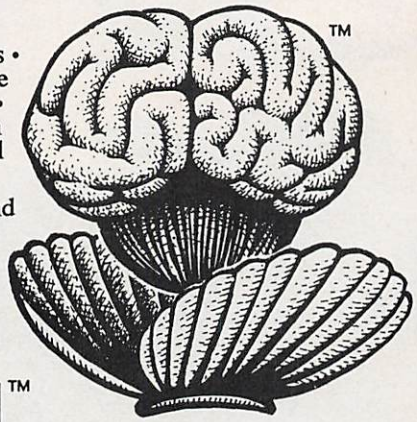
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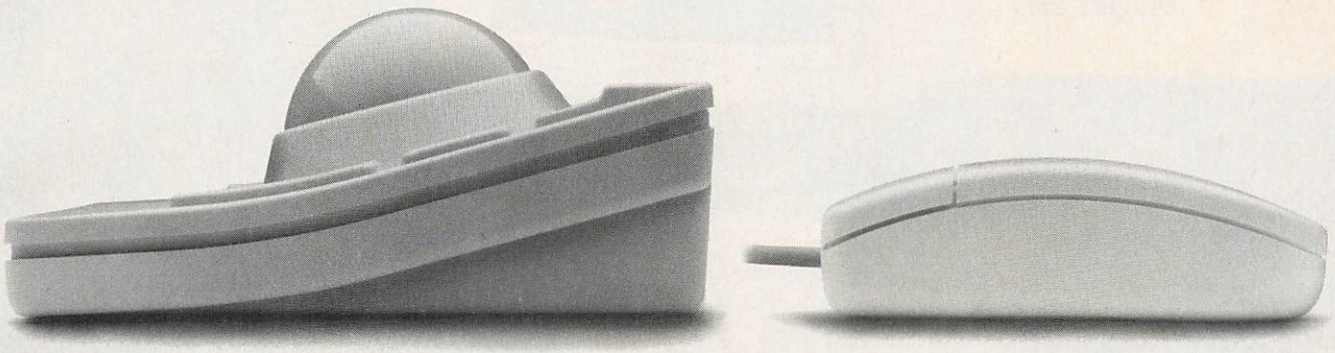
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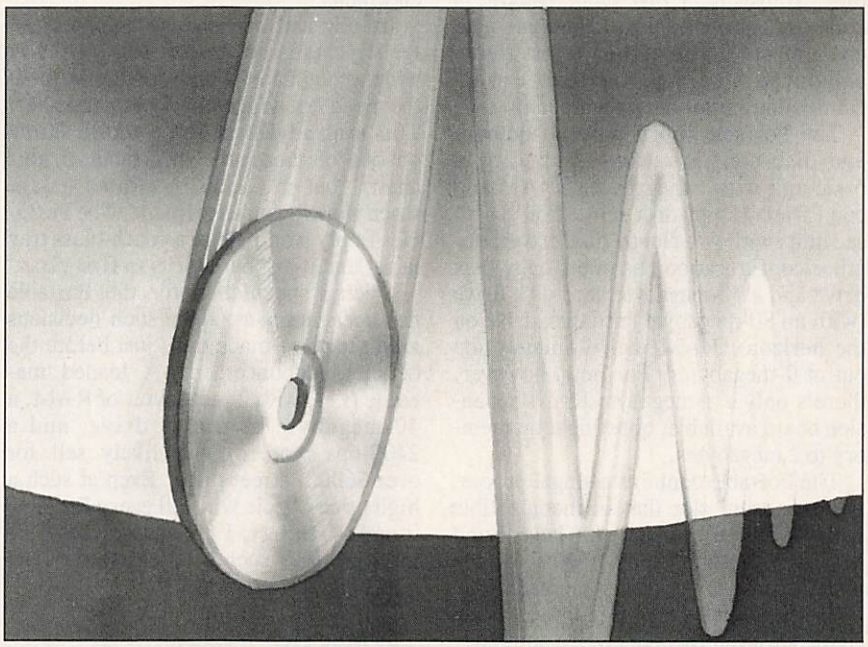
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RESEARCH À LA MAC

Apple aims at the scientific research market and announces two new Macs



Apple has always had an affinity for the higher education and scientific research community. The Apple University Consortium, a group of prestigious U.S. universities, has been an important Apple partner, even before the introduction of the Macintosh. If it weren't for the AUC's early adoption of the Mac, Apple would have pulled the plug on the machine by 1985. Sales of Macs to AUC members and the AUC's work in developing new software and hardware for the Mac have fostered much of the Mac's acceptance in business environments.

A current reminder of just how closely Apple works with the AUC members is the Apple Science CD, volume 1. This CD-ROM disk was previewed at the annual AUC meeting in July and is available at no cost through Apple's higher education sales representatives to any researchers and teachers interested.

The CD contains over 500 megabytes of scientific data covering hundreds of different scientific phenomena, including atmospheric and weather information, astrophysical data, biomedical data, scientific images, animations, and dozens of simulations.

It also has the complete suite of data-visualization and data-analysis tools developed by the National Center for Supercomputer Applications (NCSA) at the University of Illinois. Analysis software from the National Institutes of Health completes the disk. These tools let you take apart the data on the CD and demonstrate techniques to your colleagues. Also, you can use data-visualization methods that make it easy to "see" trends in the data that numerical methods alone often miss.

The value of the Apple Science CD lies in the "realness" of the data, making it an amazing teaching resource. You can now *see* what happens when a hurricane comes ashore, or what happens when two large air masses collide over land, or what happens when a star burns out. The Apple Science CD includes data for these events and many more, plus a series of simulations and animations that have been constructed based on direct measurements. It even has three-dimensional renderings that almost come alive when you view them with a standard pair of red/blue three-dimensional glasses.

The data on the disk was collected over a four-month period from research scientists across the country. The Apple Science CD owes its existence to several people, including Kurt Schmucker and Rob Wolf, research scientists at Apple; Brand Fortner, manager of applications software at NCSA; and Katie Povejsil, manager of academic solutions at Apple.

The Apple Science CD is Apple's third major CD-ROM disk. The first two, the Apple Education CD sampler and Phil and Dave's Excellent CD, are good examples of how important CD-ROMs can be to the Mac market. They remind us that desktop media and multimedia authoring *need* a source of high-quality images and sound, and CD-ROM disks are an inexpensive way to fill that need.

Apple covers a lot of ground with the Apple Science CD and deserves major-league kudos for distributing this resource for free. We should thank those involved in its production for having the foresight and guts to pull this off, especially in such a short period of time. I can't wait until volume 2!

The Soul of the New Machines

I can now talk about the two new machines that Apple announced in September, both of which I've used extensively

continued

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in prerelease versions.

The first machine is the Mac Portable. The Portable is a new "design center" for Apple; that is, it uses new components configured in new ways and manufactured on new factory lines. Unless you've been in a cave for the last year, you've probably got the basic specifications for the Portable memorized: a 16-MHz 68000-based machine of the familiar laptop/clamshell configuration made famous by Zenith and Toshiba. The Portable includes a fancy active-matrix LCD (where each pixel is controlled by a separate "transistor") that's not backlit, a keyboard, and a trackball (you can also use a mouse). The keyboard and trackball can be repositioned in the case to accommodate right- or left-handed users.

The Portable sports several memory and disk configurations, including a basic unit with 1 megabyte of RAM and one FDHD floppy disk drive. You'll also see units with two floppy disk drives; another configuration has one floppy disk drive and a 40-megabyte hard disk drive (with an 80-megabyte hard disk drive on the horizon). RAM will ultimately top out at 9 megabytes. For now, however, there's only a 1-megabyte RAM expansion board available, boosting total memory to 2 megabytes.

The Portable contains a single processor expansion slot that is incompatible with NuBus or the current Mac SE and Mac SE/30 slots. Apple seems to love mangling its own bus standards. The Portable includes the usual ports: one Apple Desktop Bus port (e.g., for external keyboards, mice, and *x,y* digitizers), two serial ports, a SCSI port, and a sound port. A 2400-bps internal modem will be an option.

Apple built the Mac Portable with the smartest power-management circuitry I've ever seen. The lead-acid gel battery in the unit I used could run the Portable for over 8 hours, unless you're doing constant disk updates. The power pack continuously monitors the state of the Portable, turning off unused components. It also acts as a power filter/surge protector. Unfortunately, the power pack is also an integral unit; you can't separate the battery from it to save weight. This means that the Portable must have the power pack installed even when the machine is using wall current.

With a 40-megabyte hard disk drive and 2 megabytes of RAM, the Portable checks in at over 15 pounds, a lot to lug around an airport. Still, it's not as heavy as some of the Zenith behemoths I've carried, like the Z-183 and the TurbosPort 386. Compared to the NEC UltraLite, the Zenith MinisPort, or the Toshiba T1000, though, the Portable seems enormous.

Even at a price over $6000, Apple will sell every Portable it makes.

Its physical dimensions heighten the feeling of largeness, because it's actually wide enough to fit on your lap without the need to wire your knees together. This is an advantage when you're sitting on one of those uncomfortable airport chairs, but it's a distinct disadvantage when working on an airplane. The Portable simply won't fit on a coach-class tray table, and it just barely fits in first class.

Pricing speculation for the Portable has been rampant, since such decisions aren't usually made until just before the official announcement. A loaded machine (i.e., with 2 megabytes of RAM, a 40-megabyte hard disk drive, and a 2400-bps modem) will likely sell for over $6000, street price. Even at such a high price, Apple will sell every Portable it makes. In fact, I'd be surprised if the machine isn't such a hit that orders get backlogged right away.

The Mac IIci

The other new Mac is the 25-MHz IIcx, called the IIci. This machine is the second small modular-design-center unit. The IIci includes built-in 1-bit and color video on the motherboard, so you don't have to buy a NuBus video card to drive a monitor. New ROMs and custom application-specific ICs complete the revamped motherboard, which uses considerably more surfaced-mounted components than the Mac IIcx, making it a reliable design.

Otherwise, the 25-MHz IIci should be similar to the 16-MHz machine. It incorporates the usual ports and an FDHD floppy disk drive, along with room for an 80-megabyte internal hard disk drive (larger hard disk drives are on the way). Three NuBus slots complete the system.

Pricing for this fastest Mac is completely up in the air, since it's likely to poach sales from the existing Mac IIx and IIcx configurations, not to mention the Mac II. The figures being tossed about as I write this in July are 15 percent higher than the IIcx. If those prices hold, most Mac II buyers will opt to buy the IIci, since it is noticeably faster at almost every computing task you throw at it. Spreadsheets update faster. Word processing documents open, close, and scroll faster. Multiple applications can be serviced faster under MultiFinder. You'll find the performance improvement of the IIci over the IIcx and IIx to be much more noticeable than you'd think.

The Mac Product Line

With the release of the 25-MHz IIci, the older Mac II becomes a product-line luxury. Since it costs more to manufacture than the IIx or IIcx while coming in last in the performance derby of Mac IIs, the Mac II is expendable. Apple is likely to cease manufacturing the Mac II this year, if it hasn't already.

What about the compact Macs? The SE/30 is a big hit. It packs a lot of computing punch and RAM capacity into a small box for a good price. Apple will surely keep it around for some time. The company might consider goosing its speed by going to a 25-MHz 68030, but I doubt that will happen for a while.

The Mac Plus is a different story. The Plus is a tired design that's a pain to manufacture and service. With System 7.0 on the horizon and requiring 2 megabytes of RAM just to boot, the basic 1-megabyte Mac Plus seems like an antique. I had considered the Mac SE to be in the same boat as the Plus, but in August Apple reduced the SE's list price by $300, while adding the FDHD floppy disk drive as standard equipment. It's the first time I've seen Apple both lower a price and add a feature to the same Mac, so it seems the Mac SE will stay around.

As happened with the Apple II, though, I can see Apple continuing to manufacture the Mac Plus well into 1991, unless it builds the Mac Classic. As long as this machine is a cash cow that isn't stealing sales from the higher-end Macs, Apple would do well to keep cranking it out, especially for the student market. This is a market where word processing and programming needs don't argue for virtual memory, blinding speed, and giant hard disk drives. ■

Don Crabb is the director of laboratories and a senior lecturer for the computer science department at the University of Chicago. He is also a contributing editor for BYTE. He can be reached on BIX as "decrabb."

Your questions and comments are welcome. Write to: Editor, BYTE, One Phoenix Mill Lane, Peterborough, NH 03458.

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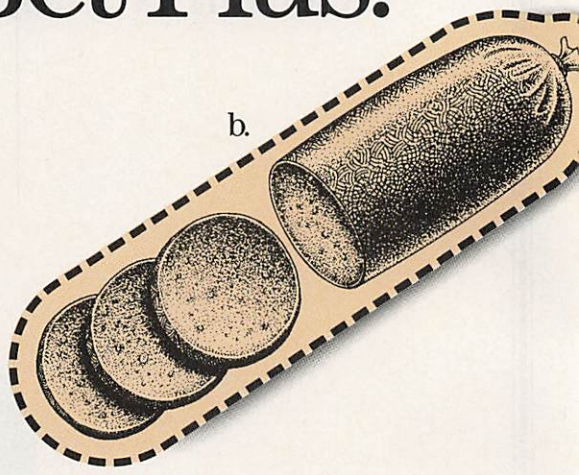
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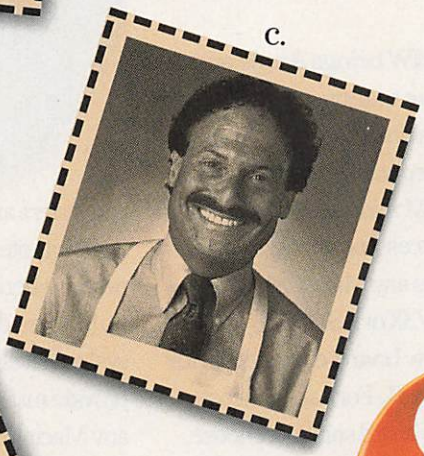
a.



b.

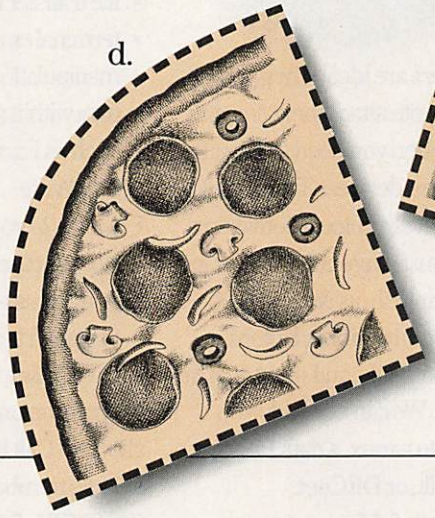


c.



Actual Scanned Images.

d.





1. Cut out the photo and illustrations on the left.
2. Put that dull, wordy document down in front of the boss.
3. For the clincher, lay the graphic elements in place.

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a.

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b.

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c.

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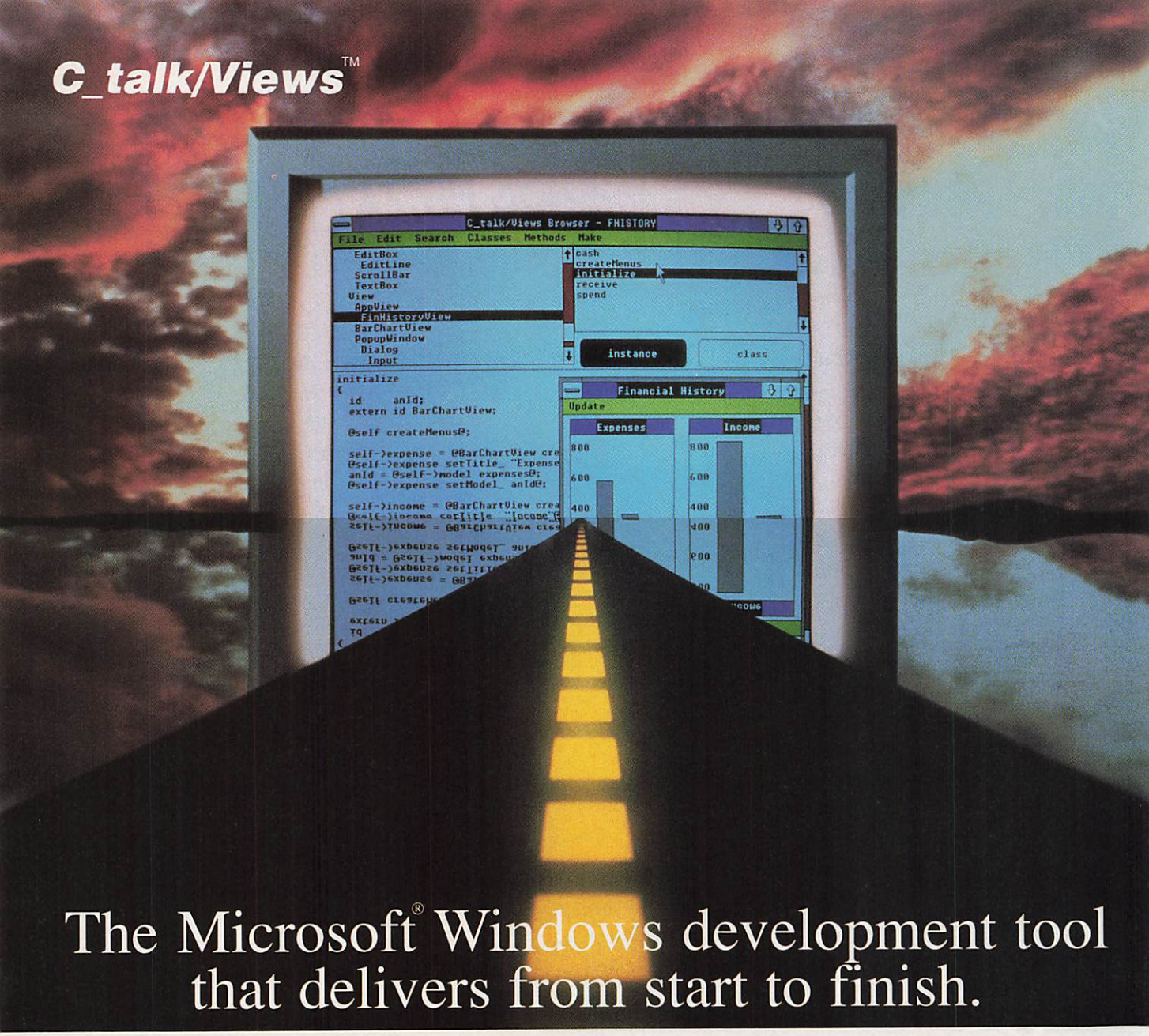
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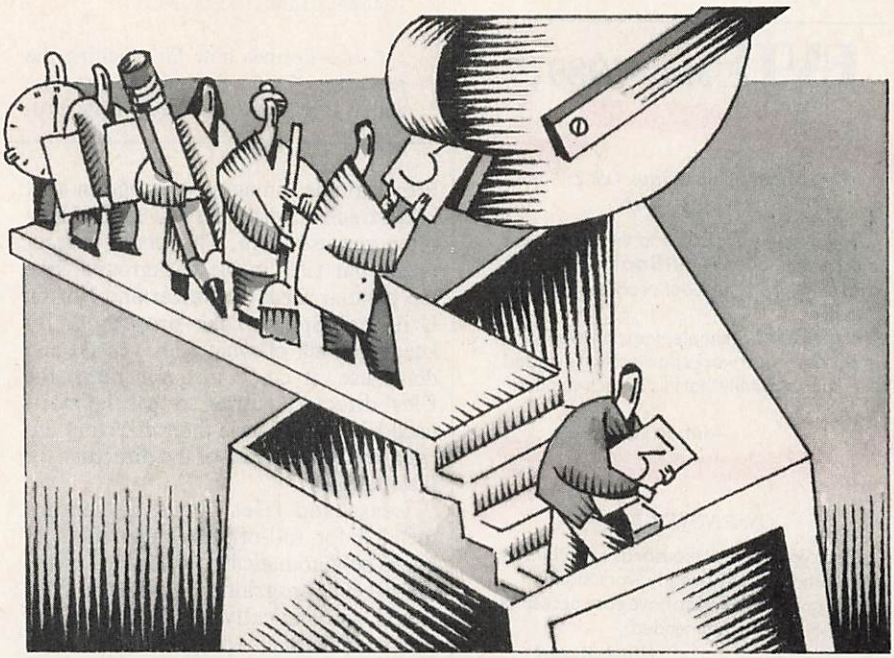
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GETTING YOUR PRIORITIES STRAIGHT

How to fine-tune OS/2's multitasking behavior with the use of time slicing



How does OS/2 manage to do several things at the same time? Of course, no single CPU can truly do multiple things simultaneously; it just fools you into thinking that it can by quickly switching from task to task. And therein lie some subtleties I've recently been exploring.

Trickery

There are actually two parts to the trickery: peripheral scheduling and time slicing. Peripheral scheduling works for the most part by exploiting the tremendous differences in speed between a CPU and its peripherals.

Time slicing is concerned with how the operating system doles out CPU time among computer tasks, and this will be the focus of my column this month. I'll take up peripheral scheduling in another column.

Here, I'm concerned with CPU-bound programs. Programs are generally constrained by a single item in the computing system. The print-formatter programs found in word processors are held up by printer speed. Thus, these programs are print-bound—no matter how fast the computer is that they're running on, they'll run only at the speed of their printer.

Database managers like dBASE spend most of their time waiting for the disk drive. Run dBASE from floppy disks, and it's not much faster on an 80386 than on an IBM PC XT, which makes it disk-bound.

A Lotus 1-2-3 recalculation, on the other hand, isn't waiting for the disk or the printer. It's merely directing the CPU to pick up numbers, perform mathematical operations on them, and put them back. In other words, it's CPU-bound.

Consider a simple case of two such CPU-intensive programs. You want two spreadsheets to appear to recalculate simultaneously on a computer. All you need to do is give a little time to spreadsheet program 1, a little time to spreadsheet program 2, a little more time to program 1, and so on.

In "OS/2's Multitasking Dashboard" (November 1988), I discussed how the length of "a small amount of CPU time" affected OS/2's performance. That span of time is called a time slice, and its duration can be set with a CONFIG.SYS command called `timeslice=nnn`, where *nnn* is a value in milliseconds (32 ms minimum).

A little experimentation that I did in that column suggested that a time slice of about 512 ms—about one half of a second—seemed about right for maximum throughput.

Priorities

Once you've set the time slice to one half of a second, spreadsheet program 1 gets one half of a second, spreadsheet program 2 ditto, back to spreadsheet program 1, and so on. Is this necessarily the way you want it? Not in most situations. Some jobs are more important than others, and they should get a greater proportion of the CPU's time. That's why OS/2 includes the notion of *priorities*. Each OS/2 task has a two-part priority value: the priority *class* and the priority *delta*.

There are three priority classes, numbered from 1 (lowest) to 3 (highest). Most OS/2 applications run at number 2 because it's the default class. Number 3 is the time-critical priority.

Number 1 is for jobs that should run only when nothing else wants the system.

continued

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Setting Task Priorities with DOSSETPRTY

As explained in the text, OS/2 programs can instruct OS/2 to increase or decrease their execution priorities with an OS/2 entry point (application programmer interface) called DOSSETPRTY:

```
ret_code=DosSetPrty
(Scope,Class,Delta,PID)
```

`Scope` defines how far-reaching the request is: 0 (just the indicated process and its threads are affected), 1 (the process and its descendants are affected), or 2 (just one thread of the indicated process is affected).

`Class` and `Delta` are the desired values for class and delta.

`PID` is the ID of the code whose priority is altered: a process ID if `Scope` is 0 or 1, a thread ID if `Scope` is 2.

As is the case with all DOS or OS/2 calls, the return code will be 0 if the request is executed successfully; the return code will be anything else if there's an error.

For example, imagine a program that keeps track of what files you use and how often you use them. This could unfragment your files in the background, like the popular Disk Optimizer and Norton Utilities' Speed Disk programs. By keeping track of what files you do and don't use, it could also rearrange the files' directory entries so that the most-used files would have their directory entries toward the front of the directory for faster access.

Less-used files could be recommended for roll-off to floppy disks or could be automatically squeezed, as the ARC-type programs do. These files would automatically be unsqueezed if ever needed. Such a program would actually give you *more* room on your hard disk as time went on and the lesser-used files were squeezed.

You wouldn't want CPU time wasted on these housekeeping tasks while you were busy doing some heavy spreadsheet work, but you wouldn't mind the system doing this while you were on the phone or scratching your head. That's the value of priority 1. Such a background task would be assigned the low priority, and the system wouldn't even consider the task for execution unless there were nothing else to do.

More specifically, you could say that a class 3 beats a class 2, which beats a class 1. If there is a single job of class 3, none of the class 2s or 1s get any time at all, except when the class 3 job is waiting for I/O. If there are no class 3s in the system, the class 2s take all the CPU time. Only when there are no class 3s or 2s, or when the class 3s and 2s are all waiting for I/O, do the class 1 jobs get any time.

Within classes are deltas. A delta is an integer from −31 to +31. If a program doesn't request a delta, it gets the middle-of-the-road value of 0. A program's default class and delta are, then, 2 and 0, respectively. Deltas matter only in the case of ties. If there are no class 3 jobs in the system, but several class 2 jobs, the class 2 job with the highest delta gets the lion's share of the time. Otherwise, they share time equally, unless you specify `priority=dynamic`, in which case the foreground program gets a bit more time. (Refer to my November 1988 column for more information.)

Deltas don't affect job performance across classes. A class 3, delta −31 program still gets more time than a class 2, delta +31 program.

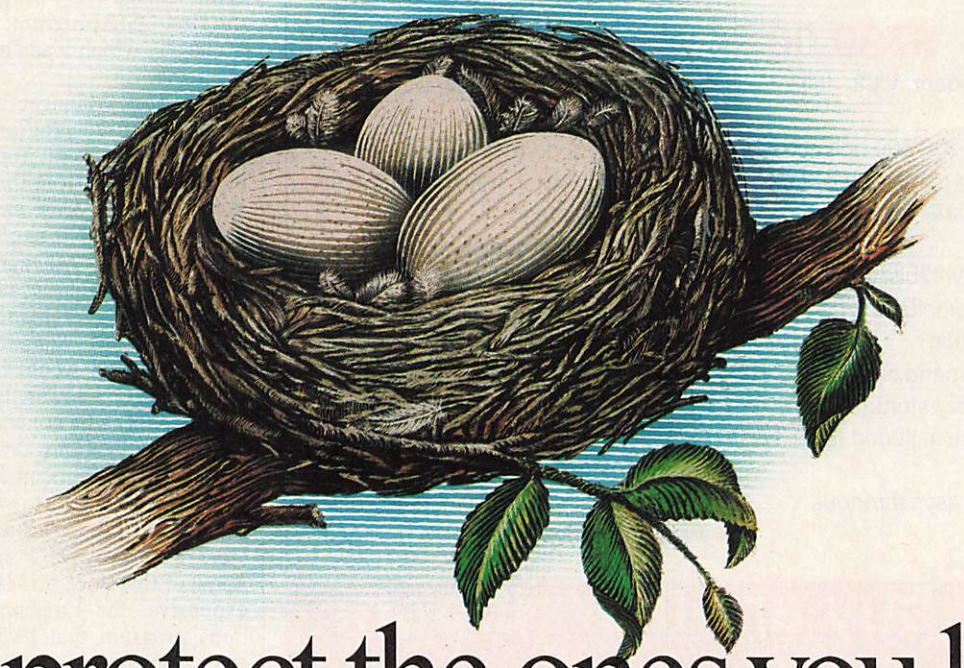
Programs get priority class 2 unless they ask for a different class. That's all it takes—they just ask. I keep fearing that a software vendor will program its package to set its own priority to class 3, mainly to ensure that it will look good in magazine benchmarks or the like. Such an action would make the rest of the system stop dead, except when the package was waiting for I/O; the entire system would be enslaved to a single application. Pretty scary, in my opinion.

Changing Priorities

How does a job change its priority? Simple: with an application programmer interface called DOSSETPRTY. For the details, see the text box "Setting Task Priorities with DOSSETPRTY" above. Basically, you just specify the process ID of the program whose priority you want to change, specify the new class and delta, and call DOSSETPRTY.

Not just anyone can change a priority. A program can change the priority of only itself or one of its child processes, a

continued



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program that it started executing. Lotus 1-2-3, for example, could not change dBASE's priority unless 1-2-3 had actually *started* dBASE on your system—not a likely prospect. The only program that could change every program's priority is the first OS/2 program, the Presentation Manager, which leads me to the following gripe.

The Task Manager window lets you see some of the programs that are running on your system. You can even terminate a program from the Task Manager. Why can't you view and change a program's priority? It can't be that hard to rewrite the Task Manager so that you see *all* programs running, not some of them, and to allow user manipulation of program priorities. Something simple and mouse-oriented would be a tremendous boon to OS/2's power. Heck, you can do it with Unix, why not with OS/2?

And applications developers, you're just as guilty. Remember that any application can change its own priority. Why not include it as a user-adjustable parameter? The only OS/2 application that I know of that does this is one of the least expensive, the Logicomm communications program that I've mentioned before. Logicomm lets you change the priority of the system while in the process of file transfer. Why no others? End of gripe.

An Update

I see that I'm almost out of space. Before I conclude, however, here's a BIOS update. I mentioned months ago that the AMI BIOS won't run OS/2. Since then (as several readers have let me know—I'd already heard, but thank you to all who wrote), AMI has remedied the problem. The latest AMI BIOS runs OS/2 with no troubles. And if you have a clone that just won't run IBM's OS/2, you might try AST Research's OS/2 1.1. It seems more forgiving than other vendors' OS/2s. I run it on an old Micronics motherboard that seems unable to run any other version of OS/2.

Coming up: a program to exercise OS/2's priority-adjustment features, the High Performance File System stuff, and more on applications. ■

Mark J. Minasi is a managing partner at Moulton, Minasi & Company, a Columbia, Maryland, firm specializing in technical seminars. He can be reached on BIX as "mjminasi."

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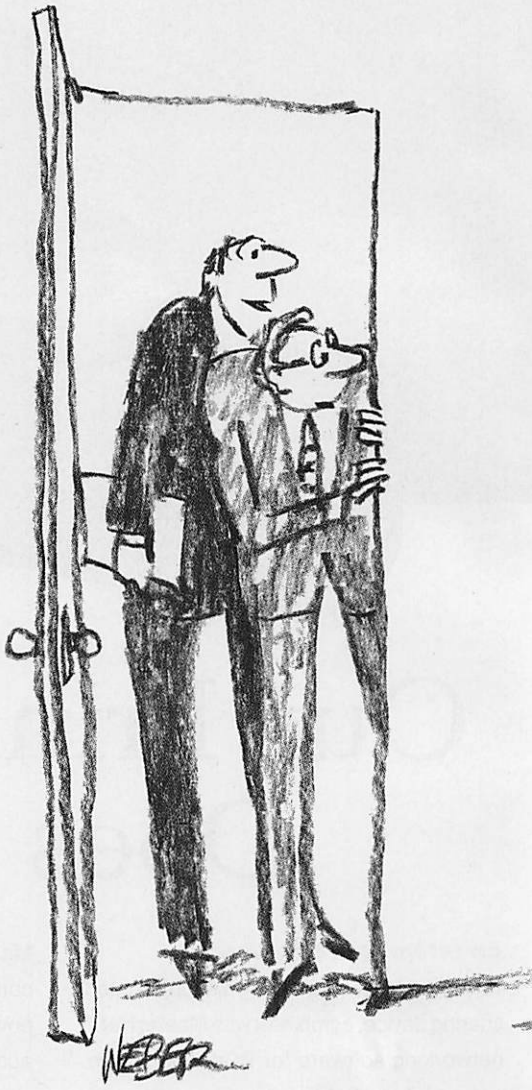
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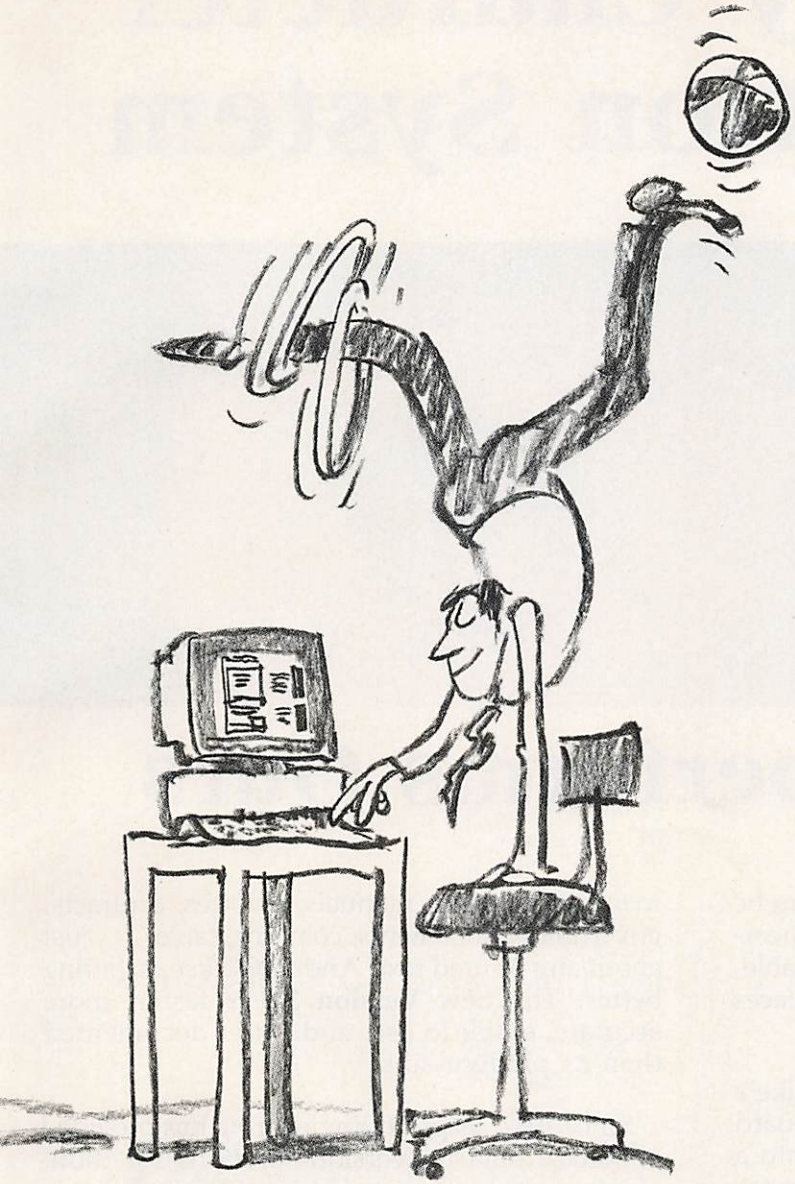
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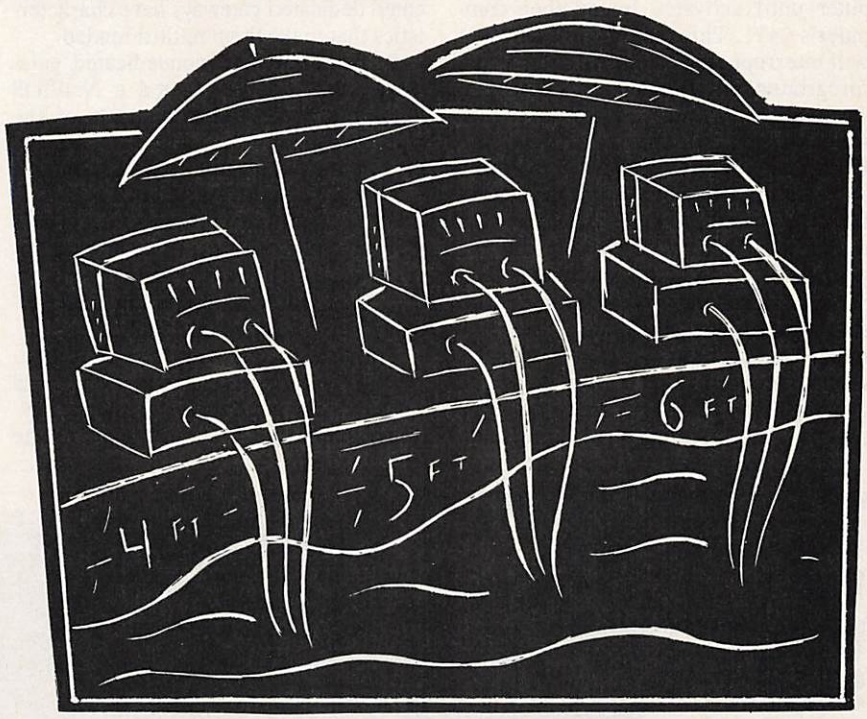
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EVERYONE INTO THE POOL

Making sense out of asynchronous gateways



LAN gateways come in many different varieties, but the most common are asynchronous gateways, or "modem pooling" devices used over dial-up lines.

In most asynchronous gateways, one or more computers act as the communications server, or gateway device. They contain the shareable communications hardware, along with special communications software that acts as a two-way link between the other LAN workstations and the communications hardware. Most often, this link uses NetBIOS to route workstation communications data to and from the actual communications hardware. On the workstation side, something other than the usual standalone communications software is required—the technique of talking directly to a communications interface adapter won't work in a gateway environment, since the workstations don't have any communications hardware of their own.

Dedicating Resources

The gateway computer is often dedicated to the task of managing communications links and may service multiple ports and modems. Some gateway implementations, however, are nondedicated, so you can use the gateway computer as a regular workstation.

Dedicated gateways typically display a "control panel" on the screen that shows current call status and session usage information. A menu or command-line interface provides the ability to perform functions like forcing disconnection of an orphaned session or, if multiple lines exist, taking a modem out of service by disabling one of the serial ports. The software may also be able to keep a log of communications activity that you can use for departmental accounting and troubleshooting.

A nondedicated gateway computer usually uses a TSR program that operates in the background. The gateway software can't take up much memory, because the computer will also be used as a normal workstation.

The gateway software also has to be well-behaved; unfortunately, most TSR programs fare badly on a LAN. The software must also be bug-free, because a system crash not only will kill the communications session but will affect the workstation user as well. Finally, the gateway software has to be time-critical: It can't soak up too much of the CPU, it can't lose characters, it has to prevent interrupt latency (i.e., failing to handle a subsequent interrupt because the servicing of the current interrupt takes place with interrupts masked), and it must handle the possibility of reentrancy (this happens, for example, when the same gateway software services multiple communications ports, and portions of the software are common to both ports; if the common code is executing when a new interrupt occurs and the new interrupt also needs to execute that common code, the code must be written to be reenterable). These are formidable issues for a personal computer.

Inside the Gateway

In a nutshell, here's how gateway software works. On start-up, the software initializes the COM ports and resets the modems. It establishes a unique name for itself on the LAN by performing a NetBIOS `Add Name` call. If the gateway serves multiple ports, it may take the approach of establishing a unique name for each port. The application then makes itself available by issuing a `Listen` command to NetBIOS for each unique name.

In a dedicated gateway, the gateway computer is idle while `Listen` commands are outstanding. Only when a

continued

ILLUSTRATION: JANE FLYNN © 1989

workstation issues a NetBIOS `Call` command to a gateway's unique name does it go to work.

In a nondedicated (background) gateway, the DOS prompt reappears once you've loaded the gateway software, and you can run other applications. The gateway software uses the NetBIOS "no wait" option on its `Listen` command, along with the Post address of a routine to handle a `Call` from a workstation, and thus it can relinquish control of the computer until activated by another computer's `Call`. This means that each `Call` will interrupt applications running in the foreground on the gateway computer. The routine at the Post address takes control, saves the caller's name and the NetBIOS-assigned Local Session Number, and sets up a Receive Network Control Block containing the Post address of a routine to handle messages sent from the workstation. The gateway software then performs a `Return-From-Interrupt` instruction to allow the application in the foreground to continue. If the program is written properly, the person using the gateway computer as a workstation never notices that the computer's serial ports are being shared.

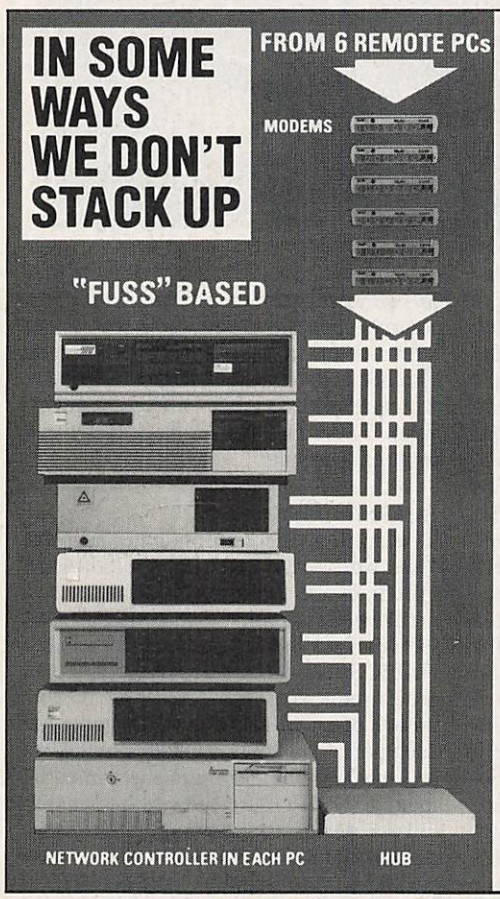
Similar processing takes place in a dedicated gateway, and it may even use the no-wait option on the `Listen` command. If so, the software monitors the Final-Return-Code field of the Network Control Block to determine when the command is complete. The difference is that the dedicated gateway software doesn't have to worry about coexisting with other applications. However, both the nondedicated and the more sophisticated dedicated gateways have characteristics that make them multithreaded.

In dedicated and nondedicated gateways, once you've created a NetBIOS session, the dialogue consists of the workstation asking the gateway, "Do you have characters you've received from the modem?," "Is the carrier still active?," or "Can you send these characters through the modem?" The gateway processes each of these messages by honoring the request and sending back received characters and a result code.

Stand-alone communications programs typically poll the keyboard and serial port in a tight loop: "Is there a keyboard character I should send to the modem? If not, is there an incoming serial port character I should show on the screen? OK, go back and check the keyboard again." As you can imagine, the polling of the serial port (or, more accurately, the buffer of received characters) happens many times per second.

If, in a gateway environment, each workstation sent its polling request to the gateway as a NetBIOS message, the LAN would begin to creak and groan under the strain. A better approach is to have the workstation and gateway be a little smarter than the average stand-alone communications package. The workstation sends a message containing the entire dialing command and phone number. It also issues a single "Any incoming characters?" request and assumes that there aren't any until the gateway replies with a message packet containing one or more received characters. If you're sending multiple characters across the line, as in the case of an X-MODEM file transfer, the workstation sends each data block of characters as a single NetBIOS message. Reporting a lost carrier is the responsibility of the

continued





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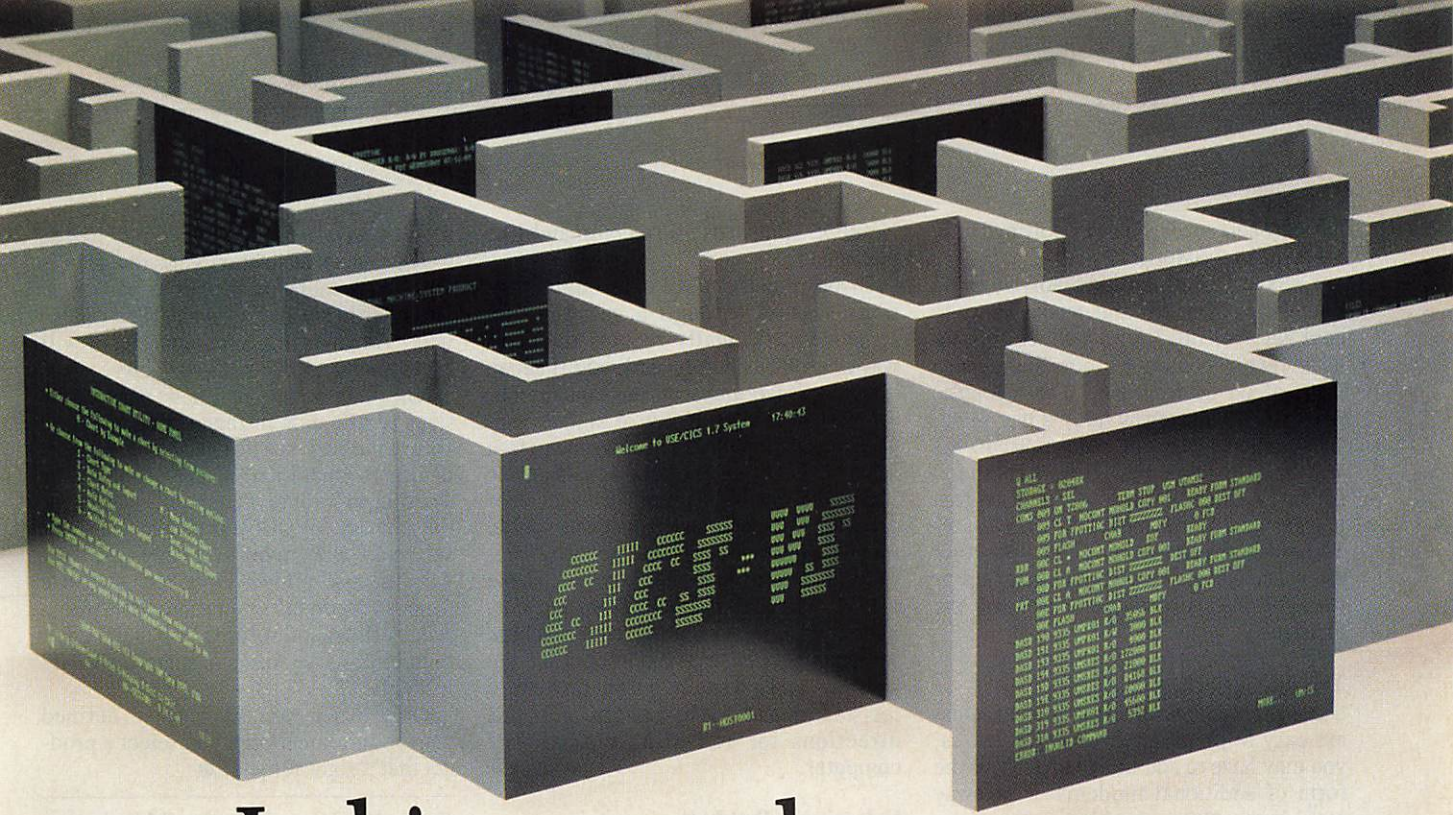
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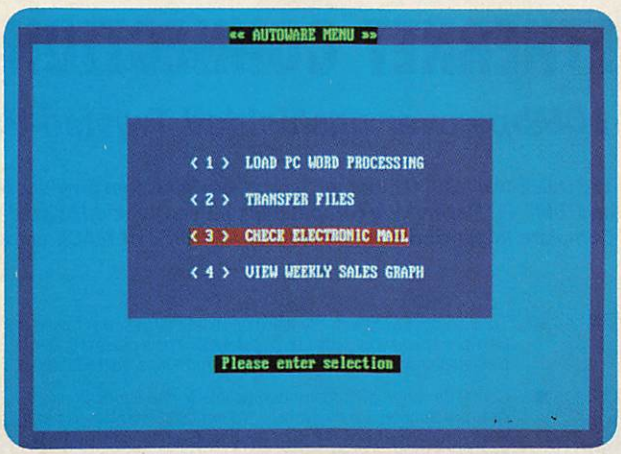
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gateway software; it's not a polling function within the workstation.

LAN communications software on both the workstation and gateway have to deal with NetBIOS return codes and unusual error conditions not found in a stand-alone environment. For example, what should a gateway do if it has an active, carrier-present communications session with a remote computer and it suddenly finds that the workstation that it's serving is no longer talking back? The programmer must decide whether the gateway software should hang up or wait for the workstation to resume the dialogue.

Troubleshooting

Some problems with gateway computers are easy to pinpoint. If usage increases, you may have to add more capacity in the form of additional modems or gateway machines. Other problems are more subtle. A gateway may be capable of managing multiple NetBIOS sessions with multiple workstations, but you may need to increase the default NetBIOS session limit (commonly six sessions) on the gateway computer. Fortunately, most NetBIOS emulators allow command-line parameters.

If you're in the midst of a communications session through a gateway and someone accidentally reboots the gateway or kicks its power cord, you'll get an error message and lose the connection. Since the gateway is out of sight somewhere, error messages usually mean that it's time to get up and take a walk to see what's happening. Unless it's only for occasional dial-out use, a gateway should receive some of the same security precautions you give to file servers. These include physical isolation from the normal work area, a sign near the machine warning people to avoid rebooting the gateway, and a written, posted procedure for starting the LAN that also contains directions for activating the gateway computer.

Selecting a Product

If you decide to add a gateway to your LAN, you almost certainly won't be able to go down to the local computer store to see demonstrations of each of the types of gateways. Although LANs are proliferating rapidly, LAN products like gateways aren't yet considered off-the-shelf items.

A good place to start your research is with the manufacturer of your particular LAN hardware and software. The vendor will have its own gateway product or will recommend a third-party package.

The next step is to know what questions to ask. For instance, can you configure the software for dedicated or nondedicated operation? Can you use your existing communications software with the gateway, or will you need to buy new software? How many users does the software license allow? Does the software support terminal emulation, file transfers, scripts, and macros? Does the communications server support NetBIOS? XNS? IPX?

Only when you have fully defined your requirements can you select a product that's right for you. ■

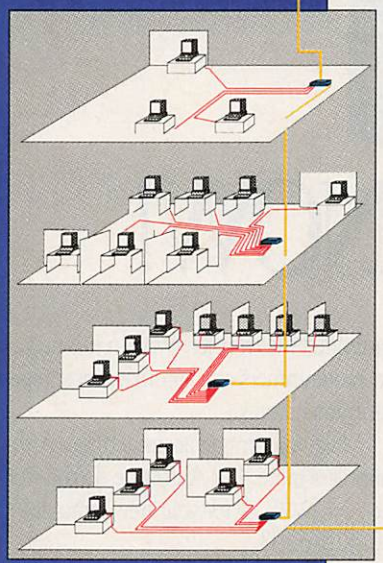
Barry Nance works in the R&D department at Programming Resources Co. in Hartford, Connecticut. He can be reached on BIX as "barryn."

Your questions and comments are welcome. Write to: Editor, BYTE, One Phoenix Mill Lane, Peterborough, NH 03458.

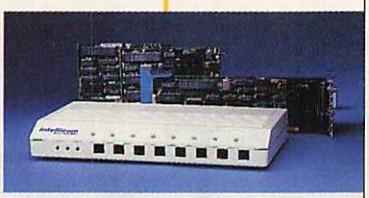
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VGA/Mono	$1602	$1827	$1932	$2057	$2552	$3012
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VGA/Mono	$2387	$2537	$2667	$2797	$3367	$3617
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VGA/Mono	$3454	$3649	$3749	$3874	$4319	$4829
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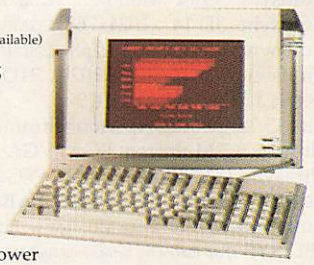
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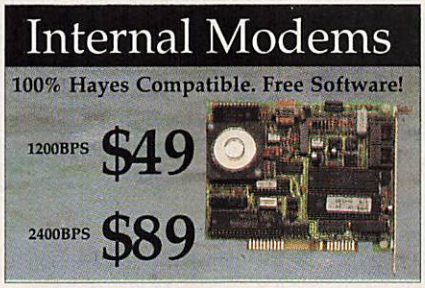
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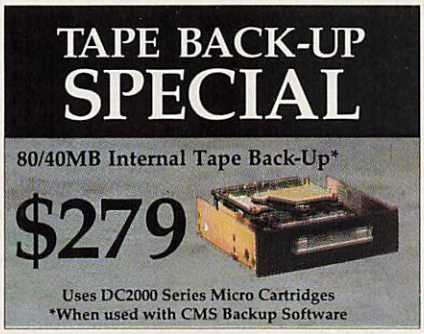
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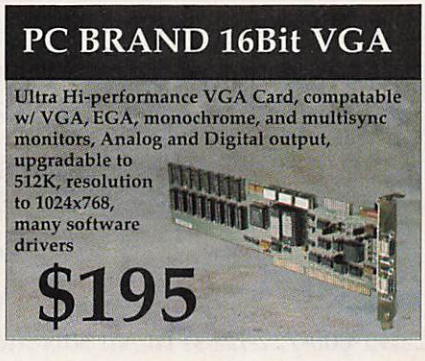
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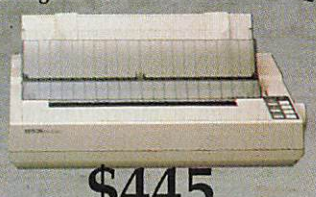
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The Brains Behind the Graphics

Coprocessor-based display controllers bring new speed and flexibility to PC graphics

Steve Apiki, Howard Eglowstein, and Rick Grehan

In the days when the C> prompt was common, handling the video display was not a big deal. You worked with a grid of 80 by 25 characters most of the time, switching to 640- by 350-pixel graphics mode to draw the odd introduction screen—nothing an 8088 or 80286 couldn't handle along with the rest of its chores.

Alas, those days are gone. Today's graphical user interfaces, windowing environments, CAD, and desktop publishing applications can put quite a strain on the CPU, even if it's an 80386. The dumb frame-buffer approach taken by VGA and previous graphics adapters can no longer support the higher resolution and higher speed that exacting applications demand.

The future of microcomputer graphics lies with intelligent display controllers. Manipulating the display space of even a medium-resolution (1024- by 768-pixel), noninterlaced display can mean modifying 768K bytes of memory—a lot to ask of the already harried CPU. Move up to 1280 by 1024 pixels, and the requirement goes up to 1.25 megabytes. As resolutions and color depths grow, the time the CPU spends updating the display grows along with them. The most effective solution is to relieve the CPU of this burden and to put control of display memory in the hands of a dedicated processor. Boards built around graphics-oriented chips also benefit from the processor's hard-wired graphics functions.

This month, the BYTE Lab examines 11 intelligent graphics controllers with an eye toward their performance in CAD and desktop publishing applications. We'll also get a glimpse at how some of these boards perform under the TIGA (for Texas Instruments Graphics Architecture) interface standard (see the text box "Benchmarking the TIGA" on page 188).

All these cards support at least 256 simultaneous colors (8-bit pixel depth) and either 1024- by 768-pixel or 1280- by 1024-pixel resolution. Two of them are designed for the Micro Channel architecture (MCA); the rest are AT-compatible. They fall into a broad price range, from around $1000 to close to $4700, with a corresponding range in capability and support software (see table 1).

Each of the 11 cards shares the same basic design: at the heart of the board, a TMS34010 GSP (for Graphics System Processor) from Texas Instruments (TI); some video memory to hold the display map; and circuitry to drive the monitor.

On-Board Intelligence

TI's TMS34010 is probably the most popular graphics processor in the current PC market. Its powerful graphics capabilities have earned it a place in everything from frame grabbers to printer controllers, including, of course, display controllers.

What makes the 34010 so well-suited to graphics is not immediately obvious. A quick glance at the instruction set reveals a typical repertoire: arithmetic operations, logical operations, comparisons, jumps—nothing surprising. There are the usual addressing modes: register-to-register, immediate-value-to-register, and absolute- or indirect-address-to-register.

Look a little more closely, however, and you'll find some instructions with unfamiliar mnemonics. These are the dedicated graphics instructions. They are hardware implementations of essential graphics functions, such as filling a pixel array, drawing a line, pixel block transfers, and comparing a point to a window.

There's also a graphics-oriented register indirect in *x,y* addressing mode. In this mode, a register holds a pixel's address in *x,y* form—the pixel's Cartesian coordinates on the screen. The mode relieves the software of the time-consuming job of working out the mapping of each pixel's memory address to its screen location.

Delve even deeper into the 34010's architecture, and you'll find that the device is built for graphics from the ground up. It has 30 32-bit registers divided into an A bank and a B bank. The A bank registers are general-purpose; software can use them for temporary storage during computation. B bank registers are specialized; they hold information like the location and dimensions of the current clipping window or the current foreground and background colors.

While the 34010 would make a credible stand-alone processor, the designers built in special provisions for working in a coprocessing environment. Twenty-eight I/O registers map to high memory locations in the 34010's address range. Some of these registers are directly accessible by the host processor via external pins. Hardware designers were relieved to see this; it made it easier for them to design a microcomputer-to-34010 interface. The programmer's job was also made easier; through these I/O registers, the host microcomputer can read from and write to the coprocessor board's memory, halt the 34010, and restart it at a known address.

The Rest of the Story

A coprocessor, no matter how powerful, does not a graphics controller make.

continued

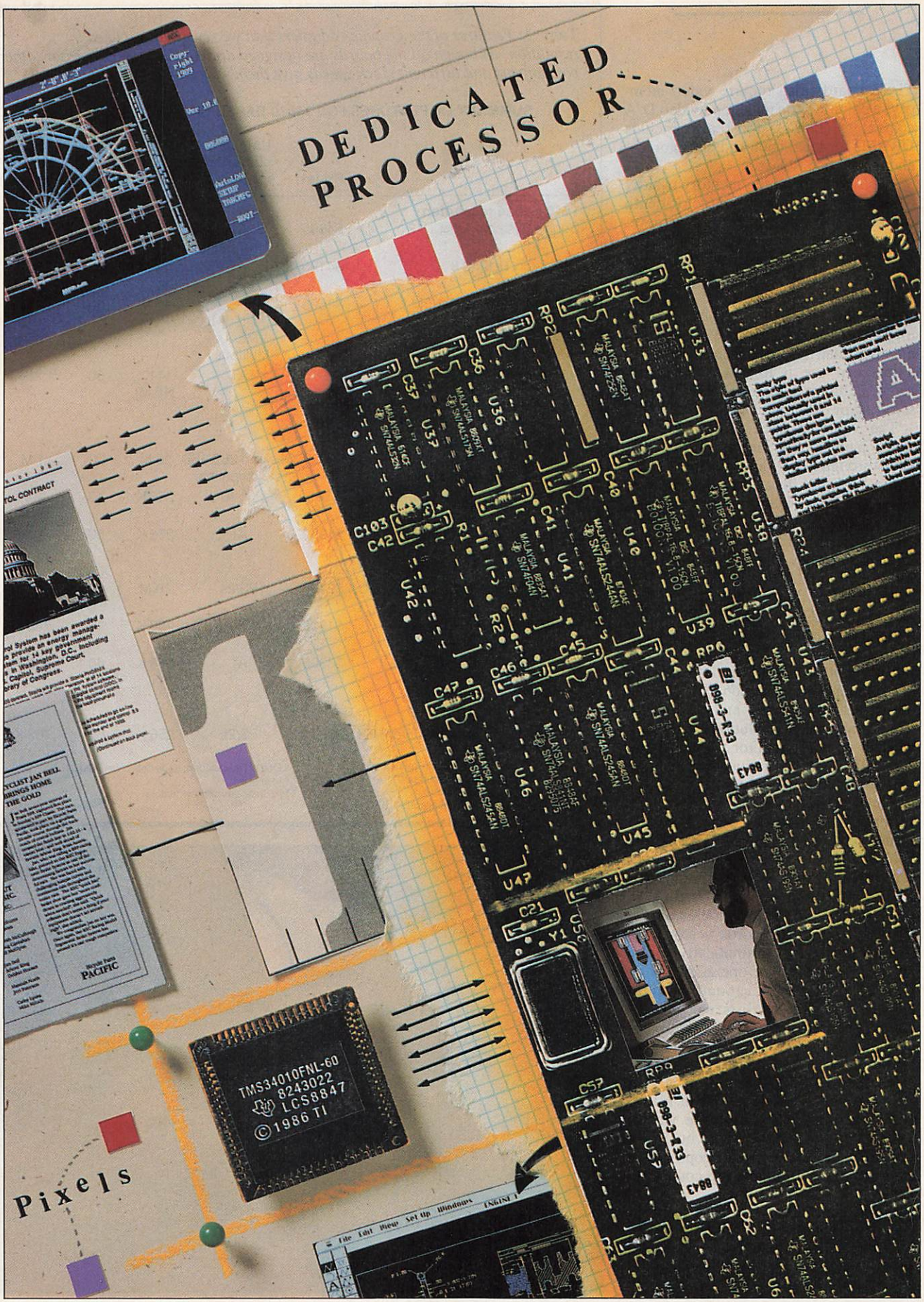


ILLUSTRATION: RICHARD SCHNEIDER © 1989

These boards also require video memory, a color lookup table, and video D/A converters (DACs). Most also include DRAMs for local code and data storage, and instruction ROMs.

The size of the video memory usually determines the resolution/color-depth combinations that a board can achieve. Each pixel requires at least 1 bit; in 256-color mode (2^8), each pixel requires 8 bits. For example, a 1280- by 1024-pixel card operating in 256-color mode requires 1280 × 1024 × 8 bits, or 1.25 megabytes. Cards that have more video memory than a single display page requires can use it to retain off-screen images that it may need for smooth scrolling or other quick recall.

The value of each pixel, stored in video memory, is indexed to a video DAC through a color lookup table. Video DACs typically have far greater color resolution than video memory can support—a typical value is 8 bits each for red, green, and blue, or 24 bits. A 24-bit lookup table allows the board to select, in 256-color mode, 256 of the possible 16.7 million colors that 24 bits allows. The lookup table/DAC combination, therefore, determines the size of the complete color palette.

On the other side of the DAC lies the analog monitor connection. The board's output scan frequency and bandwidth, which vary with resolution, determine whether or not a monitor is compatible. Typically, a high-frequency or multiscanning monitor is required.

With the exception of the Enertronics Aurora 1024, each of these devices includes some local DRAM. DRAM can hold downloaded 34010 instructions or screen-related data. When running some CAD programs, including AutoCAD, on-board DRAM might contain a *display list*. A display list records vector positions in a drawing, dramatically speeding redraw and similar operations by relieving the CPU of repeated vector calculations. Display lists can also be maintained in system memory or even on disk.

One of the more interesting features offered by several manufacturers is VGA pass-through capability, which allows you to hook to VGA hardware via the VGA extension on the MCA bus, or a special cable between the coprocessor card and the VGA card's top connector.

Table 1: *Features of the graphics adapters that we reviewed, grouped by resolution. Although all the boards are designed around the same processor, other components and different clock speeds give them widely varying capabilities.*

SUMMARY OF FEATURES FOR 34010-BASED GRAPHICS BOARDS

	Price[1]	Hardware platforms supported	Color palette	34010 speed (in MHz)	Video memory (in bytes)
1280 x 1024 resolution					
Control Systems Artist TI12	$4695	AT	16 M	50	1.25 M
IMAgraph TI-1210-8	$4195	AT	16 M	40	1.25 M
Matrox PG-1281 C/8/1.5M	$4595	AT, PS/2s, Multibus II, VMEbus, Multibus I	16 M	50	2 M
Number Nine Pepper Pro1280	$2995	AT	4 K [16 M]	50	1.25 M
1024 x 768 resolution					
Compaq Advanced Graphics 1024 (with add-on memory card)	$2098	Deskpro 286/386 or compatible	16 M	50	1 M
Enertronics Research Aurora 1024[6]	$995	XT, AT	256 K	40	1 M
NEC MultiSync Graphics Engine	$1999	AT	256 K	50	1 M
Number Nine Pepper Pro1024/MC	$2495	PS/2s	16 M	60	1 M
PC Tech Color 34010 Board	$1600	PC, AT	256 K	40	768 K
Vermont Microsystems Cobra Plus HS	$3395	AT	256 K	60	768 K
Vermont Microsystems Cobra/2 HS	$3395	PS/2s	256 K	60	768 K

[1] As tested; some boards include optional memory.
[2] Interface drivers included with board.
[3] VGA pass-through supported.
[4] Support announced but not available when reviewed.
[5] One of two included; additional driver is $100.
[6] Interlaced.
[ ] = Indicates optional feature.

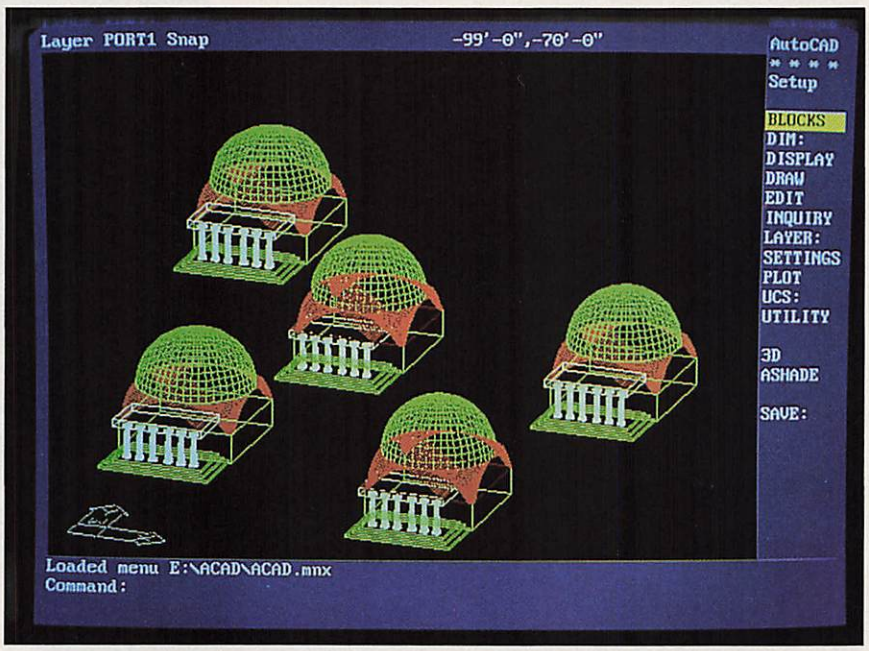
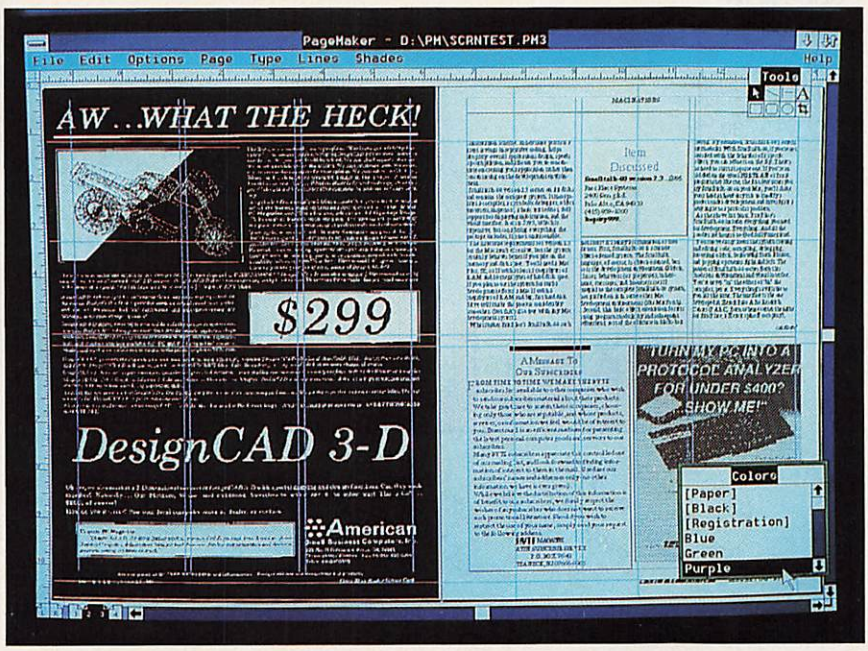


Photo 1: *The large AutoCAD drawing used in our tests, at 1024 by 768 pixels. This drawing file requires a display list of more than 512K bytes.*

Additonal RAM (in bytes)	Standard modes	Application interfaces[2]	Application drivers included	Horizontal scan frequency (in kHz)	Video bandwidth (in MHz)
1 M	VGA[3]	PGL, TIGA-340	Windows for TIGA, ADI for TIGA	64	108
512 K	MDA, CGA, Hercules[3]	DGIS, TIGA-340[4]	None	64	108
1.5 M	CGA, EGA Text	PGA[5], [CGI], LIBShell[5]	None	64	110
128 K	CGA, MDA	NNios, TIGA-340	Windows for TIGA, ADI for TIGA	64	107
128 K	None[3]	Halo, [DGIS], TIGA-340[4]	ADI, Windows/286/386	54	41
None	CGA/EGA Text[3] [VGA]	8514/A AI	ADI, Windows/286	35.5	44.9
768 K	VGA	DGIS, CGI, TIGA-340[4]	ADI, PM[4], Windows/286/386, GEM	48-64	64
512 K	None[3]	NNios, TIGA-340	Windows for TIGA, ADI for TIGA	48.5	64
1 M	None [CGA]	DGIS, TIGA-340	Windows for TIGA, ADI for TIGA	49	64
512 K	None[3]	PGL, 8514/A AI	Windows/286/386, ADI, Computervision, VersaCAD, Microcadam, PCAD	48.8	64
512 K	None[3]	PGL, 8514/A AI	Windows/286/386, ADI, Computervision, VersaCAD, Microcadam, PCAD	48.8	64



You then run the output of the intelligent card to a multiscanning monitor that can handle both high-resolution and VGA frequencies. Whenever the board is not active, it allows the VGA card to drive the monitor; when the board becomes the active display controller, it takes over the connection.

Other common components include controller ROMs, which may include IBM standard-mode (e.g., CGA or MDA) emulation firmware. Without emulation, add-on VGA modules, or VGA pass-through, you'll require a dual monitor configuration. Some manufacturers put proprietary operating systems or software interfaces, such as DGIS (for Direct Graphics Interface Standard), onboard as well.

Application Tests

Currently, CAD and desktop publishing applications represent the most likely uses of these graphics boards. We ran several tests under the two most popular of these packages, Autodesk's AutoCAD release 10 and Aldus PageMaker 3.0; the results are graphed in figure 1. PageMaker runs under Microsoft Windows, so results of the PageMaker test also give a good feel for the effectiveness of the Windows driver.

All our tests on AT-compatible cards were carried out on a Compaq 20-MHz 80386, and we tested the MCA boards on a 16-MHz IBM PS/2 Model 80. We completed the test system with one of three monitors: either NEC's MultiSync XL, which covered the lower-resolution (hence lower-frequency) controllers; or a Hitachi HM-4319 or Mitsubishi HL-6905, which both span the 30- to 65-kHz frequency range and worked with all these graphics boards.

Our AutoCAD tests were designed to test both display list and non–display list performance. Since many of these cards require expanded memory for display-list storage, we portioned out 512K bytes from extended memory using the Compaq Expanded Memory Manager (CEMM) on the Compaq or the Quarterdeck Expanded Memory Manager on the Model 80.

We used two files for the AutoCAD tests, one medium-size (300K bytes on disk and requiring a display list between 256K bytes and 512K bytes) and one large (453K bytes on disk with a display list larger than 512K bytes). The large

continued

Photo 2: *Our PageMaker test file, also at 1024 by 768 pixels. It combines text objects with bit maps of varying size.*

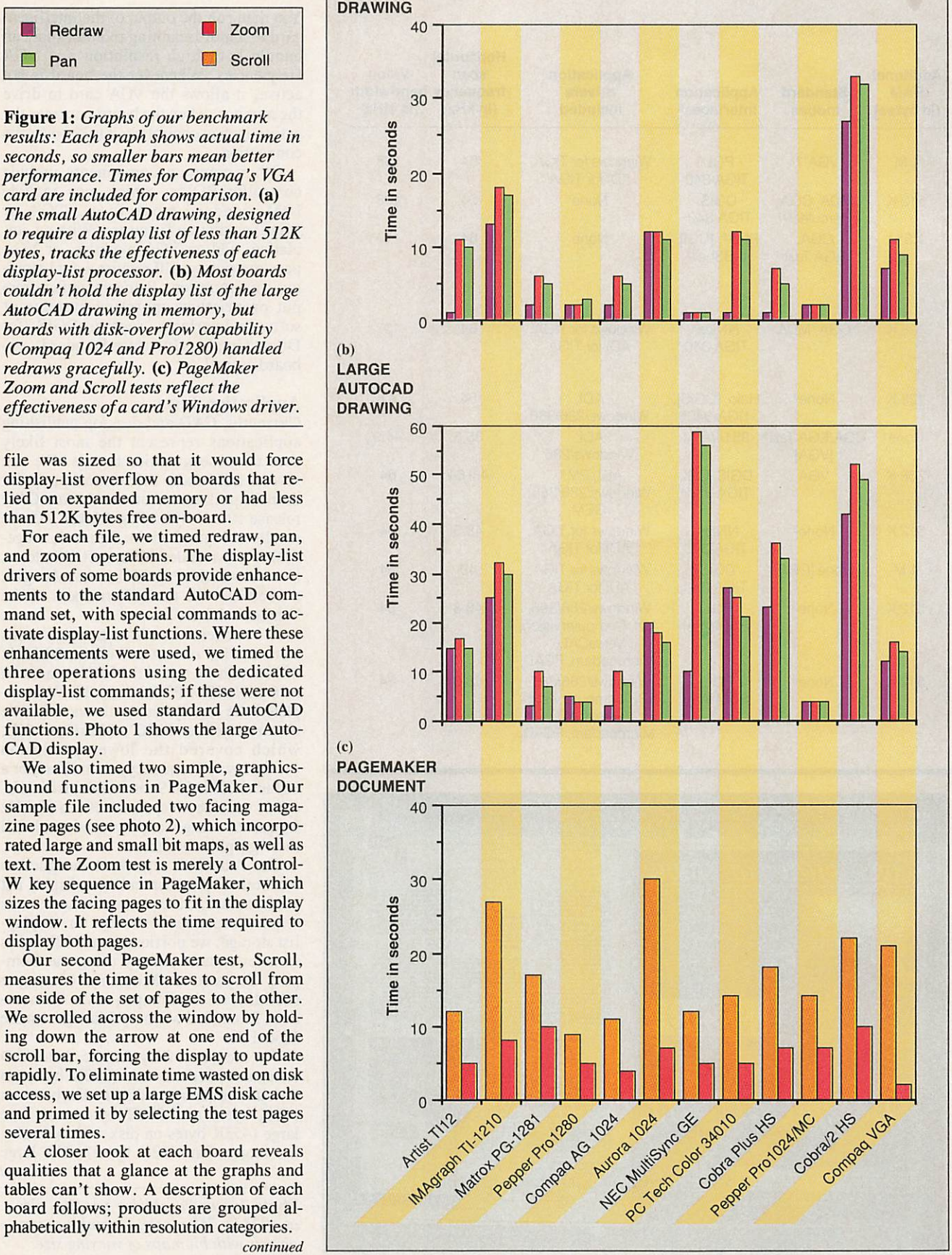


Figure 1: *Graphs of our benchmark results: Each graph shows actual time in seconds, so smaller bars mean better performance. Times for Compaq's VGA card are included for comparison.* **(a)** *The small AutoCAD drawing, designed to require a display list of less than 512K bytes, tracks the effectiveness of each display-list processor.* **(b)** *Most boards couldn't hold the display list of the large AutoCAD drawing in memory, but boards with disk-overflow capability (Compaq 1024 and Pro1280) handled redraws gracefully.* **(c)** *PageMaker Zoom and Scroll tests reflect the effectiveness of a card's Windows driver.*

file was sized so that it would force display-list overflow on boards that relied on expanded memory or had less than 512K bytes free on-board.

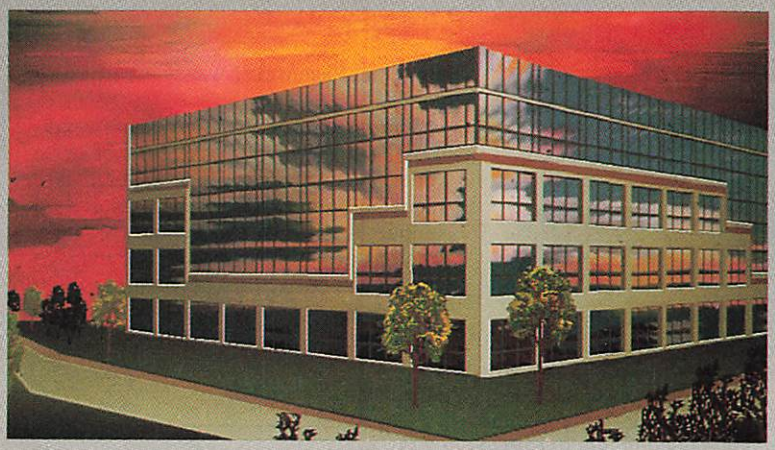
For each file, we timed redraw, pan, and zoom operations. The display-list drivers of some boards provide enhancements to the standard AutoCAD command set, with special commands to activate display-list functions. Where these enhancements were used, we timed the three operations using the dedicated display-list commands; if these were not available, we used standard AutoCAD functions. Photo 1 shows the large AutoCAD display.

We also timed two simple, graphics-bound functions in PageMaker. Our sample file included two facing magazine pages (see photo 2), which incorporated large and small bit maps, as well as text. The Zoom test is merely a Control-W key sequence in PageMaker, which sizes the facing pages to fit in the display window. It reflects the time required to display both pages.

Our second PageMaker test, Scroll, measures the time it takes to scroll from one side of the set of pages to the other. We scrolled across the window by holding down the arrow at one end of the scroll bar, forcing the display to update rapidly. To eliminate time wasted on disk access, we set up a large EMS disk cache and primed it by selecting the test pages several times.

A closer look at each board reveals qualities that a glance at the graphs and tables can't show. A description of each board follows; products are grouped alphabetically within resolution categories.

continued







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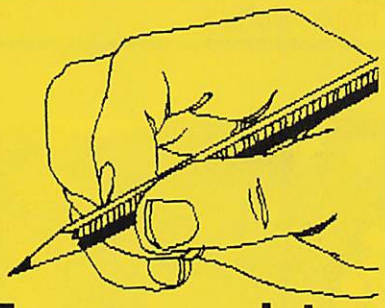
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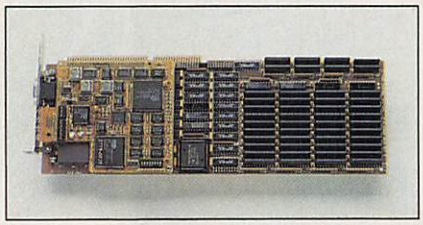
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1280 by 1024 Pixels

Control Systems Artist TI12



Although the Artist TI12 demonstrated good performance, it could not live up to expectations set by its high price. At $4695, the Artist TI12 was the most expensive board we reviewed, and it is less well equipped than a few less costly cards. Upgrades don't come cheaply, either: It costs $895 for a 1-megabyte DRAM upgrade and $1695 for 2 megabytes, $795 for a VGA Module, and $249 for a VGA pass-through kit.

The Artist package includes diagnostic software, PGL (for Professional Graphics Language) drivers, and the TIGA driver package. Control Systems does not provide any separate application drivers, so we tested the board exclusively under TIGA. If you choose to communicate with AutoCAD through PGL, you'll have to forgo display-list processing.

TIGA's AutoCAD driver supports a display list in expanded memory, but it does not have some of the slicker display-list features demonstrated by the other packages. More important, the driver is written for AutoCAD release 9 and does not support display-list-based pan and zoom functions.

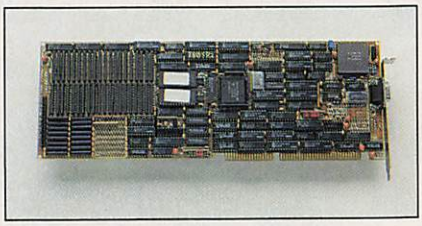
The driver intercepts standard AutoCAD commands; if the display list overruns the allotted expanded memory, all display-list processing is disabled. This is hardly a weakness of Control Systems' product, but it causes the Artist TI12 to suffer in comparison with boards like the Matrox PG-1281 and Pepper Pro1280.

The display list was enabled for the small drawing and disabled for the large drawing. While the board was very responsive when doing redraws with the display list, pan and zoom functions suffered from using the TIGA driver. Non-display-list drawing times were excellent, so if you lack the memory to use the display list, the penalty won't be that great.

All installation and testing went without a hitch. We did notice a bug in the TIGA Windows driver that keeps it from properly displaying dragged bit maps, but the problem can be corrected by forcing a redraw. Performance under Windows and PageMaker was generally very good.

The Artist TI12's only glaring weakness is in the critical category of price versus performance. While the hardware seems to be in excellent shape, software support is limited, and the current early versions of TIGA drivers do not manage to squeeze out all the performance that they could.

IMAgraph TI-1210-8



The IMAgraph is a solidly built board that provides full Hercules- and CGA-emulation modes in addition to its high-resolution graphics. The board's installation instructions make the setup and configuration as easy as falling out of bed.

One of the nicest things about the IMAgraph board is the optional ACAD ADI display-list driver. The standard driver gives you full resolution and color but no display-list capability. The $195 IMAzoom package buys you display lists and real-time display of pans and zooms. Clicking on the IMAzoom Shutter brings up a smaller window and a submenu. An overview of the screen is shown within the window, and you use the digitizer to control the interactive zoom and pan functions.

In spite of the display-list support, the IMAgraph board consistently turned in some of the slowest times in our AutoCAD tests. The TI-1210-8 keeps all display lists in local memory. Unfortunately, the on-board memory was too small for either the small- or large-file display lists—IMAzoom with our files required more than 512K bytes, so we lost display-list capability. If you do a lot of work with AutoCAD, you may find that IMAzoom is such a useful addition that a RAM upgrade may be a worthwhile investment.

The optional Microsoft Windows driver handles the IMAgraph board nicely. The text and menus are clear and easy to read. The display driver handles bit maps rather slowly, a handicap if you need to move a lot of high-resolution images. One of the two pages on our PageMaker

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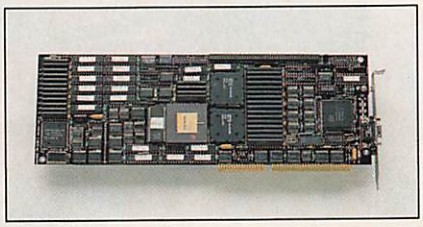
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test document is a full-screen bit map, digitized at 300 dots per inch. When this page is redrawn, the display bogs down considerably handling the bit map. Objects belonging to Windows, such as lines, rectangles, and text, are displayed much faster. Pull-down menus suffer the same fate as large bit maps. When you select a menu from the menu bar, it appears very slowly. We found this rather annoying.

At $4195, the TI-1210-8 costs much more than the Number Nine Pepper Pro1280, but it's competive with the other 1280- by 1024-pixel boards. We wouldn't choose this board for Windows, but the AutoCAD/IMAzoom combination makes the IMAgraph board (with sufficient memory) worth a look.

Matrox PG-1281 C/8/1.5M



The Matrox PG-1281 provides CGA emulation in addition to full PGA compatibility. We tested the version for the AT, but the board is also available for the PS/2s, Multibus, and VMEbus computers. We tested the optional drivers for AutoCAD release 10 and Windows.

The installation manual is very detailed. It's a good thing, too, as the evaluation unit came without a video cable. After several minutes of poking through the manual, we found the description of the video connector and located a suitable cable. Matrox sells video cables and monitors as options.

AutoCAD really likes this board. Our tests placed the Matrox as one of the fastest 1280- by 1024-pixel boards. Memory may have something to do with it. The unit we tested was equipped with the standard 3.5 megabytes of memory. There are 2 megabytes provided for video, and 1.5 megabytes handle the downloading of 34010 programming and display-list support. It takes a lot of horsepower to handle that much memory, and Matrox gave this card three custom gate arrays to boost the performance of the 50-MHz 34010 processor. The AutoCAD drivers are easy to install and provide support for the basic AutoCAD set—no fancy extras.

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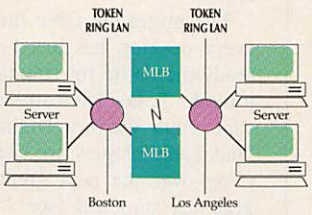
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Benchmarking the TIGA

In addition to the obvious price barrier, the major obstacle keeping coprocessor-based graphics systems from every user is a lack of suitable standards. A separate driver for each board/application combination is fine when you dedicate a board to a single CAD package, currently a likely scenario. But when your intelligent graphics board becomes your primary adapter, such an arrangement becomes intolerable.

The migration from the high end to every desktop has just begun, but already the battle for standards has been joined. Texas Instruments and 8514 supporters Western Digital and Headland Technologies are currently wrangling over the next great mainstream graphics standard (see "Clash of the Graphics Titans," *IBM Special Edition*, Fall 1989). TI touts its own 340x0 family and TIGA-340, while its rivals champion their versions of IBM's 8514 processor and the 8514 Application Interface (8514 AI).

Texas Instruments' Graphics Architecture, or TIGA, is a new software interface—the first released version (1.1) began shipping in early June. Still, its list of announced supporters from both the software and hardware development communities is impressive, and its emergence as a standard seems likely. To get a feel for the relative performance of the reviewed boards under TIGA, we developed a suite of benchmark tests, described below.

TIGA's Role

From the user's perspective, TIGA-340 is a library of graphics routines that allow application programs to communicate with boards built around chips in TI's 340x0 family. Furthermore, TI has rigorously defined the behavior of each routine in the TIGA library, so that a programmer developing an application on one TIGA board can rest easily in the certainty that his or her application will also run on any other TIGA-compatible system.

From the developer's perspective, TIGA is really two pieces of software: the communications driver, which runs on the host PC, and the graphics manager, which runs on the 34010 coprocessor board. The communications driver is actually a TSR process that usually installs itself in interrupt 7F hexadecimal. Application-generated TIGA calls pass down to the TSR process, which puts them into a kind of graphics message packet and sends them to the coprocessor board. The graphics manager then picks up the messages, determines which operation is to be performed, and executes that operation.

Any TIGA-compatible board is expected to support a minimal set of graphics operations (primitives). These are the routines that a programmer can expect to find available on all TIGA boards. The primitives are divided into two groups—core and extended. Core primitives are always available; they are loaded onto the coprocessor board when TIGA is installed (typically at boot-up). Extended primitives are optional; an application program may opt to load them only as required.

One of TIGA's strengths is that it doesn't bury that hardware under an inflexible application programming interface. Applications developers can define their own primitives, referred to as user-extended. So, if you determine that your graphics algorithms execute more efficiently when running on the 34010, you can write the routines in 34010 code (TI sells developer's kits for doing this) and build your own library of primitives. Then, at run time, your application can request that TIGA download your customized primitives to the coprocessor board. Applications can even switch libraries on the fly, deleting one set of user-extended primitives and loading another in its place.

The Benchmarks

Our TIGA benchmarks measure combined board-and-driver performance in executing common graphics tasks. They make extensive use of the TIGA 1.1 library, and they don't attempt to wring out every drop of performance through the use of user-extended primitives. Benchmarks work with objects sized in pixels, so they are independent of screen resolution.

Bit-block transfer (BitBlt) is more or less a test of memory-move operations. The BitBlt benchmark is in three parts. The first part moves a rectangular region of pixels from one region of the screen to another. The location of the source and destination regions were purposely chosen to overlap, so that the on-board transfer routine would have to set the direction pointers correctly. The second test copies a rectangular region from on-screen memory to off-screen memory and then repeatedly copies the block from off-screen memory back to

Table A: *TIGA benchmarks measure low-level performance on common graphics operations. (All times are in seconds.)*

TIGA-340 1.1 BENCHMARK RESULTS

	Clipped lines	Clipped ellipses	Filled polygons	BitBlt	Zoom	Monochrome text	Color text
Control Systems Artist TI12	33	62	71	75	42	44	58
Number Nine Pepper Pro1280 (8-bit)	34	62	N/A	75	45	46	58
Number Nine Pepper Pro1280 (4-bit)	34	62	68	40	33	41	45
PC Tech Color 34010 Board	35	67	91	97	39	73	94
Number Nine Pepper Pro1024/MC (8-bit)	28	44	60	62	25	54	76
Number Nine Pepper Pro1024/MC (4-bit)	28	44	57	33	19	43	52

on-screen memory. The times for these two benchmarks were always identical, so we combined the results under the "BitBlt" heading in table A. The final test gauges the TIGA driver's zoom capabilities. By means of a BitBlt, the program first transfers a region from off-screen memory to successively larger regions on the screen. It then copies the bit block from the off-screen source into successively smaller on-screen regions. The effect is a box that first grows to fill most of the screen and then shrinks back to its original size.

Clipped lines and *clipped ellipses* test the clipping capabilities of the TIGA hardware. The program first defines a clipping rectangle on the display and then repeatedly draws lines whose endpoints are chosen at random. Many of the lines have endpoints that lie outside the clipping rectangle; the board is therefore forced to perform clipping on such lines. The software rotates through the color palette as it draws the lines. Next, the program clears the screen, reestablishes the clipping rectangle, and repeatedly draws ellipses whose bounding rectangles are chosen at random. (The bounding rectangle of an ellipse defines that ellipse's center location and major and minor axis lengths.) Again, portions of the ellipses lie outside the clipping rectangle. The program rotates through the color palette as it draws the ellipses.

Filled polygons tests the speed with which the board can draw pattern-filled and solid-color-filled polygons. We defined four polygons of various shapes—one with holes in it—to give the filling algorithms something to think about. We also defined four fill patterns. The benchmark repeatedly draws each polygon, randomly selecting its size and location. On each iteration, the program alternates between drawing the polygon filled with a solid color or with one of the defined patterns.

Text tests each board's capabilities at drawing clipped text. The program reads a string of 5000 characters from a data file and then formats that string so that it will fit into a block defined to be a set number of pixels wide and high. The formatted text is kept in main memory. Next, the program establishes a clipping rectangle and then repeatedly writes the text out to the screen at random locations; hence, portions of the text block fall outside the clipping region. The program executes the test twice. In the first part, it displays the text in a single color with an opaque background; in the second, it cycles through the entire palette while displaying text with a transparent background.

Gauging Performance

The results of these tests on the boards in this review that support TIGA 1.1 are shown in table A. Where a board had more than one pixel depth configurable through TIGA, we ran it in both 4- and 8-bit modes. We tested AT boards on a Compaq 386/20, and the MCA boards on a 16-MHz IBM PS/2 Model 80.

Each board showed consistent performance from test to test. Results were surprisingly unlike those generated by our PageMaker application tests, despite these boards' use of the same TIGA Windows driver. The PageMaker tests seem more dependent on the ability of the Windows driver to properly utilize the 34010.

The MCA-based Pepper Pro1024/MC demonstrated outstanding speed. Its bus and 60-MHz processor contributed to excellent performance on all but the text benchmarks. The results are even more impressive when you consider that the board was run on a machine with a slower main processor than any of the others and that the text benchmarks are relatively main processor–dependent.

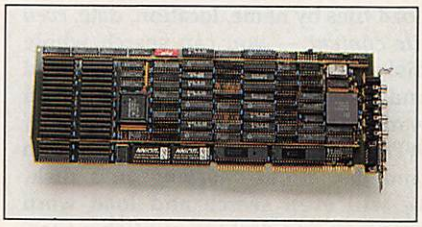
Number Nine's Pepper Pro1280 and the Control Systems Artist TI12 ran at nearly a dead heat. Although the two boards turned in virtually identical times on most benchmarks, the Control Systems board had a slight edge. The Pepper Pro1280 did not have enough DRAM to store the polygon definitions in 8-bit mode, and so it could not execute the Polygon benchmark. PC Tech's Color 34010 Board ran noticeably slower than the others, as its lower processor clock rate (40 MHz versus 50 MHz) might lead you to predict.

Differences between 4- and 8-bit modes were only apparent on benchmarks that had a high ratio of pixel manipulation to calculation. The calculation-intensive clipped lines and clipped ellipses tests, notably, did not seem pixel-depth-dependent at all.

Windows is not the Matrox board's strong suit. It's rather slow in redrawing bit maps and appears to have coarse control over its color selection. As for speed, it ranked near the bottom, along with the IMAgraph board.

Overall, we liked the Matrox PG-1281. It would be a good choice for serious AutoCAD users due to its speed and exceptionally clear display. The list price of $4595 includes more memory than any other board we tested. OEMs and value-added resellers will like the complete documentation, which makes it easier to install in complex CAD systems.

Number Nine Pepper Pro1280



The Pepper Pro1280 is a veteran among 34010-based graphics cards. Introduced in December 1986, the Pro1280 is still a top performer despite its limited DRAM capability. The board as we tested it sells for $2995; a unit with a larger lookup table and a 16-million-color palette costs $3495. The board ships with TIGA and proprietary NNIOS drivers; current versions also bundle in TIGA drivers for Windows and AutoCAD. One drawback of this older unit is its inability to work with VGA cards. Not only does it not support pass-through, it can't even coexist with a VGA in the same system.

Prices are fairly low because the board includes only 128K bytes of instruction memory; the next lowest in the 1280- by 1024-pixel class is the IMAgraph board's 512K bytes. And while other models provide for RAM expansion, the Pro1280's DRAM capacity is fixed. This kept us from running our Polygon benchmark under TIGA and may restrict other programs that require an on-board (but off-screen) memory workspace.

Number Nine's Power9 display-list driver does not even attempt to use on-board memory for display-list storage. It keeps the display list either in expanded memory or on disk. One sharp feature that we found surprisingly rare among these boards was the ability to use the disk as necessary if the expanded-memory display list overflows. Most drivers simply disable display-list processing

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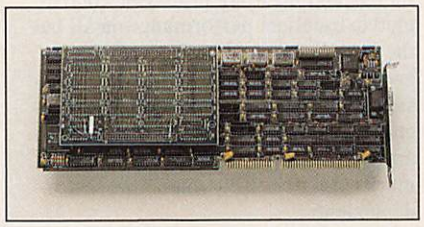
entirely if the drawing is too complex.

Power9 for AutoCAD costs an additional $250, but it adds far better performance than the standard TIGA driver. When handed 512K bytes of simulated expanded memory and using the driver's overflow-to-disk capability, the board and driver performed consistently well, especially with the large file. Power9 adds its own zoom, pan, and other display-list commands to AutoCAD. These commands duplicate the drawing (the section covered by the display list) in a small viewport at the corner of the screen. To pan or zoom, you drag or resize a highlighted box within the viewport. If you use these commands, you need to click and drag to select views; you lose AutoCAD's command-line-entry precision.

The Pepper Pro1280 runs under the TIGA Windows driver. Except for the bit map–dragging bug experienced by all boards using this driver, the tests ran smoothly. The Pepper Pro1280 tied the far more expensive Artist TI12 on one PageMaker test and topped the entire field on the other.

1024 by 768 Pixels

Compaq Advanced Graphics 1024



Our AG 1024 board was equipped with the optional 512K-byte memory-expansion module. The standard board supports 16 colors in its highest resolution. The optional memory brings the number up to 256. This board prefers to coexist with a VGA card and comes with a connection cable to pass the VGA video through to a single monitor.

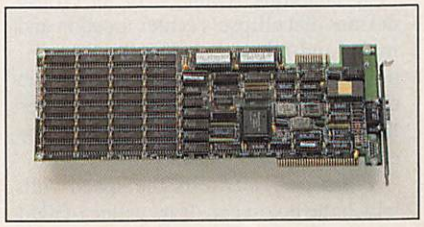
AutoCAD's performance on this board was quite respectable. Redraw times were among the fastest of any of the display boards. Pan and zoom performance was in the low to middle of the pack. The AutoCAD drivers provide QZOOM and QPAN, display-list versions of the standard AutoCAD functions. QZOOM uses the display list and your mouse to handle local zooming in geometric progression. Unlike AutoCAD's zoom, which allows for an arbitrary window, QZOOM provides a zoom "box" that you can set from 2× to 32×. QPAN lets you slide the QZOOM box around within the window. Overall, it improves on the standard zoom and pan, but not as much as IMAzoom does.

Display lists are stored outside the board, in expanded memory. The driver configuration program lets you allocate from 0 to 32 megabytes of expanded memory. Most boards we tested disable the display-list handling when they run out of memory. The Compaq driver is one of two that can overflow the display list to a disk file. The combination gives AutoCAD a real performance boost.

Windows and PageMaker work very well on the AG 1024. The board is the fastest of the 1024- by 768-pixel boards, although one of the 1280- by 1024-pixel boards was faster. The color display was crisp, and the text was easy to read.

Compaq is known for many things—excellent quality, compatibility, and reliability, to name a few. The AG 1024 has all this, and at a reasonable price to boot. The AG 1024 isn't quite the cheapest board we tested, but it's close to the fastest. It would be a good choice for people who feel comfortable buying hardware with a household name on it.

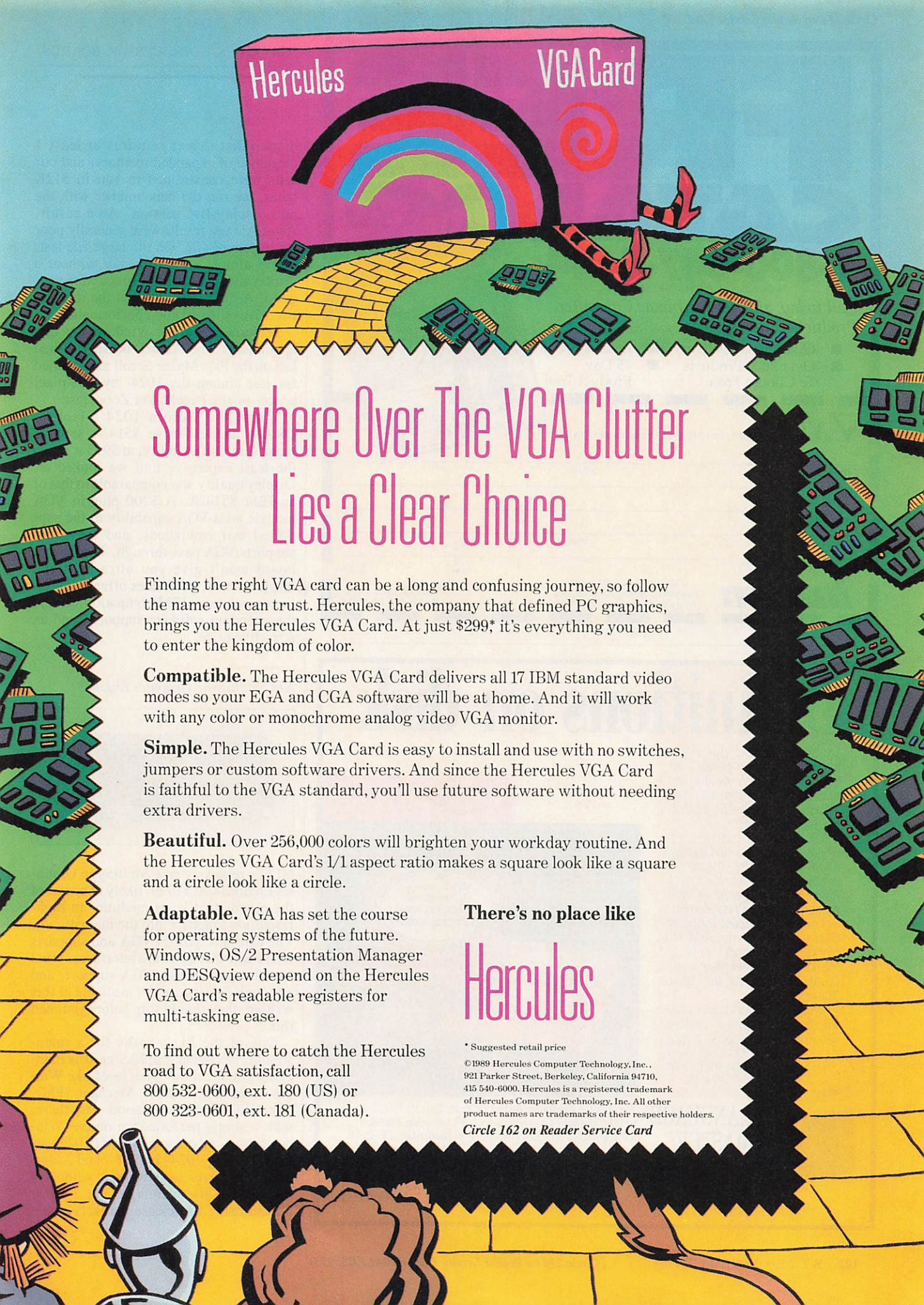
Enertronics Research Aurora 1024



Only a few 34010-based boards support IBM's 8514/A AI software interface specification. The Aurora 1024 is the only board in this review that uses the 8514/A AI as its exclusive connection to software applications. In fact, with its 1024- by 768-pixel interlaced resolution and no instruction memory, the Aurora 1024 is essentially an 8514/A clone. Since IBM markets its 8514/A adapters exclusively for the PS/2 series, the Aurora 1024 represents one of the few ways that current users can get 8514/A graphics on XT- or AT-class machines.

We tested the Aurora 1024 using ADI and Windows drivers provided by Enertronics, although you have the option of using standard 8514/A drivers. Enertronics actually ships two ADI drivers—one that supports an expanded-memory display list and one that does not. The

continued



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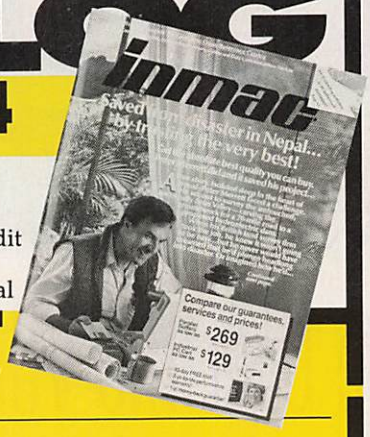
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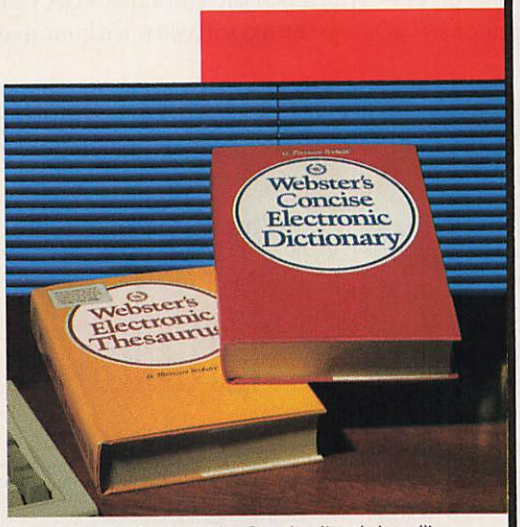
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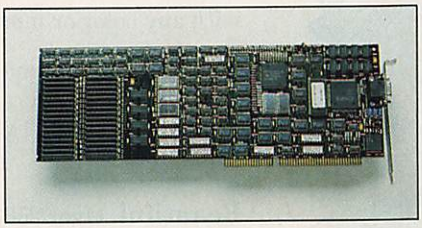
Franklin™ Software

display-list driver requires at least 1 megabyte of expanded memory, and our tests were constrained to run in 512K bytes; we ran the benchmarks with the non-display-list version. As a result, AutoCAD test results were generally poor for the small file. On the large file test, where almost all boards ran without a display list, the Aurora's times were very good. A qualitative look at the display-list drives showed good performance.

Performance under Windows was disappointing. The Aurora board finished last on the PageMaker Scroll test and tied for last among the 1024- by 768-pixel boards on the PageMaker Zoom test.

While the Aurora 1024's lack of DRAM and exclusive 8514/A support mean limited flexibility, at $995 it's also the least expensive unit we looked at. Display quality was comparable to that of an IBM 8514/A. A $200 plug-in VGA module adds VGA capability to the supported text emulations, and the board supports VGA pass-through. The Aurora board won't give you ultra-high-end display power, but it does offer medium-high resolution, IBM compatibility (and the attendant software support), and an attractive price.

NEC MultiSync Graphics Engine



NEC's relatively new MultiSync Graphics Engine is, at $1999, likely to be one of the boards that leads medium- to high-resolution graphics into the mainstream. The card has built-in VGA and supports DGIS and CGI software interfaces. NEC has also announced TIGA support, and although drivers are not available at this writing, they should ship before you read this.

One of the likely tasks for a mainstream intelligent graphics card is managing graphical user interfaces like Windows and Presentation Manager (PM). The NEC board has a good start there, with a strong performance on our Windows test—only Compaq's AG 1024 was faster among 1024- by 768-pixel adapters. The driver also worked without a hitch. NEC also claims to have a driver almost ready for release that accelerates

continued

Circle 294 on Reader Service Card (DEALERS: 295)

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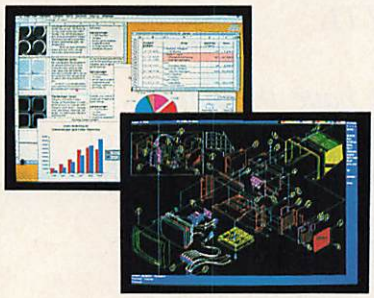
Increasing sophistication in the use of personal computers for general business applications, CAD and DTP has led to a growing demand for better resolution and larger display devices. Combining wide compatibility and functionality with the latest ergonomic design, the FLEXSCAN 9400, with a maximum resolution of 1280 dots × 1024 lines, will not only meet these requirements but those of the next generation of advanced business PCs.

Wide compatibility

With a wide Horizontal scan frequency range (30-65kHz), the FLEXSCAN 9400 is compatible with most signal sources, including standard VGA, extended VGA, 8514/A, Ultra Hi-Res Graphics controllers for PCs, as well as the Macintosh II and its Hi-Res Graphics Adapters.
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Latest Technology

By adopting a DBF (Dynamic Beam Forming) Electron Gun CRT, resolution, convergence and brightness in the screen corners have been improved over a standard CRT. By combining this with Dynamic Focusing Circuitry, the FLEXSCAN 9400 will give a sharp and bright display image over the entire screen.
The 9400 also has 2 input terminals (BNC×5 and D-sub 9 pin) which can be easily selected from a front mounted switch. This convenient feature enables the professional user to have a one-monitor solution even if he runs both Ultra Hi-Res and general business applications.



Ergonomics and Utility

The CRT of the 9400 has a special coating which not only reduces reflection but also the static electricity generated on the surface of the screen.

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Scan Frequency	H:30kHz~65kHz(Automatic adjustment) V:55Hz~90Hz (Automatic adjustment)
Standard Display Size	360mm×270mm
Recommended Resolution	1280dots×1024lines
Video Band Width	120MHz
Linearity	±5%max. (for Horizontal scan frequency ranges 30~37/48~50/63~65kHz only)
Dimensions	496mm(W)×561mm(D)×471mm(H)(at tilt 0°)
Net Weight	37kg

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Circle 246 on Reader Service Card (DEALERS: 247)

PM performance.

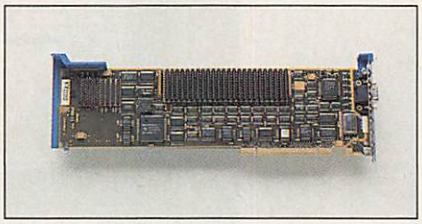
Under AutoCAD, benchmark results were mixed. As a caveat to all these results, we were using the only NEC driver available, which only supported release 9 functions. A release 10 driver is on the list of planned enhancements. NEC's display-list driver adds additional commands to AutoCAD and uses expanded memory exclusively. On the small file, where the display list fit within our 512K-byte limit, performance was outstanding. Redraw, pan, and zoom operations all executed in around 1 second.

Where the display-list commands could not be used, however (on the large file test), pan and zoom performance was abysmal. This is because the driver forces AutoCAD to regenerate the drawing when zooming on a three-dimensional display.

Another glitch that may or may not be related to differences between release 9 and release 10 came in mixing AutoCAD and NEC extended commands. If you mix NEC pan and zoom commands with standard AutoCAD pan and zoom commands, AutoCAD will lose track of the proper image position.

Overall, the NEC board seems to offer great potential at a good price. Although the driver will limit you if you're using AutoCAD release 10, the underlying hardware performs solidly. If NEC puts all the planned software support in place, the MultiSync Graphics Engine should be an outstanding product.

Number Nine Pepper Pro1024/MC



This is one of two MCA boards that we looked at. We don't have any way of comparing it to most of the other boards in this review, nor can we compare it to its AT-bus cousin, the Pepper Pro1280. The only fair comparison is to the other MCA board we reviewed, the Vermont Microsystems Cobra/2 HS. In our AutoCAD tests, the Pro1024/MC blew the doors off the Cobra/2 HS. The drivers are very similar, if not identical, to those provided with the Pepper Pro1280. We definitely recommend using the optional ($250) Power9 display-list driver.

Installing the Pro1024/MC is simply a matter of plugging the board into the MCA slot with the VGA pass-through. Once that's done, you boot the computer with the reference disk and set the slot configuration, and you're set. Batch files handle installing the required driver software.

PageMaker ran well, and the display was clear and comfortable to look at. Windows installed easily and ran with no surprises.

Our low-level TIGA tests also ran without a hitch. It's interesting to note that even though the Model 80 is slightly slower than the Compaq 386/20, the Pepper Pro1024/MC completed the TIGA benchmarks faster than any other board in the test.

The list price of $2495 includes 512K bytes of memory and standard drivers for AutoCAD and Windows. Those who use

continued

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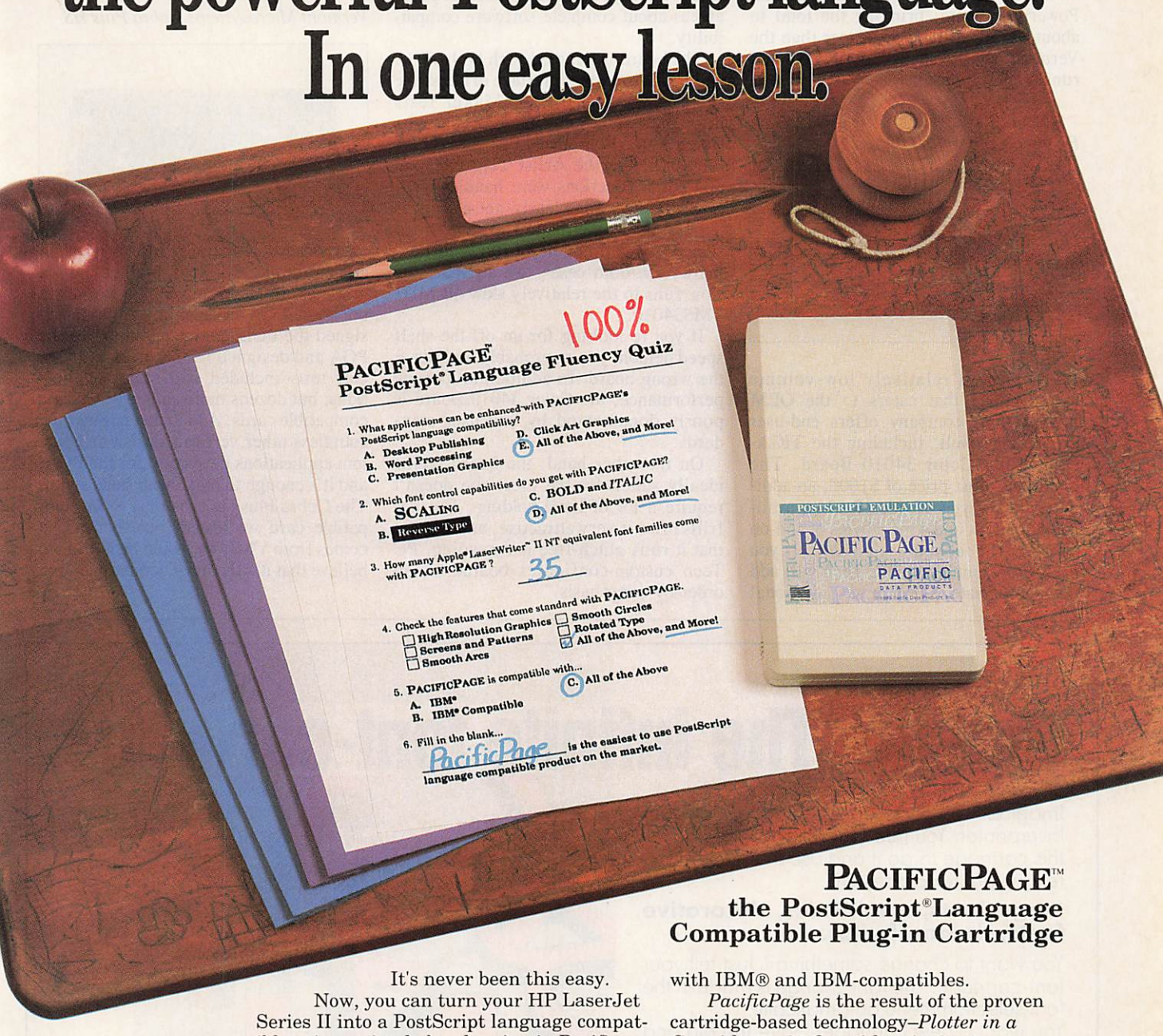


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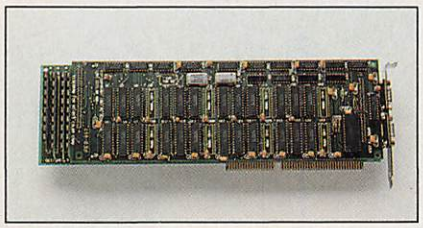
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Circle 267 on Reader Service Card (DEALERS: 268)

AutoCAD will want to add the optional Power9 software, bringing the total to about $2750. Still, it's cheaper than the Vermont Microsystems Cobra/2 HS and runs markedly faster.

PC Tech Color 34010 Board



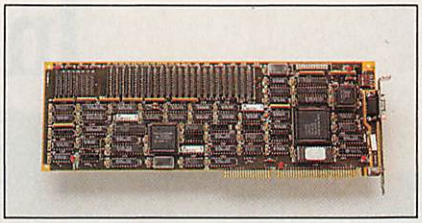
PC Tech is a relatively low-volume manufacturer that caters to the OEM market. The company offers end-user products as well, including the TIGA-compatible Color 34010 Board. The board has a list price of $1600; an additional 256K bytes of video RAM is available for $250, and 4 megabytes of add-on DRAM will set you back $1200. If you need CGA emulation, PC Tech will add the appropriate ROM at no additional charge, but the company makes no guarantees about complete software compatibility.

The board is bundled with both TIGA and DGIS software interface drivers. We ran AutoCAD and PageMaker tests through the TIGA interface. Because the Color 34010 Board used the same TIGA ADI driver as the Artist TI12 did, pan and zoom functions were handicapped. Still, the board is clearly not as fast as most of its competition. The same trend showed on our low-level TIGA benchmarks—in both cases, we attribute the slow runs to the relatively slow 40-MHz TMS34010.

If you're looking for an off-the-shelf speed demon, you're probably looking at the wrong board. In addition to its slow performance, the Color 34010 Board is poorly documented by end-user standards.

On the other hand, the board seems ideally suited for the user who doesn't require a lot of hand-holding. The no-frills price is very attractive, and the fact that it runs glitch-free is appealing. PC Tech custom-configures boards on an order-by-order basis.

Vermont Microsystems Cobra Plus HS



Vermont Microsystems, Inc. is no newcomer to the world of high-resolution graphics. In fact, the company wrote the book on PGA compatibility. VMI designed the PGL language that drives the PGA and designed IBM's original PGA. Our tests included two major applications, but dozens more support PGA and compatible cards. Add to that number the countless other vertical-market and custom applications developed for the PGA, and it's enough to make your head swim. The Cobra Plus isn't the only PGA-compatible card we tested, but, because it comes from VMI, we would be willing to believe that it's the most compatible.

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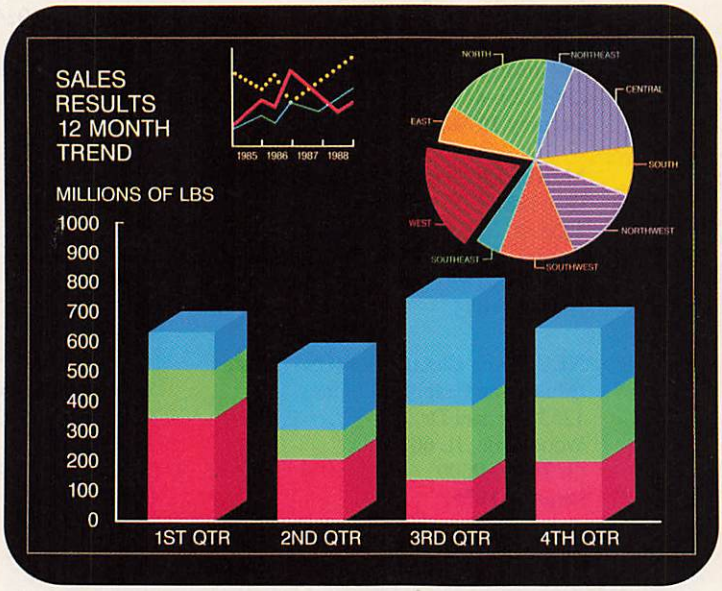


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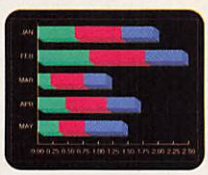
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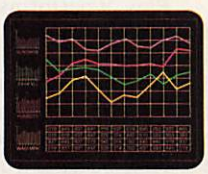
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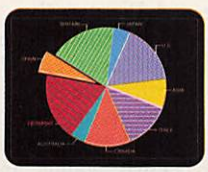
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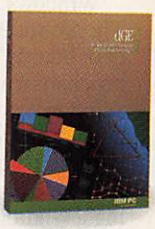
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Inquiry 1074.

Matrox Electronic Systems Ltd.
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Dorval, Quebec H9P 2T4, Canada
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Inquiry 1075.

NEC Home Electronics (USA), Inc.
(MultiSync Graphics Engine)
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Number Nine Computer Corp.
(Pepper Pro1024/MC, Pepper Pro1280)
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(617) 492-0999
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PC Tech, Inc.
(Color 34010 Board)
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(612) 345-4555
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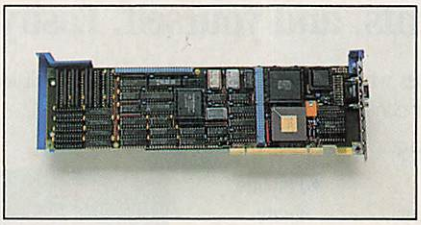
Unfortunately, our tests showed disappointing performance. AutoCAD release 10 runs flawlessly on the Cobra Plus, although it turns in the slowest times of any board with full release-10 drivers. We had hoped for better performance from a 60-MHz 34010. The board is easy to install, and VMI's installation program takes care of the device and application drivers.

Windows is something else altogether. The Cobra Plus and Cobra/2 are the only two boards that displayed any serious problems running our PageMaker tests. Windows does its scrolling by copying large blocks of display memory from place to place. Several times, we noticed that the Cobra Plus had difficulty scrolling a window that was overlapped by another window. Parts of the lower (moving) windows would sporadically appear within the white spaces of the stationary upper window.

In the scheme of things, that's far from disastrous. But several PageMaker utility windows rely on tiny icons of arrows and triangles to control different aspects of operation. VMI's Windows/286 driver was unable to render many of these little objects, replacing them with much larger black rectangles. Setting tabs was the worst case. It's hard enough to grab a 1-pixel-wide arrow with the mouse when you can see it. [Editor's note: *Since this was written, VMI has announced a new Windows driver that it claims fixes the pixel-wide arrow problem. The driver should be available by the time you read this.*]

The Cobra Plus could be faster. At $3395, it's not inexpensive. On the other hand, the display quality was excellent, and we feel confident that if anyone can build a 100 percent PGA-compatible board, VMI can.

Vermont Microsystems Cobra/2 HS



This is the MCA version of the Cobra Plus board. It is based on the same 60-MHz 34010 as the Cobra Plus, and, with nearly the same drivers as on the Cobra Plus, it performs identically.

The Cobra/2 costs $3395. For less money, the Number Nine Pepper Pro-1024/MC runs much better. If you need absolute PGA compatibility, this card is a safe bet, but otherwise, the Number Nine board is a better deal.

A Perspective

In terms of performance, all these boards exceed VGA. Not so surprisingly, prices are also in a different league. But before you buy, get the latest information from each vendor—these boards are still fairly young, and capabilities and software support change rapidly.

The Number Nine Pepper Pro1280 seems to be the best overall choice for an off-the-shelf, high-resolution board. While it's an older design and lacks some on-board DRAM, its capable display-list driver makes good use of other system resources, so AutoCAD performance is excellent. The Pepper Pro1280 is also comparatively inexpensive.

If you need a top-of-the-line platform for development, you may want to consider Matrox's PG-1281. While significantly more expensive than the Pepper Pro1280, this board has powerful hardware enhancements and comes with a vast 1.5 megabytes of DRAM on-board.

For medium to high (1024- by 768-pixel) resolution, Compaq's Advanced Graphics 1024 is a fine choice. Its combination of speed, price, and ease of use is hard to beat. Unfortunately, Compaq cannot guarantee compatibility if you don't have a Compaq 80286 or 80386.

Of the two MCA cards we looked at, The Number Nine Pepper Pro1024/MC gets the nod. It performed well under standard applications and showed great promise for use under TIGA.

Two of the stumbling blocks in achieving such high-resolution displays have been the cost of memory and the processing power that's needed to manipulate it. 34010 boards are one way to get superior graphics without crippling your CPU. Large display memories move you more than a bit beyond VGA. ■

Steve Apiki and Howard Eglowstein are BYTE Lab testing editors. Rick Grehan is director of the BYTE Lab. You can reach them on BIX as "apiki," "heglowstein," and "rick_g," respectively.

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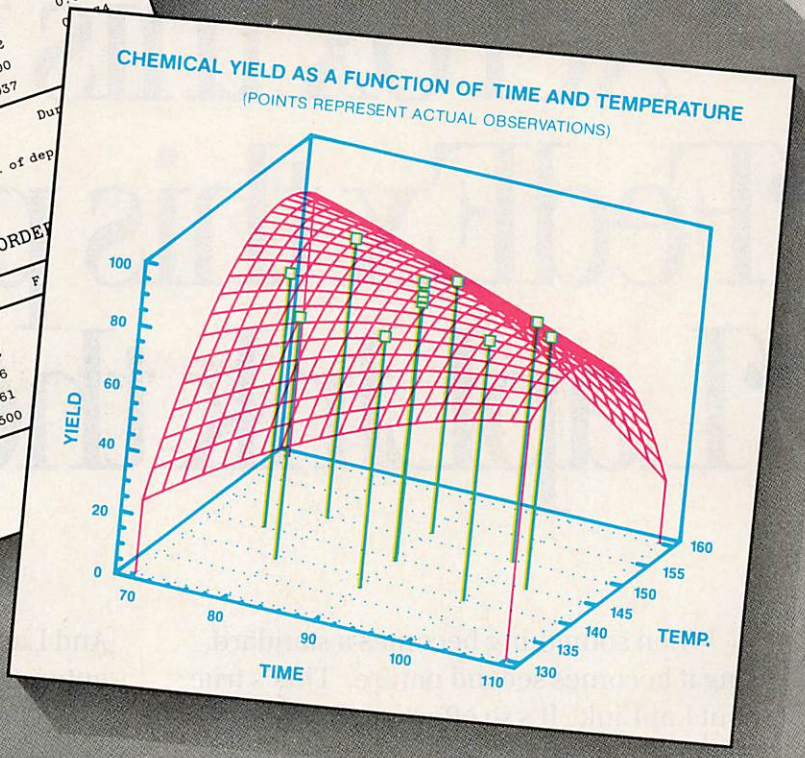
MODEL FITTING RESULTS FOR: YIELD

INDEPENDENT VARIABLE	COEFFICIENT	STD. ERROR	T-VALUE	SIG. LEVEL
CONSTANT	-3977.847583	747.932209	-5.3185	0.0018
time	17.862499	3.288094	5.4325	0.0016
time^2	-0.021469	0.008136	-2.6386	0.0386
temp	44.997502	9.614533	4.6802	
temp^2	-0.124651	0.032546	-3.8300	
time*temp	-0.0975	0.020297	-4.8037	

R-SQ. (ADJ.) = 0.7865 SE = 2.029674 MAE = 1.173868 Dur
Previously: 0.0000 0.000000 0.000000
12 observations fitted, forecast(s) computed for 0 missing val. of dep

FURTHER ANOVA FOR VARIABLES IN THE ORDER

SOURCE	SUM OF SQUARES	DF	MEAN SQ.	F
time	15.3890909	1	15.389091	
time^2	15.6011921	1	15.601192	
temp	1.0765657	1	1.076566	
temp^2	60.4298606	1	60.429861	
time*temp	95.0625000	1	95.062500	
Model	187.559209	5		



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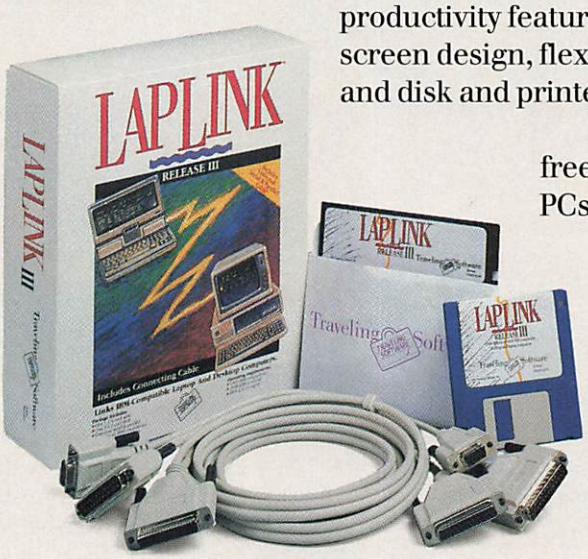
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DEC's RISC Powerhouse

The DECstation brings RISC power to Unix workstations at PC prices

Ben Smith and Rob Mitchell



The DECstation's RISC-based performance and low starting price of $7950 are turning heads in the workstation world. Its keyboard, however, is disappointing. It has no Escape key, and many keys are in nonstandard positions or have no function.

The DECstation, Digital Equipment Corp.'s lowest-priced high-performance Unix workstation yet, represents a radical approach to development and marketing for the world's second largest computer manufacturer. It also represents a new era in personal computing and a new competitive challenge for low-end workstation vendors.

The DECstation is the first machine from DEC designed to run *only* Unix. It's also the first DEC workstation to use a CPU from an outside vendor (the MIPS R2000 RISC CPU). These facts alone make the DECstation noteworthy, but it is a groundbreaking machine in other ways as well.

With a starting price of $7950, the DECstation is one of the first RISC-based workstations that are in the price range of personal computers; its introduction has hit the workstation community like a bombshell. Dubbed the "Sun Killer," the DECstation has an excellent price/performance ratio, and its functionality is equivalent to Sun's SPARCStation 1 (see "Two Powerful Systems from Sun," May BYTE).

Heavy Metal

DEC sells two versions of the DECstation: the 2100 and the 3100. With the exception of CPU and memory speed, these machines are identical. The entry-level 2100 is a diskless workstation. It includes an R2010 FPU, 8 megabytes of memory, a 15-inch monochrome monitor, a SCSI connector, switch-selectable "thick-wire" and "thin-wire" Ethernet interfaces, two serial ports, a mouse, a keyboard, and Ultrix Workstation Software for $7950 ($11,900 for the 3100). The price tag for our test machine, a fully configured DECstation 3100, was $39,300—more than three times the 3100's base price.

At the heart of the DECstation lies a MIPS R2000 RISC CPU, an R2010 math coprocessor, and an R2020 write buffer (see photo 1). The CPU runs at 12.5 MHz on the DECstation 2100 and at 16.67 MHz on the 3100; DEC rates the machines at 10 and 14 million instructions per second, respectively. The FPU puts in a double-precision LINPACK performance of 1.2 million floating-point operations per second on the 2100 and 1.6 MFLOPS on the 3100.

continued

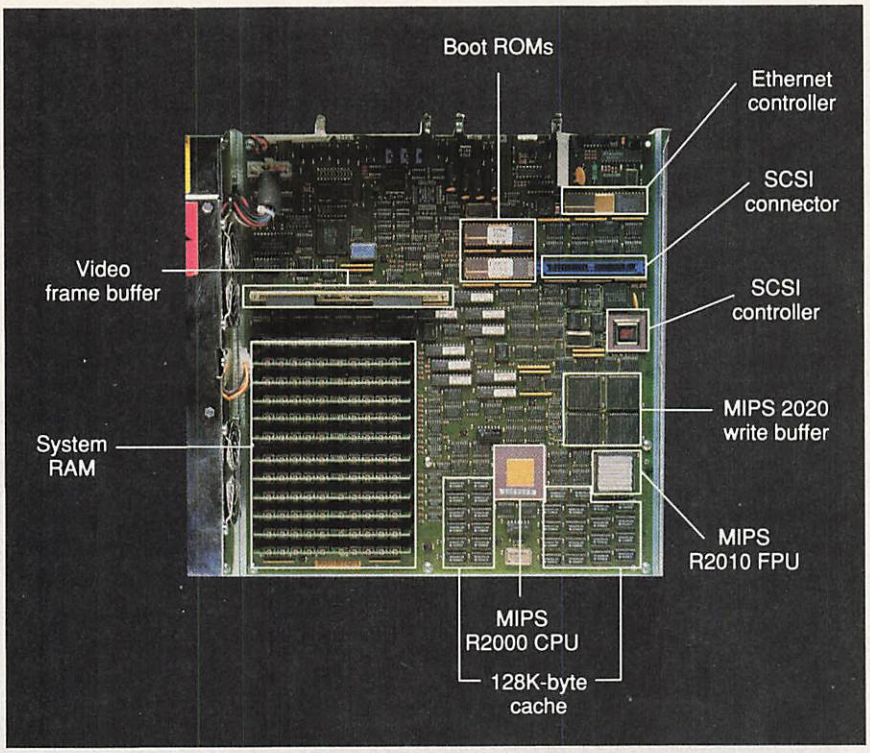


Photo 1: *With the exception of its CPU clock speed and its faster cache, the DECstation 3100 is exactly the same as the 2100. Note the double-mounted single in-line memory modules and the heat sink on the FPU.*

Unlike Sun's SPARCStation 1, the DECstation's 32-bit memory bus doesn't support direct memory access, and it doesn't have any expansion slots.

System memory consists of 120-nanosecond parity DRAMs mounted on double-sided, single in-line memory modules; you can upgrade in 4-megabyte increments up to the 24-megabyte maximum. Our DECstation 3100 review machine came fully populated. Also standard are a 64K-byte data cache and a 64K-byte instruction cache. DEC uses 35-ns static RAM (SRAM) chips in the 2100 and 23-ns chips in the 3100.

Hidden inside the box is a small shelf that can hold two 104-megabyte SCSI hard disk drives ($2400 each) that have an average access time of 33 milliseconds. DEC recommends using these for page swapping in a Network File System (NFS) environment, but you can also use them to store data. A SCSI connector lets you attach additional devices. Our unit included one internal hard disk drive, a 330-megabyte 5¼-inch external hard disk drive with an average access time of 24 ms ($6500), and an external 95-megabyte streaming-tape subsystem ($3500). A 600-megabyte CD-ROM drive is also available for $1600. The DECstation supports up to four storage devices.

The external hard disk drive can run asynchronously or synchronously. In synchronous mode, it has an aggregate transfer rate of 4 megabytes per second. (The DECstation can only retrieve data at up to 1.25 megabytes per second, so this performance is noticeable only if you're running multiple disk drives.)

Our test machine included a 1024- by 864-pixel, 60-Hz, noninterlaced 15-inch analog color monitor (a 15-inch monochrome monitor is standard). DEC also offers 19-inch color and monochrome monitors. The 8-bit color system uses a 1-megabyte frame buffer to display up to 256 colors simultaneously from a palette of 16.7 million. In monochrome mode, the DECstation uses a 256K-byte single-plane frame buffer. The graphics subsystem doesn't include a video controller, relying instead on the CPU.

In addition to the SCSI connector, a complement of I/O ports graces the back of the system unit, including both standard Ethernet interfaces, a 15-pin D-sub video port, mouse and keyboard interfaces, and two serial ports (designated as printer and modem ports). Regrettably, the DECstation lacks a parallel port, and the serial ports use a proprietary six-wire interface that looks like a modified RS-442 jack. You'll need a special DB-25 adapter and cable ($37) to use the ports with non-DEC serial devices.

Aesthetically, the DECstation is sleek and attractive; the system unit has an 18- by 15½-inch footprint and rises just 4 inches off the desktop. The external hard disk drive and tape systems are housed in stackable boxes that measure 12½ by 11½ by 5½ inches. Each external device includes its own power supply. A handle at the rear of each unit makes the drives easy to carry; it snaps down over the power and SCSI cables when not in use, locking them into place.

Only the DECstation logo and green power light adorn the front of the unit; the power and reset switches are on the rear panel. The nonstandard 105-key keyboard is a bit of a kludge; it's essentially a VAXstation keyboard that DEC has adapted for use in a Unix environment—with mixed results. For example, it has no Escape key; to generate an Escape, you must press the Control and left bracket keys. Many other commonly used keys are located in unusual positions, and many keys are specific to DEC's VMS operating system and have no function at all under Ultrix.

Ultrix

The DECstation's Ultrix Workstation Software includes Ultrix-32, Ultrix/DECwindows, a C compiler, X Window System 11, X User Interface (XUI), and implementations of TCP/IP and NFS.

Ultrix-32, the DECstation's operating system, is a robust implementation of BSD Unix that also includes library routines and commands from System V.3. Ultrix has its own versions of `/bin/sh` and `/bin/csh`. DEC also provides the standard Unix shells, but having both means that you must pay careful attention to which shell you're running. The obvious advantage to having two versions is the enhancements that DEC provides. The disadvantage is that it's difficult to move between Ultrix machines and other Unix machines. Enhancements are barbed hooks for new users who don't realize what they're getting into. The adoption of the AT&T Korn shell would offer far more to everyone.

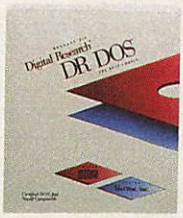
Ultrix for DEC's RISC machines contains special commands for optimizing program execution. Two examples are `pixie`, a program for analyzing program block use, and `cord2`, a program that takes information that `pixie` generates and rearranges the basic blocks to facilitate better cache mapping. Also included are many utilities for E-mail, network mail, and *message handling* (the Ultrix

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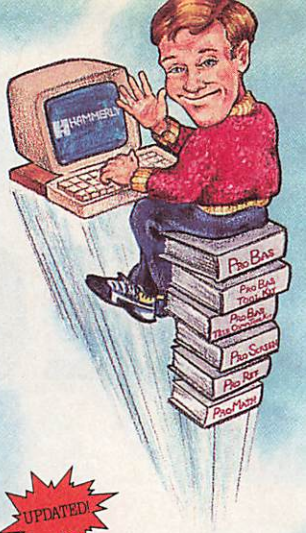
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label for a collection of single-purpose programs that send, receive, save, and retrieve E-mail messages). As with most Unix utilities, you can freely use these commands in shell scripts, thereby simplifying the task of `crontab` mail management scripts.

XUIstation

The DECstation is not intended to be a Unix process server; it's designed exclusively as an XUI server workstation. In that vein, it is DEC's brightest star, and at the moment it's the most affordable machine of its type.

Built on top of the X Window System, XUI is the distributed client/server windows standard developed at MIT. XUI is the graphical user and programming interface at the core of the Open Software Foundation's Motif (see "A Guide to GUIs," July BYTE). XUI is the precursor of Motif on DECstations.

XUI consists of a window manager; a Session Property Manager, which is a user's work environment with file and task management; a style guide for developers; and a graphical user interface compiler and resource manager to simplify development of the user interface for applications. XUI gives the DECstation its feel.

XUI is consistent with DECwindows, another implementation of the X Window System that runs under VMS. The user interface is consistent and simple to grasp. However, some of the standard utility programs aren't properly integrated. For example, when you select a file in the User Executive window and select the Notepad application, the selected file should appear; instead, the Notepad window comes up empty.

Performance

Performance is the DECstation's major selling point. Benchmark data supplied by DEC shows the DECstation 3100 outperforming both Sun's SPARCStation 1 and Hewlett-Packard's HP 9000/835. Our tests show the DECstation 2100 offering up to 85 percent of the performance of the 3100.

We subjected the DECstation 3100 to a preliminary version of the new BYTE Unix benchmarks, currently under development in the BYTE Lab. We compared both the 2100 and 3100 against our baseline development machine, an Everex 386/33 running SCO Xenix 2.3.1. Unlike our MS-DOS and Mac benchmarks, Unix benchmarks reflect not only hardware performance but also the performance of the version of Unix and the particular compiler optimization.

DECstation 2100/3100

Company
Digital Equipment Corp.
146 Main St.
Maynard, MA 01754
(508) 897-5111

Features
Processor: 12.5- or 16.67-MHz 32-bit R2000 RISC CPU; MIPS R2010 math coprocessor
Memory: 24 megabytes of 120-ns parity-checked DRAMs on double-sided SIMMs (DECstation 2100 has 8 megabytes); 64K bytes of 23-ns SRAM write-through data cache; 64K bytes of 23-ns SRAM instruction cache (SRAMs in DECstation 2100 are 35-ns)
Mass storage: External 330-megabyte SCSI hard disk drive; SCSI tape backup system; 104-megabyte internal SCSI hard disk drive
I/O interfaces: Two serial ports; thin-wire and thick-wire Ethernet ports; DB-15 video port; mouse port; SCSI port

Size
18 × 15½ × 4 inches

Price
Base DECstation 2100: $7950
Base DECstation 3100: $11,900
DECstation 3100 as reviewed: $39,300

Inquiry 851.

We found that the Everex actually outperformed the DECstation on low-level, integer-type operations (register, short, int, and long). But the DECstation was nearly five times faster on low-level floating-point operations (float and double). In random and block (sequential) memory operations, the DECstation outperformed the Everex by 10 percent to 20 percent. File operations showed similar performance. Note, however, that RISC processors do not show their true advantage over complex-instruction-set computer (CISC) processors until the compiler optimizes for RISC. The BYTE benchmarks don't reflect performance with normal RISC optimization.

Surprisingly, the margin of performance that the DECstation exhibited on the low-level operations wasn't as significant when we tested more all-inclusive operations. Our shell script test loads the system with various Unix commands and uses intermediate files for reading and writing. In these tests, the DECstation's performance was only fractionally better than the Everex's. And when it came down to our C compiler test, the Everex actually outperformed the DECstation.

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What this means is that the DECstation is exceptional at crunching numbers. However, when it comes to the more mundane operations of office and software development applications, its performance is good, but not what we would have expected.

Big- and Little-Endian

DEC stirred up a controversy when it decided to use "little-endian" memory-mapping byte order in the DECstation, as it does in the VAX. Most other workstations, such as Sun's SPARCStation 1, use "big-endian" order, the reverse byte order. Most minicomputers, mainframes, and microcomputers based on the Motorola microprocessors (such as the Macintosh) use big-endian ordering. IBM PCs, Xenix machines, and other microcomputers that use Intel processors use the little-endian method. MIPS processors can run either way.

Byte order isn't significant for executable binary files (compiled programs), because very few executables run on a different architecture than the one for which they were compiled. But many data files are binary. If you move them to another machine that uses the reverse byte order, the data is scrambled. In a heterogeneous computing environment, byte order is a major factor in ensuring data portability.

It would seem to be a trivial task for the data transfer program to reorder the bytes, but since the algorithm needs the size of the data structure in order to figure where to begin and end the reordering, this isn't a problem that a general-purpose data transfer program can solve. The only solution is to limit the data in a heterogeneous network to a maximum data element of a single byte. In other words, you convert all data to ASCII before moving it out to the network.

This is how file transfers are traditionally done in the Unix environment. But this approach slows down the data operations of applications running on different kinds of machines. Still, the little-endian approach makes sense for DEC, since it's more likely that its users will network the DECstation with other DEC machines than with non-DEC computers.

The Good and the Bad

The DECstation is an excellent high-performance, single-user workstation, but it's not a good choice as a compute server or file server because it doesn't handle heavy disk I/O or user loads well. DEC markets the DECstation for office or engineering use, but the documentation is oriented toward the engineer, and the machine is best suited for this type of user. You don't need a DECstation for most office applications; inexpensive terminals running off general-purpose machines can perform those tasks perfectly well.

The DECstation is ready to network using either type of Ethernet. But it can't handle more than two serial I/O devices, its lack of a parallel port prevents its use with a wide variety of printers, and its unusual keyboard is a significant limitation.

However, if outstanding performance is what you're after, the DECstation won't disappoint you. It offers more horsepower than 80386-based systems can muster, at a very competitive price. And it provides strong competition for Sun and other workstation vendors. ■

Ben Smith and Rob Mitchell are BYTE technical editors. You can reach them on BIX as "bensmith" and "rob_mitchell."

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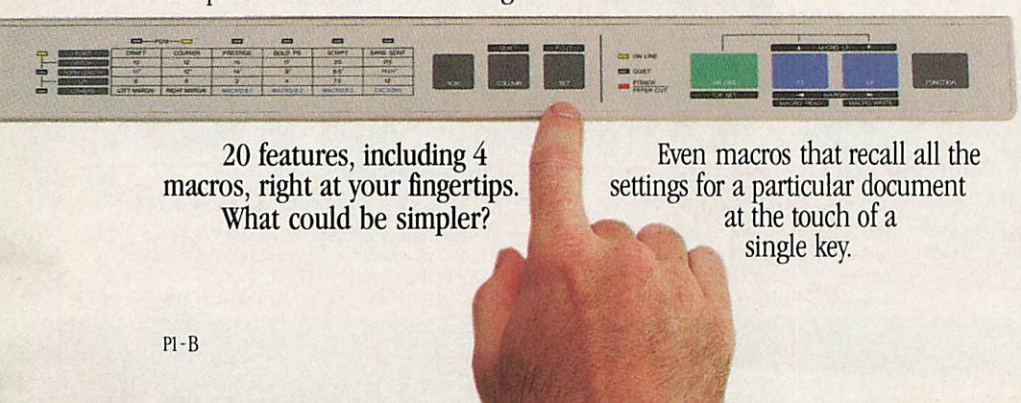
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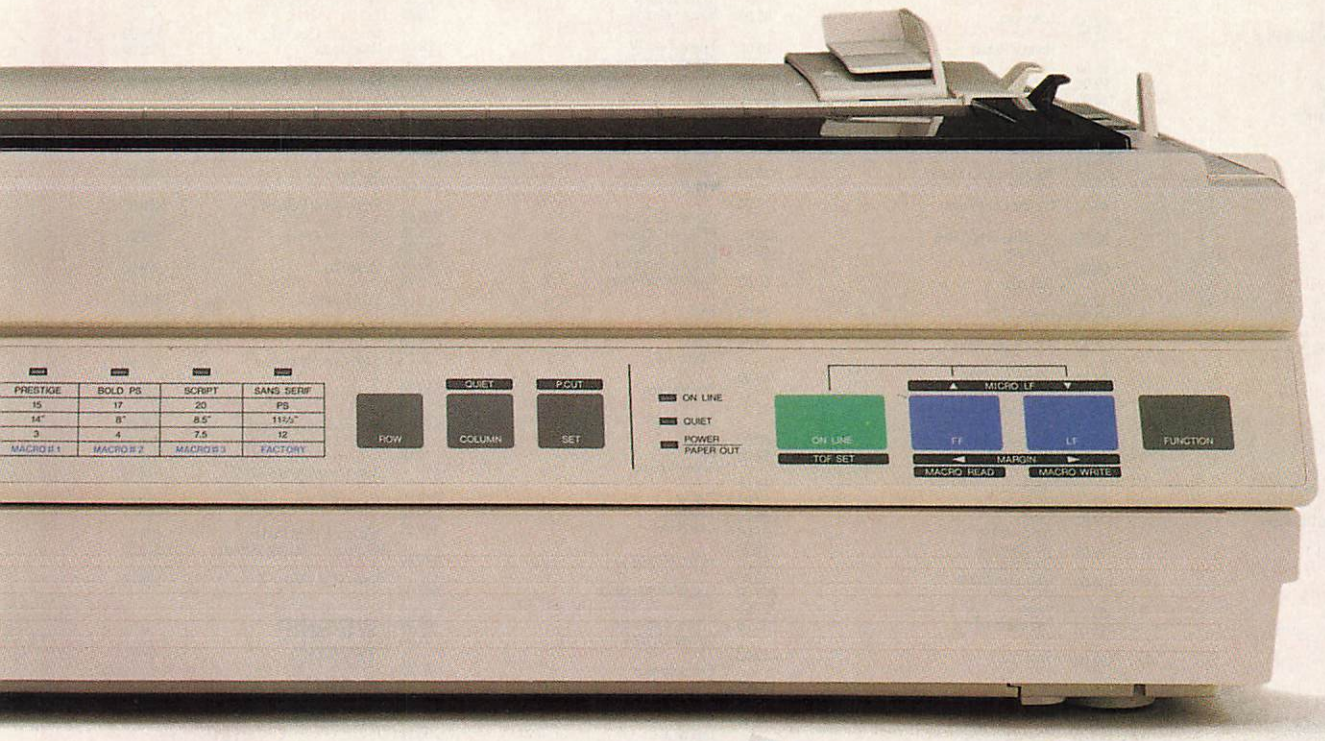
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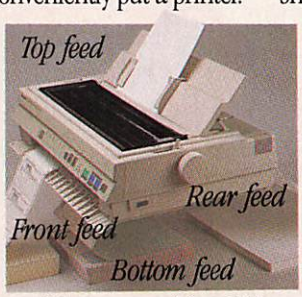
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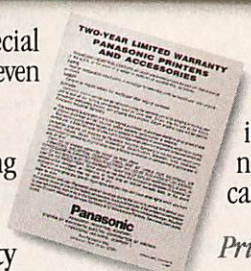


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Bill Catchings
and Mark L. Van Name



The Wyse WY-212 (left) and the TeleVideo TS2 TeleStation.

Diskless PCs make a certain amount of sense on a LAN. Rather than using local storage, a diskless PC boots from a LAN server and stores all its data on a server. With all the data in a central place, backups are easier, and, so diskless PC vendors claim, the network is more secure because workstations have no local disk drives. Diskless PCs also should cost less than standard PCs because they don't have disk drives and can use smaller power supplies.

To test these claims, we looked at two 80286-based diskless PCs: the TeleVideo TS2 TeleStation and the Wyse WY-212. Both units house a monitor and motherboard in one compact case and use ROMs to boot from a Novell NetWare file server. Both also include 1 megabyte of 120-nanosecond DRAM on the motherboard. From there, however, the configurations diverge.

The TS2 is a 10-MHz 80286 machine that includes an 8-bit Ethernet adapter and Novell boot ROM for $1695 ($1429 without the Ethernet adapter and boot ROM). The unit comes with a socket for an Intel 80287 math coprocessor; a built-in green-phosphor, 14-inch, Hercules-compatible monitor; two RS-232C serial ports; one parallel port; and a 101-key Enhanced AT-style keyboard. The network interface card occupies the unit's single 8-bit expansion slot.

The TS2's memory configuration is expandable. Two of its four banks of 256K-byte, parity-checked memory come in single in-line memory modules. You can replace those SIMMs with 1-megabyte SIMMs to bring the memory to its maximum of 2.5 megabytes.

Our test unit also included MS-DOS and GWBASIC 3.3 ($85) and a 10-MHz 80287. TeleVideo doesn't sell an 80287, so we assumed the common list price of $250 to calculate a total system cost of $2030.

The WY-212 has a 12.5-MHz 80286 CPU and and 1 megabyte of RAM for $1799. The Wyse system delivers a little more performance than the TS2 and has monochrome VGA rather than Hercules graphics. It includes a socket for either a 6- or 10-MHz Intel 80287 math coprocessor (we tested the machine with a 10-MHz 80287); a built-in, 14-inch, white-phosphor VGA monitor; a Wyse 8-bit VGA card; one parallel port; two RS-232C serial ports; and an Enhanced AT-style keyboard. The VGA card and the network interface card fill the system's two 16-bit AT-bus expansion slots.

Wyse sells the WY-212 through distributors; you can also buy the identical machine through retail channels as the Amdek System/286N from Wyse's Amdek subsidiary.

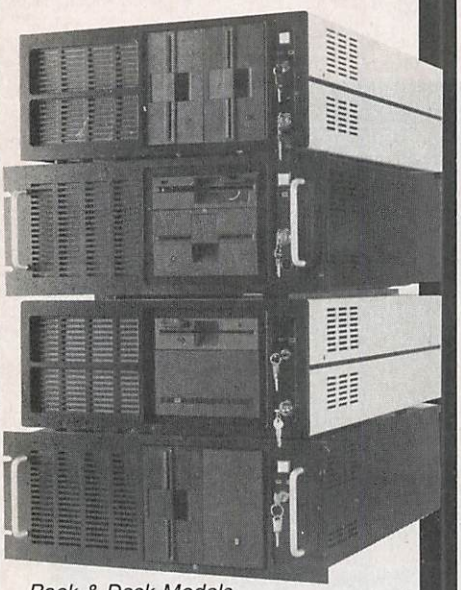
The WY-212 includes two VGA utility disks, but it doesn't come with a LAN adapter or DOS. You'll have to buy the adapter from a third party. Wyse does, however, sell Novell NetWare and 3Com

continued

Circle 175 on Reader Service Card

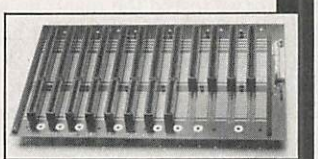
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(800) 438-9973
(408) 473-1200

Amdek Corp.
3471 North First St.
San Jose, CA 95134
(800) 722-6335
(408) 922-5700

Components
Processor: 12.5-MHz Intel 80286; socket for 6- or 10-MHz Intel 80287 math coprocessor
Memory: 1 megabyte of 16-bit 120-ns DRAM; 32K bytes of BIOS ROM
Network adapter: Not available from Wyse
Display: Built-in Wyse monochrome, white-phosphor, 14-inch VGA monitor; Wyse 8-bit VGA card
Keyboard: 102-key IBM Enhanced
I/O interfaces: Two RS-232C serial ports with DB-9 connectors; DB-25 parallel port; RJ-11 keyboard connector; two 16-bit AT-bus expansion slots for video board and LAN adapter card

Size
13 × 13 × 14 inches (height includes built-in monitor); 32 pounds

Software
VGA drivers and utilities disks

Documentation
User's guide; GWBASIC manual; MS-DOS manual

Price
Base system: $1799
System as reviewed: $2487

Inquiry 863.

TeleVideo TS2 TeleStation

Company
TeleVideo Systems, Inc.
550 East Brokaw Rd.
San Jose, CA 95161
(408) 954-8333

Components
Processor: 10-MHz 16-bit Intel 80286; socket for 8- or 10-MHz Intel 80287 math coprocessor
Memory: 1 megabyte of 16-bit 120-ns DRAM, expandable to 2.5 megabytes on the motherboard; 64K bytes of BIOS ROM
Network adapter: TeleVideo 8-bit, Novell NE-1000 compatible, Ethernet adapter with NetWare boot ROM
Display: Built-in TeleVideo monochrome, green-phosphor, 14-inch Hercules-compatible monitor; video circuitry on motherboard
Keyboard: Modified 101-key IBM Enhanced
I/O interfaces: Two RS-232C serial ports with DB-9 connectors; DB-25 parallel port; AT-style DIN keyboard connector; 8-bit AT-bus expansion slot for LAN adapter card

Size
12½ × 12¾ × 15½ inches (height includes built-in monitor); 26 pounds

Software
MS-DOS and GWBASIC 3.3 ($85)

Documentation
User's guide

Price
Base system: $1695
System as reviewed: $2030

Inquiry 864.

3+Share boot ROM chips for $40 each. These chips fit into a socket in the Western Digital EtherCard Plus 8-bit Ethernet board (WD8003EBT); a spokesperson from Wyse said that the chips will often work in other network adapters as well. Our evaluation unit included the $438 WD8003EBT card with a Wyse NetWare boot ROM. Wyse doesn't sell an 80287, so we added $250 to get a total system price of $2487.

The WY-212's memory is fixed; it limits you to 1 megabyte with no parity checking. That's not much memory these days, but Wyse at least lets you configure the 384K bytes of it above 640K bytes as extended memory.

Neither system compares well on price with many low-cost AT clones. Furthermore, in this day of 20-MHz 80286s, neither system is especially fast: Both units run with one wait state.

A Look Inside

The first thing you notice about these systems is how small they are. Both monitors attach directly to bases on necks that tilt and swivel. Those bases have a small footprint—13 inches square for the WY-212, and 12½ by 12¾ inches for the TS2.

The TS2 is no harder to open than a standard PC, although the monitor makes the task a bit awkward. Fortunately, once you remove the six screws from the bottom and the two from the back,

Wyse WY-212, TeleVideo TS2 TeleStation

LOW-LEVEL PERFORMANCE[1]

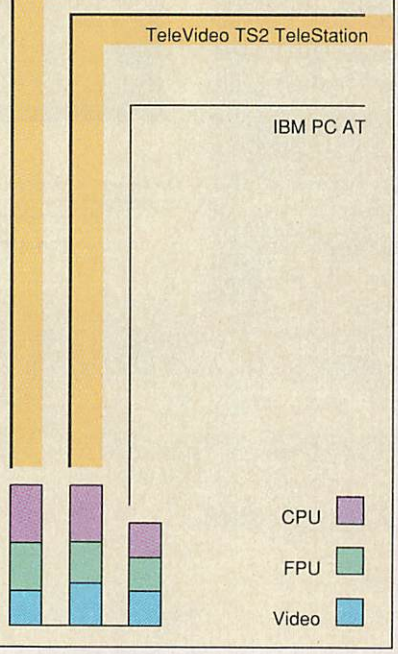
CPU	WY-212	TS2
Matrix	7.40	7.89
String Move		
Byte-wide	50.99	53.65
Word-wide:		
Odd-bnd.	51.01	53.60
Even-bnd.	25.52	26.84
Sieve	46.74	44.87
Sort	36.77	35.04
Index:	**1.68**	**1.64**

FLOATING POINT	WY-212	TS2
Math	34.29	39.62
Error[2]		
Sine(*x*)	13.97	16.60
Error		
e^x	12.19	14.28
Error		
Index:	**1.40**	**1.19**

VIDEO	WY-212	TS2
Text		
Mode 0	12.10	N/A
Mode 1	12.10	N/A
Mode 2	11.86	N/A
Mode 3	11.85	N/A
Mode 7	N/A	12.31
Graphics		
CGA:		
Mode 4	3.39	N/A
Mode 5	3.40	N/A
Mode 6	3.57	N/A
EGA:		
Mode 13	5.77	N/A
Mode 14	6.30	N/A
Mode 15	N/A	N/A
Mode 16	6.30	N/A
VGA:		
Mode 18	6.61	N/A
Mode 19	3.66	N/A
Hercules	N/A	3.10
Index:	**1.01**	**1.24**

N/A=Not applicable.
[1] All times are in seconds. Figures were generated using the 8088/8086 version (1.1) of Small-C.
[2]The errors for Floating Point indicate the difference between expected and actual values, correct to 10 digits or rounded to 2 digits.

For a full description of all the benchmarks, see "Introducing the New BYTE Benchmarks," June 1988 BYTE.



you can put the monitor portion of the case aside.

Inside, however, the TS2 is very different from most PCs. There are no drive bays, no fan, and only one horizontally mounted expansion slot. That slot holds the LAN adapter. It's easy to see why these units are among the quietest PCs you'll find.

The TS2's TeleVideo Ethernet adapter includes a NetWare boot ROM. The adapter is compatible with Novell's NE-1000, so installing the TS2 on a NetWare LAN is a snap.

The WY-212 opens much like the TS2, but it has nine screws on the bottom of the base. The main difference between the two systems is the two 16-bit expansion slots present in the WY-212. They're mounted above the motherboard, one to the left and one to the right. The LAN adapter is in the left slot, and the VGA board is in the right slot. The standard 8-bit Wyse VGA card uses chips from Tseng Labs. The CPU has a compatibility speed of 8 MHz, which you can set with SETUP. Jumpers let you run the 80287 at 6 or 10 MHz.

The motherboard is a tiny 10¼ inches wide by 9¼ inches deep. Ours had no visible trace cuts or jumpers. On it were a total of 78 chips, 32 of which were for memory. Four application-specific ICs (ASICs) from VLSI do most of the job of emulating an IBM AT. With so few chips and no mechanical components, the WY-212 should be reliable.

The TS2's motherboard is even smaller (8 inches wide by 7 inches deep, with a 1½- by 4½-inch notch in the back left corner) and has mostly surface-mounted chips. Like the WY-212 board, its design is mature—there was only one jumper wire. Of its 70 chips, 36 of them are for memory. One NCR ASIC and six VLSI ASICs provide the Hercules and AT emulation—an AT and video adapter in only 34 chips. The TS2's 80286 has a compatibility speed of 8 MHz that you can set with an external DIP switch.

Neither machine gives you many options; these units are basically smart terminals with no free expansion slots. You couldn't add a disk drive even if there were room in the cases, because the power supplies run at only around 50 watts. Other than the TS2's few memory choices, the only real option is MS-DOS 3.3. Currently, you also cannot run OS/2 on either machine; that will have to wait until vendors offer OS/2 remote-boot software.

Performance

We tested both diskless PCs on a thin-wire Ethernet LAN with a 16-MHz 80386-based Samsung file server running Novell's NetWare 2.15 SFT (for System Fault Tolerant). The server included a 150-megabyte hard disk drive, a Novell NE1000 Ethernet adapter, and 4 megabytes of RAM. The server's hard disk drive delivers excellent performance by combining a SCSI disk drive with an intelligent controller that has an on-board 8K-byte cache. NetWare further speeds disk accesses by prefetching sectors on most reads and by caching recently read sectors.

Because neither of these systems has a hard disk drive, their disk performance depends largely on the speed of the network and the file server. We chose, therefore, not to run any of the application benchmarks, which depend heavily on disk access and so could be misleading. We discarded the low-level disk I/O benchmarks for the same reason.

The network interface cards in each machine also affect overall performance. We tested both machines with 8-bit Ethernet adapters. Unlike the TS2, however, the WY-212 could use potentially faster, 16-bit LAN adapters.

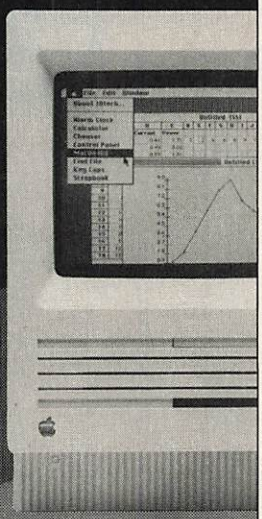
We ran all the tests on an unloaded network. They showed just how hard it is to benchmark disk-oriented tests on a LAN: Both systems received a disk index over 10 times that of a standard AT, courtesy of the unloaded network and the speedy file server. While the disk test

continued

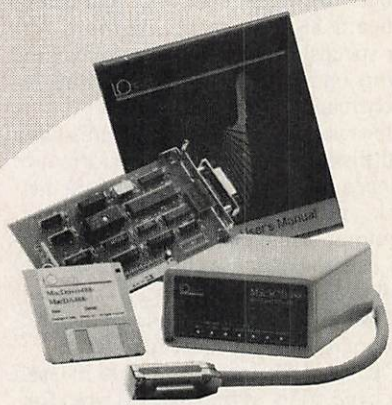
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Price remains a big question: These two systems cost as much as, or more than, many AT clones that include hard disk drives.

results are meaningless in absolute terms, it's clear from our tests that network-based systems aren't intrinsically slower than disk-based ones.

Surprisingly, despite its faster CPU clock speed, the WY-212 didn't score significantly higher than the TS2 on the CPU tests. The similarity in scores probably stems in part from the fact that both machines run with one wait state.

In the FPU tests, however, the WY-212 beat the TS2 by about 15 percent. The TS2 lost here because it runs its 10-MHz 80287 at only 6.7 MHz. (A TeleVideo spokesperson said that the TS2's coprocessor speed is limited to a maximum of 6.7 MHz, one-third the speed of the unit's 20-MHz oscillator.)

The TS2 won the video tests by about 20 percent. That difference is potentially misleading, however, because the results come from two different sets of tests—the WY-212's for VGA, and the TS2's for a Hercules-compatible display.

Compatibility

Both systems fared well in compatibility testing. With no expansion slots, we couldn't test much hardware. Two external serial devices, a USRobotics Courier 2400 modem and a Microsoft Serial Mouse, worked with both systems.

There were also no major software problems. Both flawlessly ran a wide range of applications, including Borland's Quattro 1.0, Reflex 1.14, Turbo C 2.0, and Turbo Pascal 4.0; Digitalk's Smalltalk/V 1.2; Kermit 2.32/A; MicroPro's WordStar 3.3 and 4.0; Lotus's Symphony 2; Microsoft's PC Paintbrush 2.0 and Word 4.0; Novell's NetWare 2.15; and Symantec's Q&A 1.1.

The TS2 did have a problem with Microsoft Windows 1.01. That software ran fine on the WY-212, but on the TS2 it got caught in an endless loop before it could completely come up on the screen. Every minute or so it would give the error that it "could not access the drive NETWORK." A spokesperson for TeleVideo said that a newer Windows version (2.03) works fine.

Bits and Pieces

The TS2 comes with a Fujitsu Limited FKB4700 AT Enhanced keyboard, which we've tested on other systems. It has an enlarged Return key and uses the standard AT DIN connector. The Fujitsu keyboard has a soft mechanical click and feel that we've come to like.

The WY-212 uses Wyse's own keyboard, which is fully compatible with IBM's AT Enhanced keyboard. Like Wyse's terminal keyboards, however, it has a tightly coiled telephone-type (RJ-11) cable connecting it to the base. The keyboard is a little stiff for our tastes.

Both machines include a one-year, mail-in, parts-and-labor warranty. The manufacturer pays for return shipping. Wyse offers on-site service through several firms, including TRW's Customer Service Division. Both companies also provide unlimited telephone support—but neither, unfortunately, has a toll-free support number.

To Disk or Not To Disk?

Both systems are well built and attractive and score high marks for their ease of installation and compatibility. With the right network adapter installed, you can just take them out of the box and hook them to a network, and you're ready to go. Depending on your LAN, you might need to build a boot disk on the server for your first diskless PC; after that, however, you can connect as many additional workstations as you like.

Price remains a big question: These two systems cost as much as, or more than, many AT clones that include hard disk drives. Furthermore, the absence of local hard disk drives hardly makes these two machines secure—it's easy to get at server data via their serial and parallel ports.

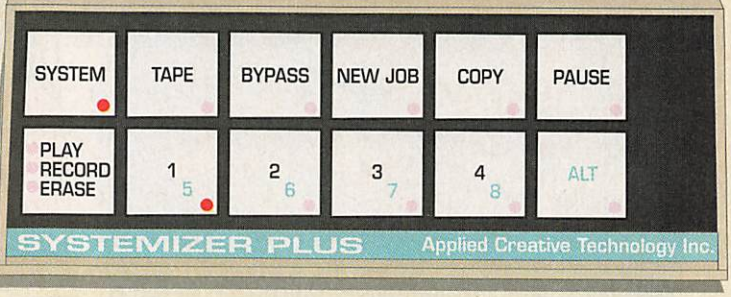
If you want a diskless PC, either system is a reasonable choice. The TeleVideo TS2 TeleStation is cheaper and has more memory capacity, while the Wyse WY-212 offers a VGA display and supports higher-performance, 16-bit network interface cards. ■

Bill Catchings and Mark L. Van Name, a BYTE consulting editor, are independent computer consultants and freelance writers based in Raleigh, North Carolina. You can reach them on BIX as "wbc3" and "mvanname," respectively.

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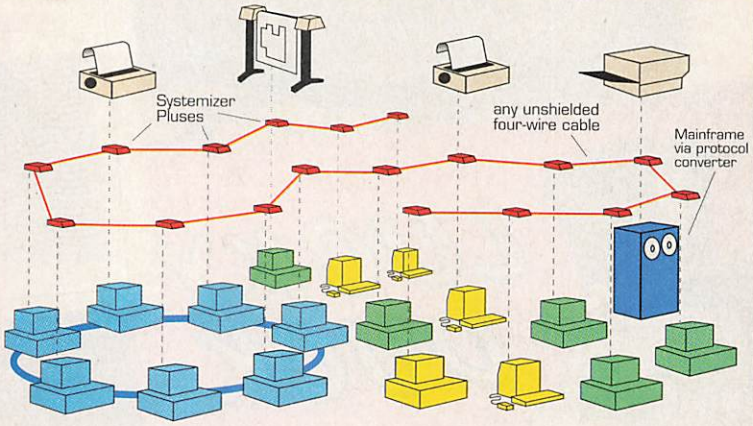
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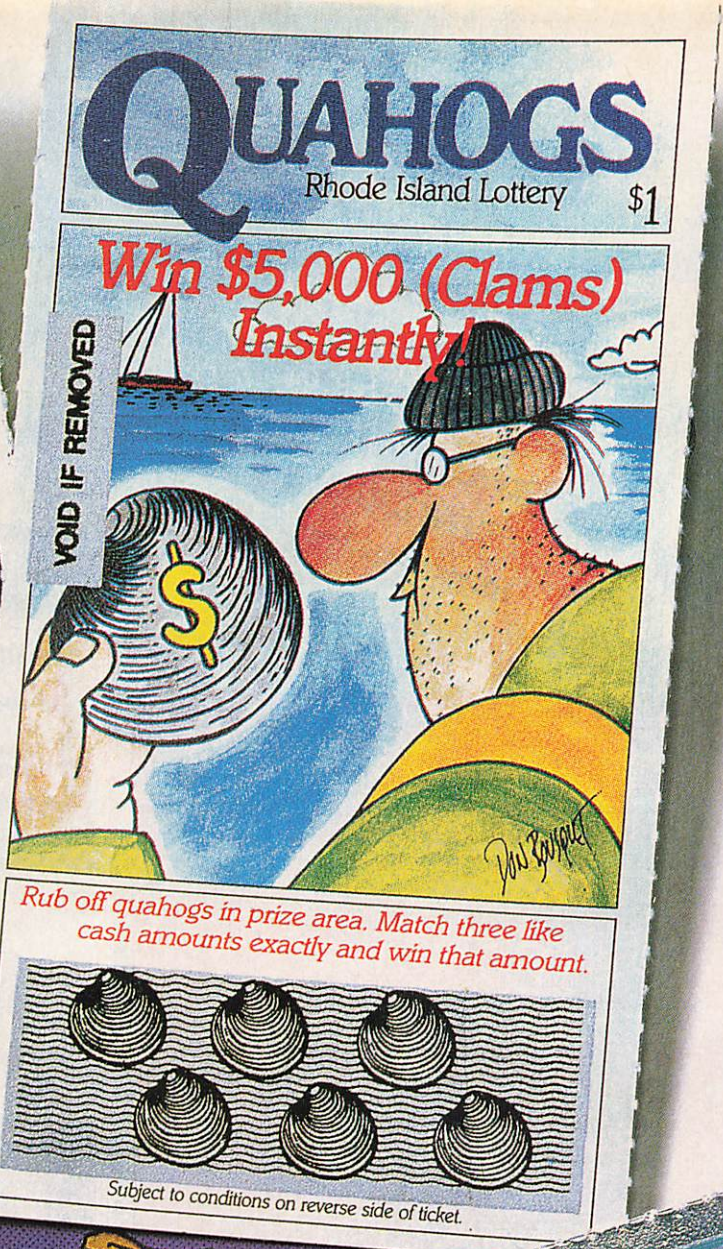


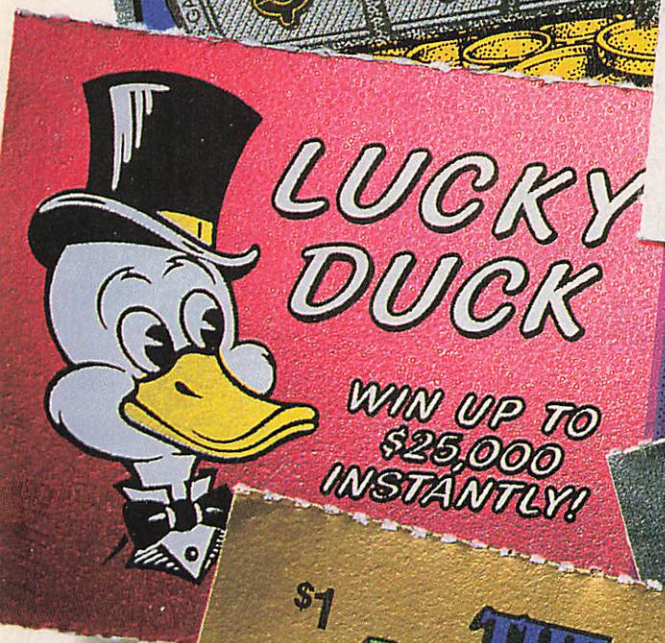
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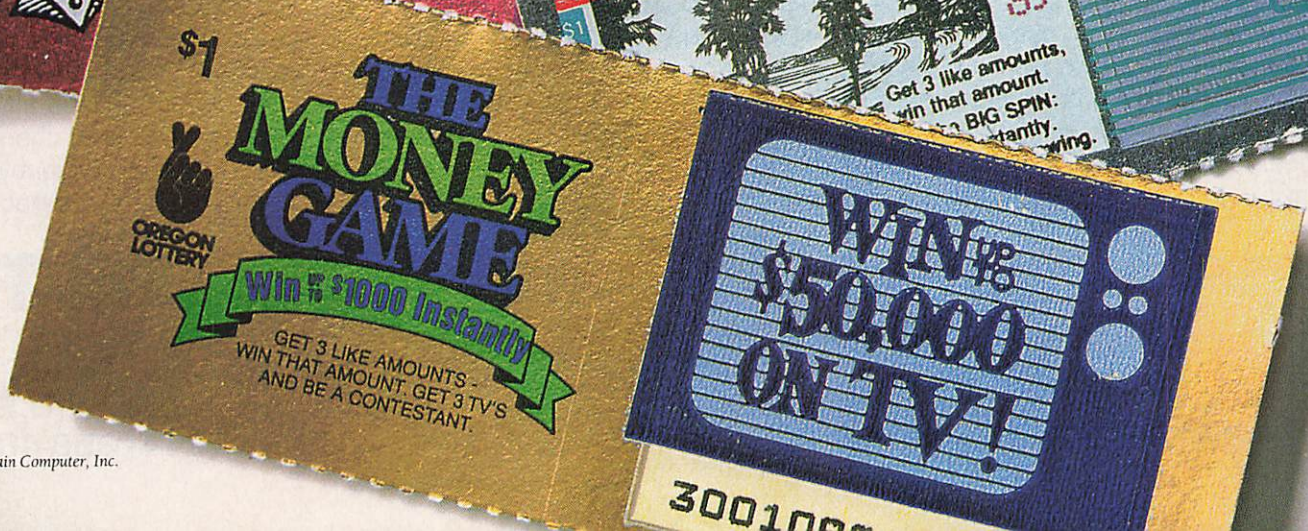
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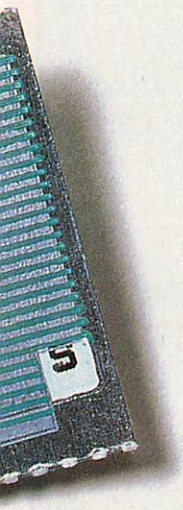
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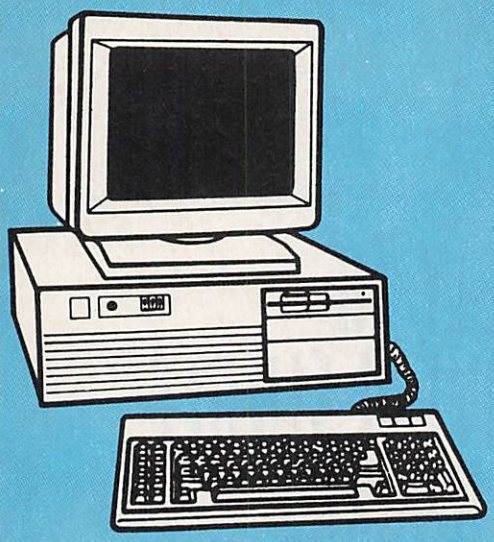
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20MB	1190	1640	1715
40MB	1345	1795	1865

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- 1P, 2S ports

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Paradise VGA-Plus-16	320
Paradise VGA-Prof	470
Quadram Quadega	250
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Video 7 Vega VGA	300
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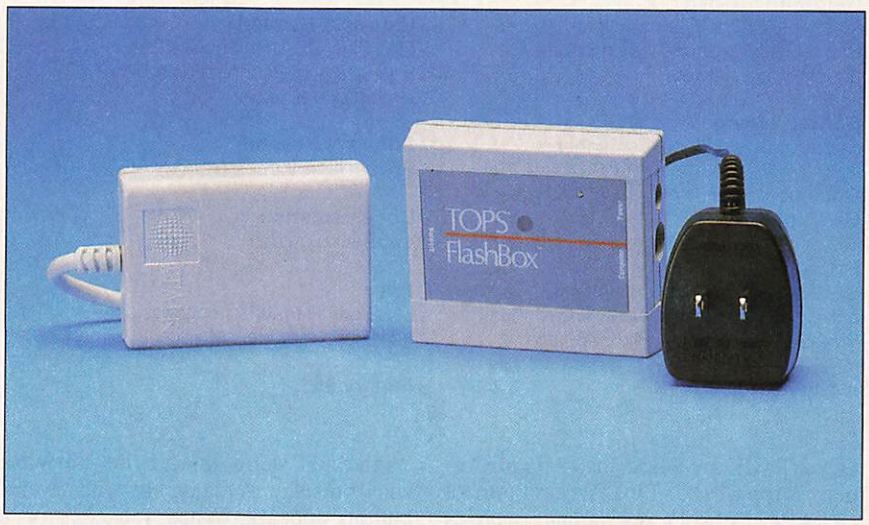
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LAN Aid: Mac Booster Modules

DaynaTALK and FlashBox connection modules provide fast pickup for sluggish LocalTalk networks

Tom Thompson



DaynaTALK (left) and FlashBox promise to triple network performance.

Can you improve the performance of your sprawling Macintosh network without scrapping the whole thing and starting from scratch? Dayna Communications and Sun Microsystems' TOPS Division say yes. Both offer products with modified network drivers and enhanced connection modules that will boost the data transfer rate of existing LocalTalk networks. Dayna claims that DaynaTALK can increase transfer rates to a maximum of 850 kilobits per second, while TOPS says that its FlashBox kit will provide a maximum transfer rate of 768 kbps.

By themselves, DaynaTALK and FlashBox don't give a Mac any extra networking capabilities, such as transferring files. Each Mac and file server must be equipped with either the Dayna or TOPS product to be able to operate at the higher transfer rate. But both products work with Apple's networking software, AppleShare 2.01, and install easily on Macs acting as AppleShare file servers. The faster DaynaTALK and FlashBox modules can coexist with devices running at the slower, standard LocalTalk transfer rate, such as Macs without enhanced connectors, laser printers, and certain network bridges.

Although similar in design and identical in price ($189), the products showed subtle differences in our tests. With its collision filters, DaynaTALK seems targeted for networks with a centralized server. FlashBox, with its TOPS/Macintosh networking software, is more suitable for distributed networks without servers.

Common Roots

These two products are similar solutions for the same problem. To Apple's credit, each Macintosh system includes basic AppleTalk networking protocols and drivers. LocalTalk, Apple's low-cost connector module and cabling option, lets you link Macs and laser printers together with transfer rates of 230.4 kbps. Add networking software (e.g., AppleShare), and you can establish a dedicated Mac as a file server.

Because LocalTalk lets Mac users into the networking game cheaply and easily, chaos often results. Soon, the network becomes a maze of cables strung from cubicle to cubicle, and perhaps through the ceiling. Some users begin launching applications stored on the file server. Others regularly transfer huge files back and forth. One department attaches a color PostScript printer to the network. Soon all that activity slows down the network, and 230 kbps doesn't seem like such a fast transfer rate after all. If you're delegated to beef up that rate, you'll face a big headache: new and costly upgrade hardware, and worse, the prospect of ripping out the existing network wiring to add new cables.

Enter the Dayna and TOPS enhanced connection modules. To install either one, you turn off the Mac and attach the existing network connection module to the enhanced module, which in turn attaches to the Mac. Next, you restart the Mac, run the installation software to install the new network driver, and make any adjustments (e.g., you can set the DaynaTALK driver for transfer rates from 600 kbps to 850 kbps). You then reboot.

Both of these kits contain test applications that "exercise" the network connection by sending and receiving test packets between two nodes. The standard

continued

DaynaTALK

Company
Dayna Communications, Inc.
50 South Main St., Fifth Floor
Salt Lake City, UT 84144
(801) 531-0600

Features
Boosts LocalTalk data transmission to a range of rates from 600 kbps to 850 kbps; SpeedGuard timing and filters for avoiding data collisions during high-speed transmissions

Hardware Needed
Mac Plus, SE, or II; LocalTalk or PhoneNet-type connection module attached to a network

Software Needed
System 6.0.2/Finder 6.1 or higher

Documentation
User's guide

Price
$189 per kit (each kit contains one enhanced module, software, and manual)
SpeedGuard Collision Filter: $69.95

Inquiry 854.

TOPS FlashBox

Company
Sun Microsystems
TOPS Division
950 Marina Village Pkwy.
Alameda, CA 94501
(800) 445-8677

Features
Enhanced LocalTalk data transfer rates of 768 kbps; LED indicator that shows when data is being transmitted; accommodates FlashBox-compatible Macs and PCs in the network

Hardware Needed
Mac Plus, SE, or II; LocalTalk or PhoneNet-type connection module attached to a network

Software Needed
System 4.1/Finder 5.5 or higher

Documentation
Installation guide

Price
$189 per kit (each kit contains one enhanced module, software, and manual)

Inquiry 855.

DaynaTALK or FlashBox software replaces AppleTalk's Link Access Protocol (ALAP). Network operations, such as calling a file from the server, don't change; they just proceed at the higher transfer rate.

Talking DaynaTALK

Roughly the size of a cigarette package, the DaynaTALK connection module has a mini-DIN-8 cable at one end that attaches to the Mac's printer port. A female mini-DIN-8 socket at the other end accepts the cable from a network connection module.

The software disk contains the ubiquitous read-me-first file, the DaynaTALK driver, and a network diagnostic application. Several Apple files also reside on the disk: the Network cdev (used to select the network driver via the Control Panel desk accessory), the Responder INIT (which responds to packets sent by the diagnostic network software), the Installer application, and Apple System software version 6.0.3.

Installation is a breeze because you simply boot the Mac with the disk and run the Installer. Once the Installer is launched, you just click on a mouse button to add or remove the DaynaTALK software.

To alter the Mac's network transfer rate, you just click on the DaynaTALK "sneaker" icon inside the Network cdev's display. A dialog box with several buttons appears. When you click on a Configure button, a new dialog box offers you a range of transfer rates: 850, 768, 740, and 600 kbps. The rate you select depends on the system you're using. The entire Mac II family, the Mac SE/30, and some Mac SEs can operate at 850 kbps. Mac SEs made prior to mid-1988 can manage only 740 kbps. The 600-kbps setting accommodates marginal networks where low-quality cabling or widespread nodes degrade the signals.

The user's manual thoroughly explains DaynaTALK, the test applications, troubleshooting, and how to avoid network collisions (see the text box "DaynaTALK Option: Collision Control" on page 223). The manual's step-by-step procedure might be overdone for experts, but it serves novices well.

FlashBox Speed

The TOPS FlashBox connector module is slightly larger than the DaynaTALK unit. FlashBox requires external power to operate its electronics, so, unlike with DaynaTALK, every FlashBox user needs to have an extra power outlet. But FlashBox offers something that DaynaTALK doesn't: an LED indicator that shows when it's transmitting. This is a welcome feature when you find yourself puzzling over whether the Mac is talking to the network or not.

A female DIN-8 port for the network connection sits at one end of the module; at the other end is a six-pin female socket that accepts an adapter cable for the Mac's printer port. Adapter cables have the male DIN-8 connector; cables with a male DB-9 connector for use with the Mac 512KE are planned. While this adds a measure of flexibility to the design, it can also cause trouble. If you're not careful, you might plug the network's connection-module cable into this six-pin socket, damaging the FlashBox.

The software disk contains several versions of the network driver, an installer application, a network diagnostic application, an INIT, and a file with various installation resources. It also includes Apple's Network cdev and an AppleTalk file that provides a new version of the AppleTalk driver for a Mac Plus.

The disk is not bootable, but the custom installer application manages nicely as is. I recommend that you make a boot floppy instead (there's room on the disk for a stripped-down system) to minimize the risks of modifying a live System file. A click on the appropriate mouse button installs or removes FlashBox software. The package doesn't offer configuration options for network speeds, and it only allows transfer rates of 768 kbps or 230 kbps. Also, no collision filters are available. However, the DaynaTALK's optional Collision Filter is compatible with the FlashBox.

The FlashBox manual, like DaynaTALK's, offers detailed installation instructions for novices and a quick start-up guide for experts, and it has a section on diagnostic testing and topology mistakes. The manual is terse in some areas, but it doesn't scrimp on troubleshooting hints—a plus for any network manager.

Acid Test

We measured relative data transfer rates of the modules in real-world tests with BYTE's LAN. We also copied files between two Macs in isolation (to eliminate network traffic) and over an "ideal conduit" (a network link consisting of a short length of phone wire between two PhoneNet connection modules).

To minimize the effects of machine performance on the transfers, we used a Mac IIcx equipped with an 80-megabyte internal hard disk drive and a Mac II with a 40-megabyte internal hard disk drive. Both disks were empty except for the system and benchmark files necessary to conduct the tests. We used 6.0.3 System

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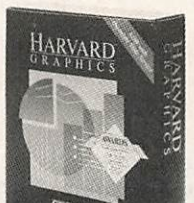
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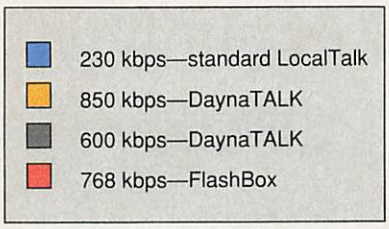
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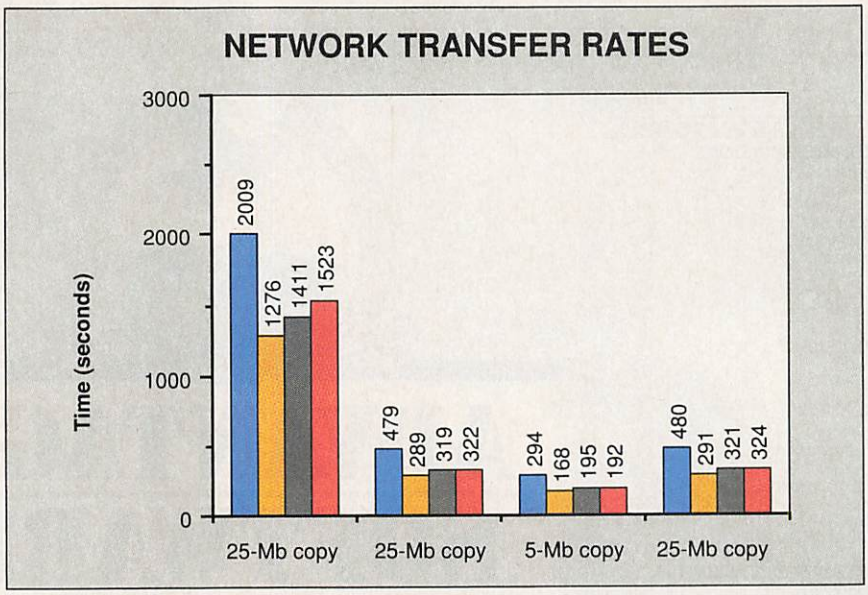


Figure 1: *Note that in the file transfer tests, subsequent file copies took less time to complete than the initial one. Subsequent copies benefited because the file structure was already built. FlashBox is, at worst, only 12 percent slower than DaynaTALK in these tests.*

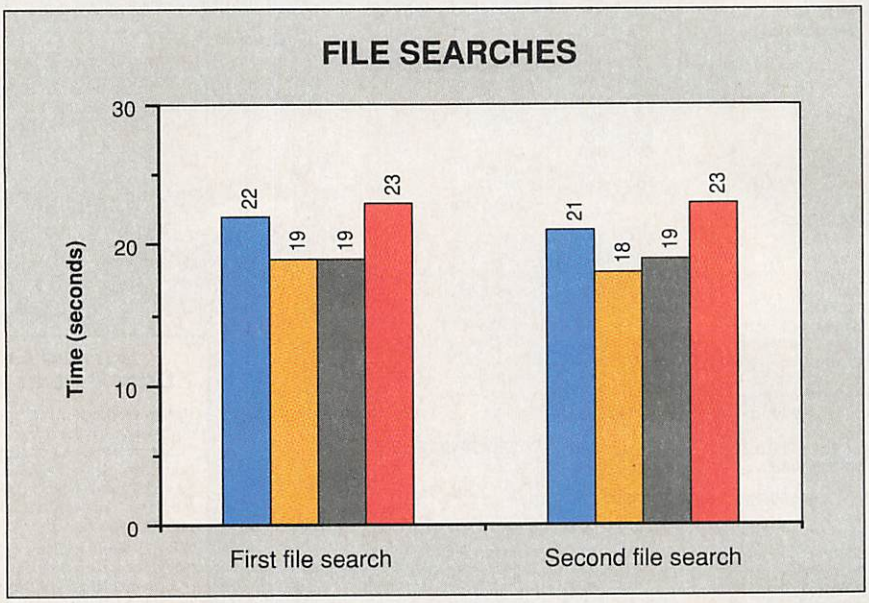


Figure 2: *In searches for a file among lots of files, FlashTalk was slower than even standard LocalTalk.*

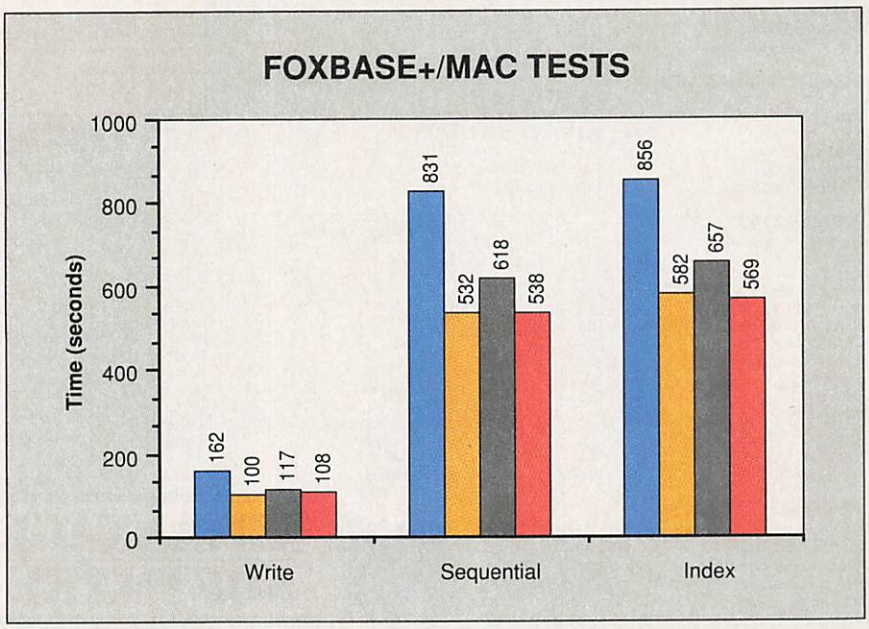


Figure 3: *In database tests, FlashTalk operating at 768 kilobits per second performed nearly as well as, or equal to, DaynaTALK operating at its maximum rate of 850 kbps.*

DaynaTALK Option: Collision Control

DaynaTALK's first line of collision defense in high-speed networks is SpeedGuard timing, a standard feature in DaynaTALK software.

Collisions occur in LocalTalk networks because only one node can transmit at a time. Slower nodes (operating at 230 kilobits per second) sometimes don't recognize high-speed transmissions in progress. A slower node may inadvertently broadcast on the network, "stomping" on a high-speed transmission and causing a *collision*. If slower nodes cause frequent collisions, network throughput degrades because high-speed nodes spend too much time resending information.

SpeedGuard timing simply places an irregular clock signal on the network (this signal is created by stopping the clock signal's transmission for 10-microsecond intervals). The irregular clock generates an error condition in the Mac's network communications hardware, the serial communications chip. Certain implementations of AppleTalk read this error as a sign that the network is busy. In this way, DaynaTALK's timing scheme tricks slower devices into thinking that the network is in use and thus prevents collisions.

However, Mac IIs, Mac SE/30s, the LaserWriter Plus, and LaserWriter IINT and IINTX printers use a new version of AppleTalk that doesn't treat this error as a busy condition. Dayna's response to this is the SpeedGuard Collision Filter. This $69.95 option acts like a standard LocalTalk connection module with additional electronics to detect the high-speed signals. It resembles the DaynaTALK connection module, but instead has a DB-9 cable connector (a DB-9-to-DIN-8 adapter cable is included) and uses a small external power supply that's similar to a calculator-battery charger. When the SpeedGuard Collision Filter detects a high-speed transmission, it generates signals that the Macs and the printers see as a network busy condition.

software running under the Finder with no special INITs installed.

Benchmarks consisted of abbreviated tests used to evaluate SCSI WORM (write once, read many times) drives (see "The Optical Option," October BYTE). The first set of tests (see figures 1 and 2) used an automated MPW script to copy many large files from one system to another and search for individual files. The second set of tests (see figure 3) used FoxBASE+/Mac 1.0 to perform database searches on a single file. DaynaTALK ran AppleShare 2.01 with the Mac IIcx acting as the file server, while FlashBox used TOPS/Macintosh 2.1 to publish the Mac IIcx's hard disk.

When you examine the results shown in the figures, remember that DaynaTALK was running under AppleShare, whereas FlashBox ran with TOPS/Macintosh. Although FlashBox can work with AppleShare, the intent here was to show how well FlashBox fared when using its own networking software. Notice also that even though data can move through LocalTalk several times faster, file transfers aren't greatly accelerated. They're stalled by the network overhead of links and protocols that ensure an error-free data transfer.

The DaynaTALK finished first on throughput, but even at its peak transfer rate of 850 kbps, the tests ran only 32 percent to 43 percent faster than standard LocalTalk speeds. TOPS FlashBox was, at worst, only 12 percent slower than DaynaTALK at its maximum on the file copy tests. On the FoxBASE database tests, TOPS performed about as well as DaynaTALK on the write and sequential operations, and was even a fraction faster than DaynaTALK on the index test.

While these increases don't seem like a big improvement, there is another factor to consider: network traffic. Since only one node can use LocalTalk at a time, many operations stall while waiting for network access on a high-traffic network. If every node can finish its job faster, more networking jobs get done in the same amount of time, which adds up to better use of the network. Since network traffic varies from network to network, it's something we couldn't measure and doesn't show up in the figures.

In real-world tests with BYTE's network, the enhanced modules helped us run applications off the file server faster. At DaynaTALK's maximum speed, we'd occasionally experience delays on file transfers, probably due to the quality of our network cabling (standard phone wire arranged in a Gordian Knot topology). The problem went away when we switched to FlashBox's speed. We also used DaynaTALK, its collision filters, and TOPS FlashBox on the same network without trouble.

Tough Choices

Both DaynaTALK and FlashBox provide higher network transfer rates. While DaynaTALK offers the faster rate, you can't take advantage of it unless your network is in good shape. DaynaTALK overcomes this with a choice of several lower transfer rates to deal with marginal networks. Dayna's efforts to minimize network collisions and offer compatibility with FlashBox are commendable.

TOPS FlashBox comes close to matching DaynaTALK's maximum transfer rate, and, on slightly marginal cabling, DaynaTALK's edge can disappear. The FlashBox software seems better crafted than DaynaTALK's.

Although DaynaTALK connection modules don't require a power supply, be aware that the design isn't compliant with Apple's use of the printer port, while the FlashBox connection modules are compatible. This will become a design issue for you if your network is strapped for power outlets.

Neither kit provides networking software to handle file transfers. DaynaTALK requires a file server and additional software to accomplish this. TOPS offers its TOPS/Macintosh software, which provides this capability without the need for a server. While TOPS/Macintosh isn't cheap, for small networks it's far less than the price of a PC server.

If I had my choice, I would combine Dayna's multispeed network driver and collision filters with the TOPS network diagnostic software and TOPS/Macintosh software to manage file transfers.

Both DaynaTALK and FlashBox are designed to boost an existing network's performance, but they won't solve all your networking problems. They both deliver higher network throughput, although the boost is relatively small for the price. Nevertheless, each is worth considering if data transmission on your LocalTalk network is becoming a waiting game. ■

Tom Thompson is a BYTE senior technical editor at large. He can be reached on BIX as "tom_thompson."

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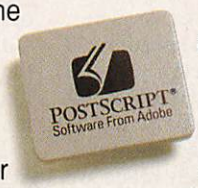
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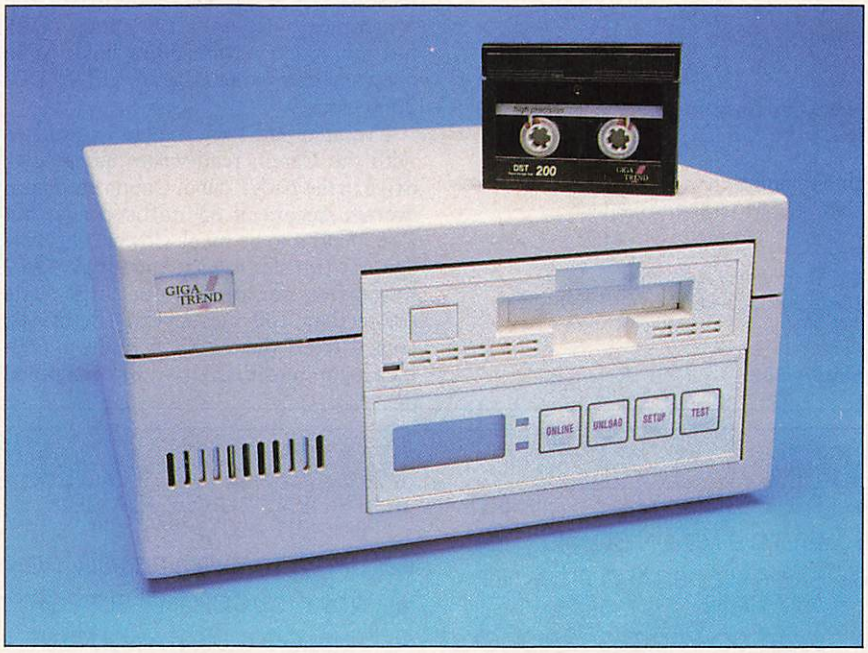
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DAT Drive Eases Mac Backups

The pioneering Gigapack-Mac lets moneyed Mac users effortlessly store gigabytes of data

Don Crabb



Storing 1.2 gigabytes costs $6000 with the Gigapack-Mac and a 120-minute cassette.

I've had nothing but problems with every DC-2000 tape I've ever made, and I'm tired of it. My headaches range from hard-read errors and unintentional overwrites, to tapes being just too small to back up an entire disk. If this sounds familiar, then the Gigapack-Mac DATA/DAT drive may be a welcome, if expensive, solution for your nasty back-up problems.

The Gigapack-Mac stores data as bit streams on digital audio tape (DAT), an interesting technology that so far has not set the world on fire (see the text box "Defining DAT: Formats and Standards Lack Consensus" on page 230). First developed for high-quality audio recordings, DAT's role in computer data storage is still evolving.

DAT drives approximate a read/write tape equivalent of CD-ROMs. One of DAT's biggest advantages is the tremendous amount of information (roughly 1.2 gigabytes) that can reside in a single 2- by 3-inch cassette.

The Gigapack-Mac, by GigaTrend, is one of the first commercial DAT drives to ship, although a host of others is expected to be released this fall. The Gigapack-Mac serves Macintosh II, Plus, and SE users. GigaTrend imports DAT drive mechanisms from its West German parent, GigaTape GmbH.

The Gigapack-Mac consists of the drive, custom electronics, and two SCSI ports. Four touch-sensitive front-panel switches help users load and unload tapes, test the unit, and set up the SCSI ID (the drive comes preset to SCSI 4). A four-digit LCD status panel and two LEDs monitor on-line status and errors. A separate LED indicates power-on and is placed next to the tape-loading slot. Tape loading and unloading are power-assisted, much like a front-loading VCR.

My review unit arrived with a DB-25–to–DB-50 SCSI cable, a SCSI terminator, a power cord, a software disk, and two BASF DAT 120 cassettes that were certified by GigaTrend for data service. Completing the expensive ($5950) package was a thin and completely inadequate manual. It does only the weakest job of explaining how to use the hardware and software. A $6000 hunk of hardware deserves better.

A Drive Test-Drive

I connected the drive to three different systems: an 8-megabyte color Mac II with an internal Apple HD40SC hard disk drive, a 1-megabyte Mac SE with an internal Apple HD20SC hard disk drive, and an 8-megabyte color Mac II with an internal Apple HD40SC hard disk drive and an external Jasmine DirectDrive 140 hard disk drive. In all three cases, the Gigapack-Mac was the only additional SCSI device connected. Besides everyday use, I tested the Gigapack-Mac using timed backup and restore tasks.

GigaTrend claims backup speeds of 10 megabytes per minute. At no time during any of my testing did my results come close to that (see table 1). Nevertheless, the Gigapack-Mac proved to be a reasonably fast tape drive, averaging a transfer rate of better than 1 megabyte per minute in most situations. Many DC-2000 and

continued

Gigapack-Mac

Company
GigaTrend, Inc.
2234 Rutherford Rd.
Carlsbad, CA 92008
(619) 931-9122

Features
1.2-gigabyte storage capacity per 4-mm DAT 120 cassette; DATA/DAT logical tape format with save, restore, and random access; SCSI, Pertec, and QIC-02 computer interfaces; 0.32-inch-per-second tape speed; search time of 20 seconds (average)

Size
9½ × 4½ × 9¾ inches; 12⅕ pounds

Hardware Needed
Macintosh Plus, SE, SE/30, II, IIx, or IIcx

Documentation
Hardware and software manuals

Price
$5950 (quantity discounts available)
10-pack of data-certified DAT cassettes: $260

Inquiry 853.

DC-600 tape backup units that I've used fall considerably below this rate.

For example, the Jasmine DirectTape DC-2000 tape drive holds 38.5 megabytes on a single DC-2000 tape. Its average transfer rate runs slightly under 1 megabyte per minute on both file-by-file and image backups. (The Gigapack-Mac doesn't provide for image backups.)

The Jasmine's burst transfer rate is about 1.5 megabytes per minute. My tests placed the DAT drive's burst transfer at about 4 megabytes per minute. Overall, the Gigapack-Mac performed at least as fast as the DC-2000 drive, and sometimes twice as fast or more. (DAT has the added advantage of holding, in one cassette, enough data to fill 31 DC-2000 tapes.)

I've also had some recent experience with the Canon read/write optical disk drive in the NeXT cube. Canon claims an average access of 85 milliseconds, but I've found it to be much slower. On average, my transfer rates ranged from 5 to 9 megabytes per minute for large-scale (more than 100 megabytes) file-by-file copies from the NeXT's built-in 660-megabyte hard disk drive to the optical disk drive, which makes it faster than the Gigapack-Mac.

Snappy Tape Shuttles

Overall, the Gigapack-Mac performed solidly. Even though the DAT cassette is small, it quickly shuttles tape back and forth during a backup or restore operation, making the unit suitable for quick restores of single files.

During my testing, the time to access and restore a single file in a data set was about 30 seconds; it never took longer than 55 seconds or less than 15 seconds. The exact times depended on the position of the file in the data set.

The supplied backup-and-restore software admirably handled file-by-file operations. A filtering scheme for selecting a specific file, an updated file, or all files meant that I could easily back up only what I needed.

File restoration performed equally well. I could restore the entire data set or parts of it at will. I could even set the dialogue to automatically overwrite my restored files, never overwrite them, or let the software prompt me each time. In all

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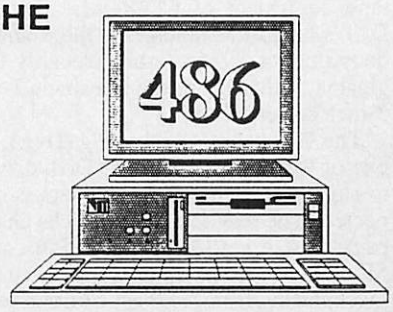
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Circle 288 on Reader Service Card

cases, file restoration was a snap.

Unfortunately, version 1.06 lacks a mirror-image capability (although it is present in the menus as a dimmed item), so I couldn't do volume image backups. This is an important omission. Any medium that stores 1.2 gigabytes as quickly as the Gigapack-Mac needs an image backup mode. (GigaTrend says it intends to offer this capability in the future.)

Another drawback was my review unit's SuperLock copy-protected software. This annoying copy-protection scheme has since been removed from all copies of the Gigapack-Mac software.

Torture Tests

GigaTrend claims that the cassettes provide stable, long-term storage of large files, such as graphics images or font files. To test short-term stability, I carried a full cassette (containing 1.2 gigabytes of Mac files) in my soft-sided briefcase for about three weeks. The cassette received significant magnetic and environmental abuse (e.g., from airport metal detectors) and never failed.

I also shipped this same cassette from my office to my home and back again via overnight mail. I used the standard next-day-letter cardboard envelope, and I didn't pad the cassette in any special way. The cassette still worked fine after making the round trip from Chicago to the carrier's Memphis headquarters and back.

Finally, I placed the same full cassette

continued

Table 1: *In backup and restore tests using internal and external hard disk drives, the Gigapack-Mac provided average data transfer rates of better than 1 megabyte per minute. Times are in minutes:seconds.*

BACKUP AND RESTORE TESTS

Macintosh II[1]	
Backups to Apple HD40SC:	
41,399,296 bytes, 1002 files in 162 folders	27:30.44
10,410,003 bytes, 1002 files in 162 folders	07:11.13
41,210,050 bytes, 2004 files in 324 folders	31:11.09
Restore of Gigapack-Mac files to a clean Apple HD40SC:	
41,210,050 bytes, 2004 files in 324 folders	38:40.01
Macintosh SE[2]	
Backups to Apple HD20SC:	
20,105,123 bytes, 1002 files in 162 folders	19:48.20
5,372,090 bytes, 1002 files in 162 folders	07:29.19
20,101,495 bytes, 2004 files in 324 folders	22:11.50
Restore of Gigapack-Mac files to a clean Apple HD20SC:	
20,101,495 bytes, 2004 files in 324 folders	25:19.30
Macintosh II with external hard disk drive[3]	
Backups to Jasmine DirectDrive 140:	
137,405,729 bytes, 1002 files in 162 folders	87:35.10
65,210,045 bytes, 1002 files in 162 folders	45:20.51
138,004,167 bytes, 2004 files in 364 folders	92:22.38
Restore of Gigapack-Mac files to a clean Jasmine DirectDrive 140:	
138,004,167 bytes, 2004 files in 324 folders	97:06.20

[1] 8-megabyte Mac II with Apple RGB 256-color video in 2-bit black-and-white mode, two internal floppy disk drives, and one internal Apple HD40SC hard disk drive; system software was installed on the HD40SC drive. No other SCSI drives were connected except the Gigapack-Mac. The backed-up drive was the start-up disk.

[2] 1-megabyte Mac SE with one internal floppy disk drive and one internal Apple HD20SC hard disk drive; system software was installed on the HD20SC drive. No other SCSI drives were connected except the Gigapack-Mac. The backed-up drive was the start-up disk.

[3] 8-megabyte Mac II with Apple RGB 256-color video in 2-bit black-and-white mode, two internal floppy disk drives, one internal Apple HD40SC hard disk drive, and one external Jasmine DirectDrive 140 hard disk drive; system software was installed on the HD40SC drive. No other SCSI drives were connected except the DirectDrive and the Gigapack-Mac. The backed-up drive (DirectDrive) was not the start-up disk.

Note: Tests ran with System 6.0.2, Finder 6.1, and the other system software from the 6.0.2 System Tools package. Only the desk accessories, fonts, INITs, and cdevs supplied with the Apple system were kept. MultiFinder didn't run. LocalTalk/AppleTalk was disconnected. During all testing, the CPU's data cache was disabled. I installed Gigapack-Mac's version 1.06 software on the start-up disks for file backup and restore testing. Each timing reflects the mean of 10 repetitions of each benchmark.

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Defining DAT: Formats and Standards Lack Consensus

Digital audio tape (DAT) technology uses helical-scan recording to store information as a digital bit stream. That bit stream can be digitally sampled music with a signal-to-noise ratio rivaling that of compact disks, or it can be plain old computer data bits.

GigaTrend's Gigapack-Mac uses a logical tape format known as DATA/DAT. Also championing this format are 11 other companies, including Apple, Fujitsu-Ten, Hitachi, JVC, Kenwood, Panasonic, Sanyo, TEAC, and Toshiba. DATA/DAT distinguishes itself by its ability to do both random reads and writes to a tape. In other words, DATA/DAT can update the tape in place.

This format competes directly with digital data storage, which permits random tape reads, but not writes, so it cannot update a tape in place. DDS is sponsored by a committee of 10 companies, including industry giants Hewlett-Packard and Sony. So far, IBM has not come down on either side of the DAT format debate.

DATA/DAT has not yet made it through the ANSI standardization process. The only part of DATA/DAT that its supporters have agreed on is the process for updating a tape in place. DDS, on the other hand, is a more mature technology that offers slightly higher storage capacities.

Partly because formats and standards are still evolving, immediate DAT sales may be modest. According to Hinda Chalew, an industry analyst with the market researcher Dataquest, 3800 DAT drives should ship this year, generating $5.6 million in revenues. Of these, only about 1000 drives will be full-price commercial units. But by 1993, shipments are expected to jump to 123,500 units, with revenues exceeding $74.1 million, according to Dataquest.

1 foot from a commercial bulk-tape eraser and then switched the unit on and off several times. Proximity to the strong magnetic field caused no apparent damage to the files, as repeated restore operations proved. This indicates high short-term reliability; however, long-term, archival storage remains to be tested.

Bottom Line

Compared to other mass-storage technologies, the Gigapack-Mac reigns as the big-ticket item. For example, DC-2000 tapes cost about $30 apiece (formatted) and hold 38.5 megabytes. A typical DC-2000 tape drive costs $1095. Storing 1.2 gigabytes of data requires more than 31 DC-2000 tapes, at a cost of almost $1000 (not to mention hours of time spent loading tape after tape). But the total storage cost for 1.2 gigabytes comes to only about $2095.

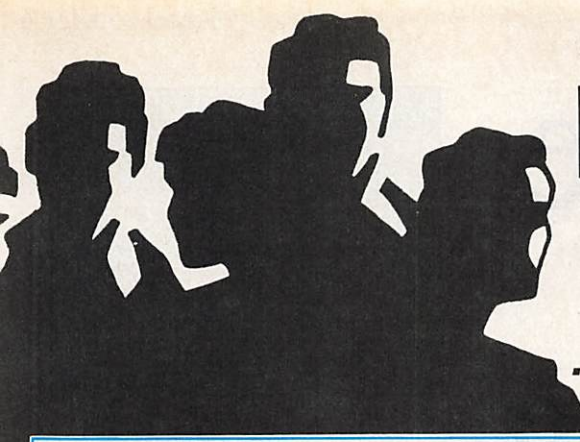
Optical disk drives, like the Canon unit, hold 256 megabytes per side and cost about $100 each for double-sided 512-megabyte disks ($50 for single-sided 256-megabyte disks). The drive sells for nearly $5000. Storing 1.2 gigabytes, then, commands a total media and machine outlay of about $5300.

The Gigapack-Mac sells for $5950, and 120-minute cassettes cost $26 each in their data-certified format. That puts the total cost of storing 1.2 gigabytes at about $5976—the highest cost of these three options.

Is there a Gigapack-Mac in your future? That depends on your needs. For individual Mac users, the answer is probably no. You'd be better off with a cheaper backup technology, like DC-2000 tape or shadow directories recorded to another hard disk drive.

But if you have many small Mac hard disk drives, you might consider the Gigapack-Mac as a shared device used to back up all of them. And where large Macintosh disk drives and file servers hold many megabytes, the Gigapack-Mac also makes sense because it's easy to set up and use, and because the media is easy to store. Now, if only the price could come down a bit! ■

Don Crabb is the director of laboratories and a senior lecturer for the computer science department at the University of Chicago. He is also a contributing editor for BYTE. He can be reached on BIX as "decrabb."



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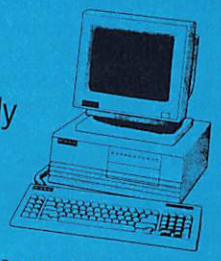
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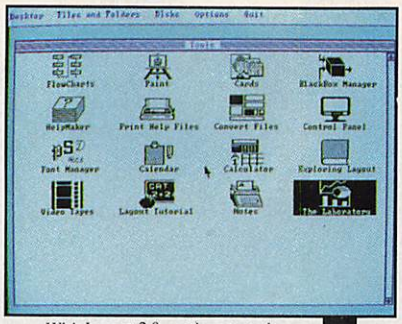
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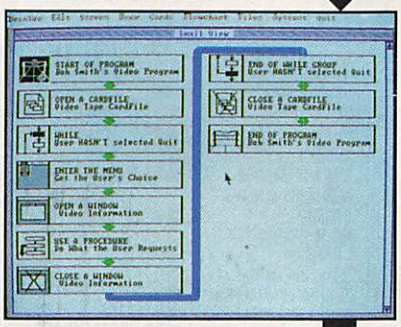
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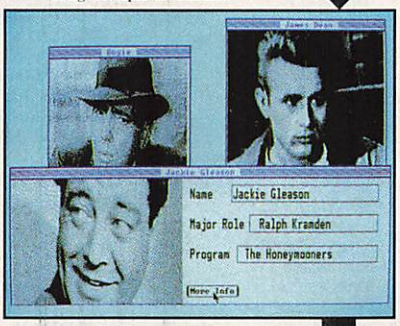
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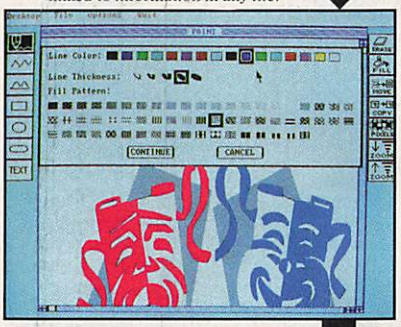
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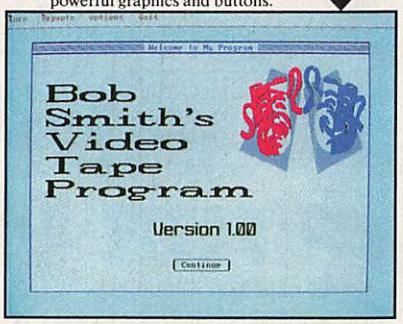
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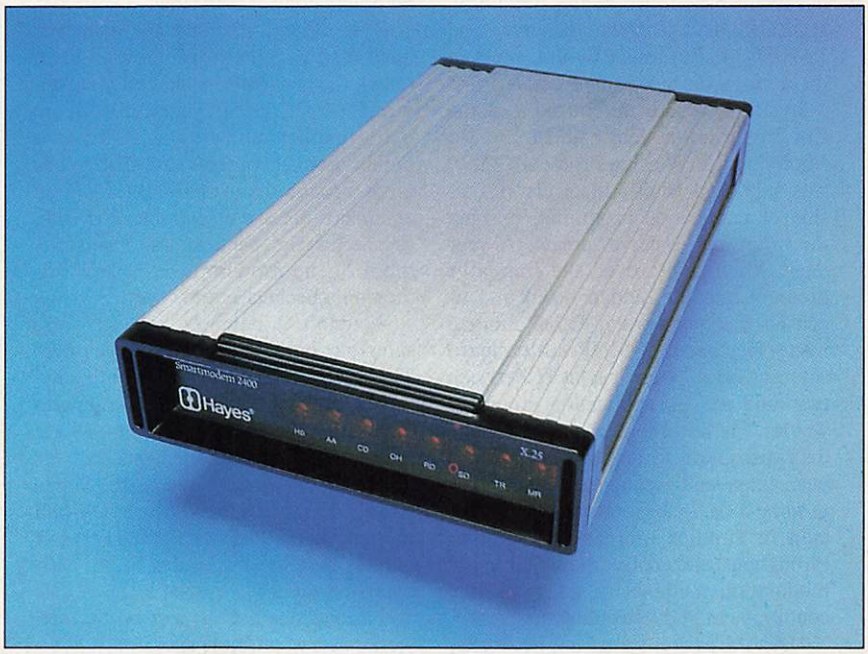
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Circle 215 on Reader Service Card

X.25 Pads Performance

Although tricky to install, Hayes's V-series modems with X.25 PADs boost data accuracy and throughput speed

Stephen Satchell



The Hayes V-series Smartmodem offers X.25 PADs at a relatively affordable price.

If you need to communicate with the outside world through Tymnet or Telenet and you value your time and money, Hayes Microcomputer Products' X.25 modems and modem enhancers offer you messages of hope. The company is now shipping X.25 PAD (which stands for packet assembler/disassembler) firmware with its V-series Smartmodem 2400, V-series Smartmodem 9600, and V-series Modem Enhancers. (X.25 is the CCITT-recommended standard for synchronous packet-switching networks.)

With X.25 firmware, the Hayes modems provide access to as many as four "virtual" connections. This means that, for example, you could simultaneously read three BBSes and an electronic conferencing system, if all these systems are connected to the same X.25 network.

The X.25 firmware also promises error control from source PADs to target PADs or host systems. Packets are built once in the source, and the information stays inside the packet until it reaches its ultimate destination. Data that is transmitted through asynchronous methods, like MNP and V.42 (see the text box "Origin of the Protocol: X.25's Evolution" on page 234), can sometimes be lost as packets flow between the two environments.

Because X.25 links the network and the source PAD using synchronous connections and high-level data-link control (HDLC), data pops through about 10 percent faster than if you used a standard asynchronous connection. Even without multiple-session support, your on-line time should drop significantly.

To see just what the Hayes X.25 PAD can do, I tested the V-series Smartmodem 2400 with a variety of public data networks. [Editor's note: *This review will concentrate on the X.25 PAD enhancement. For a complete review of the V-series Smartmodem 2400, see "4800 Bits, No Errors," June BYTE.*]

Manual Omissions

The weakest part of the Hayes product is the X.25 manual. It is disorganized, and it's missing a section covering Macintosh and other computer systems without flow control. The manual also lacks a translation dictionary to help set up the CALL command and understand X.25 jargon. If digging out details about how to dial into the services that you use is not your forte, save yourself the headache and hire someone to do the dirty work. Once you have the information, perhaps safely stored in calling scripts, you are in business.

Properly setting up the X.25 modem presents other installation battles. The V-series Smartmodem 2400 comes preset for flow control using the request-to-send and clear-to-send leads on an RS-232C port. Macintosh users must change flow control to use XON/XOFF before trying to issue PAD commands or make an X.25 connection; otherwise, the

continued

Origin of the Protocol: X.25's Evolution

In the beginning, modems simply converted digital data into telephone-line signals at one end and reconverted those signals back to digital data at the other end. Any error control took place outside the modem. Then desires for error control gave birth to a number of mutually incompatible software- and hardware-based protocols, including HDLC/SDLC, BiSync, Kermit, and XMODEM. But under duress, most of these protocols proved ineffective.

In 1983, Microcom introduced the Era 2 internal modem with MNP (for Microcom Networking Protocol). MNP was supposed to eliminate errors outside of application programs, making the programs easier to create. A year later, Microcom moved the link-layer protocol into the modem itself and licensed the technology. Other modem makers latched onto MNP as a standard solution for data error control between two modems, so application programs wouldn't have to be designed to handle data disruption. Since then, MNP has been extended to reduce the overhead of sending data, incorporate data compression to further increase end-to-end throughput, and control the switching of modulation methods to adapt to line conditions in 9600-bps modems.

Users of packet-switching networks, such as Tymnet and Telenet, know that garbled bits are only one of a variety of transmission problems. Many asynchronous network interfaces assume that you are using dumb (non-error-control) modems or that you're directly connected to terminals. Because of these assumptions, the interfaces offer no way to control data flow.

Even if you upgrade the interface hardware to recognize flow control (using the request-to-send and clear-to-send RS-232C leads), you'll still endure many packet conversions. The host builds network packets and then sends them through the network to the packet assembler/disassembler. The PAD disassembles the packets and transmits them to the modem, which rebuilds them into packets again.

Wouldn't it be more sensible—and safer—to build the packets just once? This is the X.25 philosophy. In this approach, the PAD at the host computer builds the packets (no modems in the middle) and sends the packets the way the network wants to see them. When you need to access the network, you call in, making the PAD part of the network only as long as you need it to be. This approach saves the cost of a leased line and allows one access port on the network to serve multiple sites.

modem will appear dead. The frustrating part of this is that the modem works just fine when you use it with a normal connection.

Before making a virtual connection using the PAD-to-user interface, you must know exactly what the network and the target PAD want to see. This can vary.

For example, when using Tymnet's Tymdial X.25, I accessed CompuServe and MCI Mail according to Tymnet's instructions, but my call to BIX required me to set up the CALL command in a specific manner. (Try this: CALL -D BIX. If you are using Smartcom III 1.1, you'll need to define the string "BIX" in the field "User Data.")

In addition to Tymnet, Telenet offers X.25 in-dial access through X.25 Dial. (As this article went to press, CompuServe reported that it was developing, but had not yet introduced, similar X.25 services.) X.25 in-dial is not limited to public networks; if your company has a private X.25 computer network, the same hardware setup will work with that system as well.

Each network and each host on the network has its own special requirements. Finding out what those requirements are may not be easy, because X.25 modems are new, and many network representatives are unfamiliar with X.25 specifications. Be prepared to face some puzzled voices on the other end of the support call. Or you may end up listening to someone talking "X.25-ese," so have your glossary handy.

Fortunately, the advantages of the Smartmodem with X.25 are worth the installation fuss. For example, when accessing BIX, I was able to download files using XMODEM-1K and Smartcom III with far less trouble and more speed than with a standard Tymnet access number. Reading messages interactively, I noticed far smoother performance using the X.25 connection. I'm just sorry I have to make a long-distance call to get that kind of access right now. (Tymnet is planning to link additional cities to X.25 in-dial. You should check the status for your location.)

Padded Packets

Speed and efficiency are only two benefits of having a Hayes modem with its own X.25 PAD. Many public-access PADs have limited RAM, so the packets transferred between the host and your computer can be quite small. With your own PAD, however, you can ask for blocks as large as 512 bytes. If you're charged by the packet, the ability to handle large packets can save you a bundle of money.

The X.25 in-dial services allow you to make one call into the network and as many "virtual calls" as you want without redialing. The number of concurrent virtual connections is limited only by the capabilities of your PAD. And if you add Smartcom III 1.1 or use software that supports Hayes AutoStream, you can simultaneously transfer data on all four virtual connections. Even with these multiple connections, your communications software will continue to perform as if you were using a standard dial-in line.

To set up multiple virtual connections, I established two links to CompuServe, one to BIX, and one to MCI using Smartcom III 1.1 on an 80386SX-based computer. I was able to transfer files in the "background" while working interactively, but Smartcom III was clumsy to use. I would have been far happier with a communications program running on a Macintosh (with a 19-inch screen, of course) with each session in its own window.

Affordable PAD

Hayes has managed to bring X.25 PADs to market at a relatively affordable price. The V-series Smartmodem 2400 with X.25 support lists for $899, while the V-series Smartmodem 9600 with X.25 is $1299.

If your modem isn't a V-series, you can achieve compatibility with a Hayes Modem Enhancer for $349; this is handy if you are using V.32-based (9600-bps full-duplex) X.25 access ports. Hayes offers the option of choosing V.42 for error control at the same prices. (X.25 and V.42 are standard features, not options.)

So who needs X.25 in-dial? Not every-

V-series Smartmodem 2400 X.25

Company
Hayes Microcomputer Products, Inc.
P.O. Box 105203
Atlanta, GA 30348
(404) 441-1617

Features
Error control during transmission of data packets; synchronous connections and HDLC links for fast data throughput; large, 512-byte packets; simultaneously handles four virtual connections to a data network

Size
5½ × 9½ × 1¾ inches; 2 pounds

Documentation
V-series Smartmodem 2400 manual; X.25 manual supplement

Price
V-series Smartmodem 2400 X.25: $899
V-series Smartmodem 9600 X.25: $1299
V-series Modem Enhancer X.25: $349
Unit as reviewed: $1148
Smartcom III 1.1: $249; upgrades from older versions of Smartcom II and III range from free to $75

Inquiry 852.

one, that's for sure. Since it's new, X.25 in-dial won't be fully incorporated by service providers like Delphi, Dialog, CompuServe Information Service, and BIX for some time.

In addition, many potential users may flinch at today's public-network access prices. Tymnet imposes a prime-time surcharge of $2 per hour ($1 per hour non-prime-time) for X.25 access. Telenet doesn't add surcharges, but its per-hour access charges range from $6 to $9 per hour, depending on your location. Both Tymnet and Telenet bill each virtual connection at the same rate as an individual connection using the same line speed.

On the other hand, for businesses and others who are willing to pay for higher accuracy and shorter transmission times, the Hayes X.25 products deserve a close look. ■

Stephen Satchell has evaluated computer products for 17 years. His company, Satchell Evaluations in Incline Village, Nevada, tests microcomputer hardware and software. He can be reached on BIX as "ssatchell."

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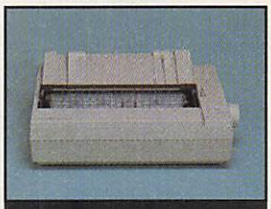
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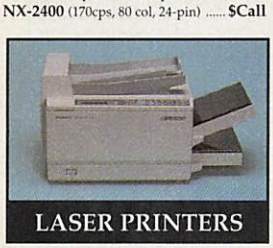
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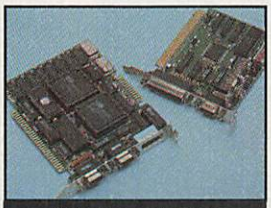
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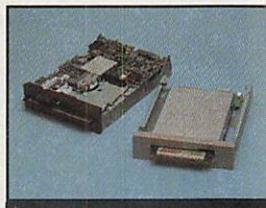
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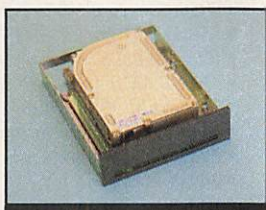
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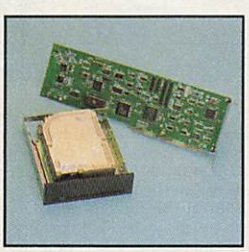
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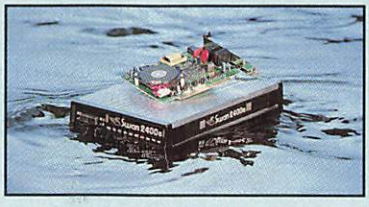
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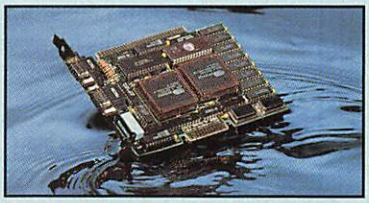


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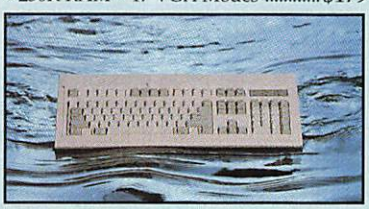
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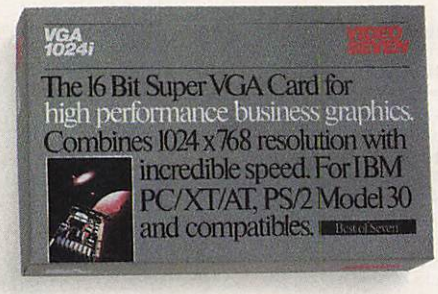
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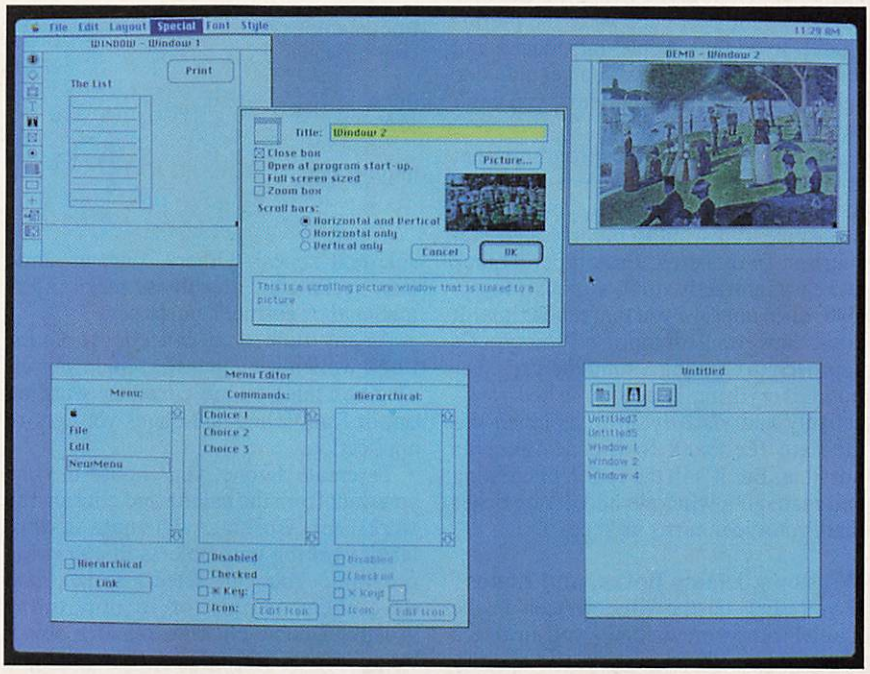
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Ease into Mac Programming

Prototyper 2.1 gives Mac programmers a jump start

Ray Valdés



SmethersBarnes' Prototyper lets you interactively build menus and link menu choices to window displays.

Prototyper is an interactive tool for creating prototypes of Macintosh programs. It's aimed at two audiences: It helps nonprogrammers design prototype applications in an interactive, nontechnical manner to help visualize product ideas, and it enables programmers who are not familiar with the Macintosh Toolbox to create skeleton applications that can be fleshed out over time. Prototyper's code generator produces the drudge code needed to support a complex Mac interface with nested menus and intricate dialog boxes.

The program's centerpiece is a Prototype window. In this window, you manage the interface objects that constitute an application. The window contains three icons that represent the major categories of interface objects available, and a scrolling portion that lists those that you have created for your prototype. The interface objects are menus, windows (including dialog and alert boxes), and a demo window that's the basis of Prototyper's simulation capability.

Clicking on the icons invokes the appropriate editor for that class of interface object. For example, clicking on the menu icon invokes a menu editor, while clicking on the window icon lets you create and modify windows, dialog boxes, and alert boxes. Each interface object owns a window on the desktop; you can leave the windows open and switch back and forth between them. This is a very Mac-like approach to prototype creation. You work interactively and iteratively—creating and editing the application's menu bar, and switching over to tinkering with the details of a dialog box. You then return to the menu for further adjustments.

You can run your prototype at any time with Command-R. The simulated application's menu bar appears at the top of the screen, replacing that of Prototyper. You can select menu choices, open application windows that have been linked to those choices, click on buttons, and view dialog boxes. The application's Quit item brings you back to Prototyper.

Prototyper includes a short tutorial in one of the folders on the distribution disk, but it's almost unnecessary—this product is extremely accessible. A friend of mine—a software developer who'd spent months writing the core of an application—used Prototyper to design and build his application's interface in just a few days, without ever consulting the manual or the tutorial.

The Menu Editor

Your application's menu bar is the logical place to begin the prototyping process. Prototyper's menu editor is a window that contains three scrolling lists. The first scrolling list holds menu headings for your application—Apple, File, Edit, and so on. The next contains items for each heading (e.g., Edit might contain these items: Cut, Copy, Paste, Clear, and Undo). The last helps you build hierarchical menus.

It is very easy to define the menus for

continued

your application. You just type a list of the menu headings into the first scrolling list. By clicking on any one of these headings, you can type the respective menu items in the second list box. This process takes longer to describe than it does to do. While you are working on a particular menu heading, the heading is temporarily added to Prototyper's main menu bar. This lets you pull down a list of items from the menu bar and check on spacing, spelling, and visual appearance as you enter the items. To check the entire menu bar, you would choose Run or Quick Look from Prototyper's menu. For a particular menu item, you can also define a sublist of choices in the hierarchical style that Apple introduced not long ago. In Prototyper, you get only one subordinate list of menu items; you can't nest to arbitrary depth.

In the realm of Mac programming, writing menu-handling code is one of the more straightforward tasks. You can also use Apple's ResEdit to modify menu resources. In this area, Prototyper's quick and easy interactive tool, although enjoyable, does not save you that much time. It does, however, exemplify Prototyper's approach to creating a simulated application: Everything is accomplished interactively and visually, with as much immediate feedback to the designer as possible. But it's in the realm of creating and managing windows and dialog boxes that Prototyper earns its keep.

Windows, Dialog Boxes, and Zones

If you click on the window icon in the main Prototyper window, you invoke a dialog box with which you can specify the kind of window object you want to create. You can create six types of windows, two types of dialog boxes, and three types of alert boxes. These window types are all standard Macintosh window types. As such, they can differ in the style of their borders, in the use of close boxes and title bars, and in whether or not a dialog box is modal.

Once you specify the kind of window you want to create, Prototyper presents what it calls a worksheet—a window similar to that found in many drawing programs. The window features a palette of interface objects called *zones*. These zones are icons, scroll bars, editable text areas, noneditable text (static text), pictures (graphics imported from other Macintosh drawing programs), round-cornered buttons, radio buttons, check boxes, scrolling lists, pop-up menus, rectangles, and lines. Some of these are objects with which you can interact (e.g., pop-up menus, radio buttons, and editable text zones). Others, such as static text, rectangles, and lines, serve informational or cosmetic purposes.

At any time, you can choose Quick Look, which simulates the window or dialog box that you are currently working on, or Run, which simulates your entire application.

To create a zone, you choose the one you want from the palette and click on the worksheet. Working with zones is similar to working with objects in a drawing program. You can select, resize, and drag them—singly or in temporary groups. Double-clicking on any object brings up a dialog box that lets you change that object's characteristics. This dialog box includes a brief, helpful description of the object, obviating the need for a context-sensitive Help function. Objects can snap to a grid.

Prototyper also provides some basic alignment commands (e.g., Align Top, Bottom, Center, Left, and Right). These are useful, but I wish there were more of them—for example, an `Align Middle` function or a `Distribute` function, as found in MacDraw II or MacDraft.

You can specify a text zone's font and size. Presently, you cannot specify the text style (i.e., bold, italic, or underline). The choices are tantalizingly present on one of Prototyper's menus, but for some reason, they are not supported in this version. As with most Mac programs, there is an `undo` function. Although it's workable and helpful in its present form, this function could be expanded further. In the course of creating a prototype, I encountered situations that I thought should be undoable but were not. However, none of these was of major import.

One nice feature is the ability to export a window definition into a separate Prototyper file. You can then incorporate this file into some other prototype application. You can also import resources, such as menu definitions or dialog box specifications, from any Mac application that has these in its resource fork.

Prototyper 2.1

Company
SmethersBarnes
520 Southwest Harrison St., Suite 435
Portland, OR 97201
(503) 274-2800

Hardware Needed
Mac Plus, SE, or II with 1 megabyte of RAM; a hard disk drive is recommended

Software Needed
Apple's System 6.02 or higher; Think C 3.0, MPW C 2.0, MPW C 3.0, Think Pascal 2.0, Turbo Pascal 1.10, MPW Pascal 3.0, or TML Pascal II

Documentation
User's manual

Price
$295

Inquiry 881.

Simulating an Application

Real applications, of course, have dynamic behavior. It isn't enough to view a dialog box; you need to be able to choose items or enter the parameters that the dialog box requests. Prototyper provides a simple mechanism for simulating this dynamic behavior.

For any interface object in your application (i.e., a menu item or zone), you can specify an action that will occur when you click on the object. Prototyper calls this feature *linking*. For example, you can link a button to the action of closing one of the windows in the simulation, or you can link a menu item to a sequence of different actions, such as closing one window, opening another, and disabling (graying out) other menu items. It is this linking feature that makes Prototyper a tool for simulating applications, as opposed to merely being a friendlier version of ResEdit.

Links in Prototyper are vaguely similar to links in HyperCard. HyperCard goes much further in allowing you to associate a HyperTalk script with an object and thus describe a much wider range of behaviors for that object. But this then becomes more like programming, which Prototyper seeks to avoid.

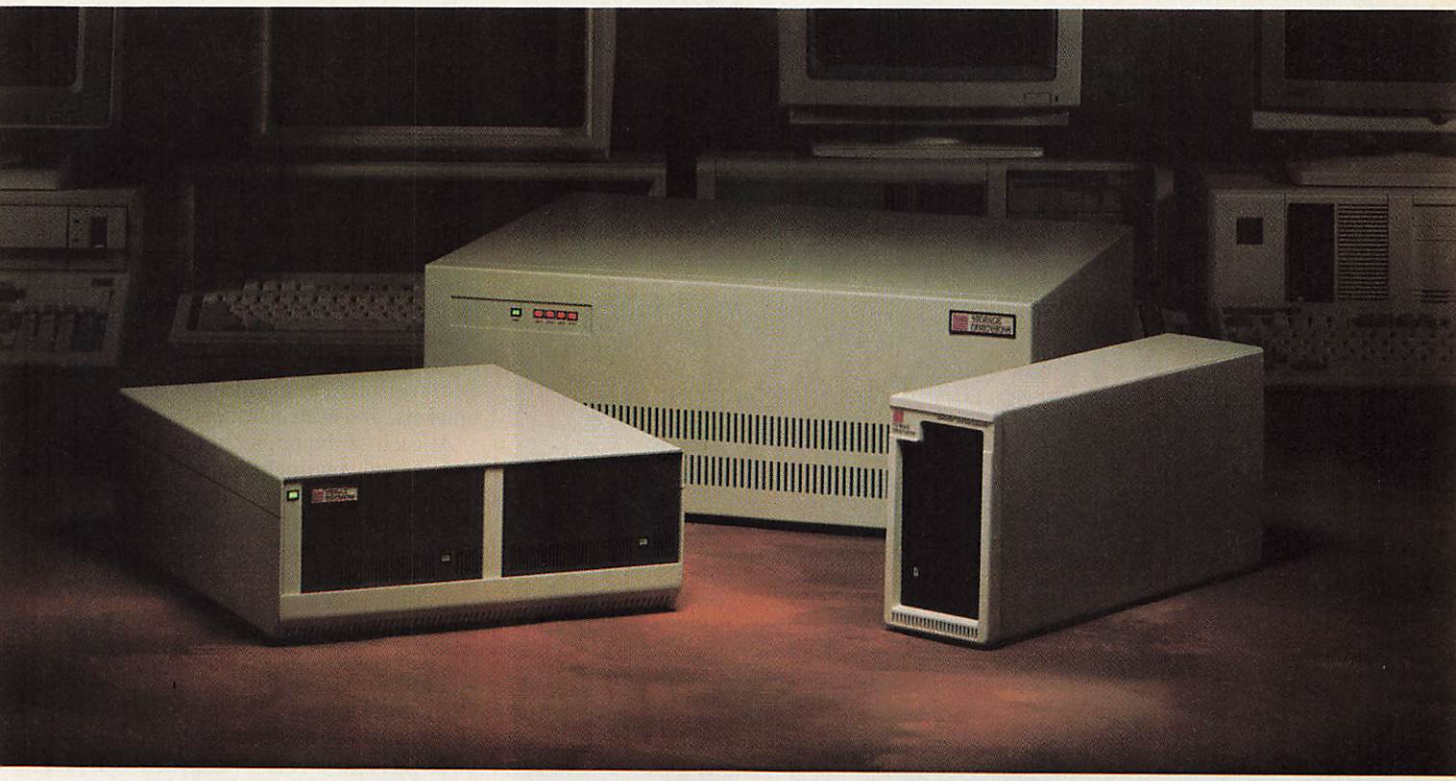
Prototyper can also simulate a real application through the use of demo windows. These are standard Mac document windows (with a title bar, a drag region, a close box, and scroll bars) that are linked to either a text file or a Macintosh graphic (i.e., a PICT resource). When a demo window gets displayed (either automatically at program start-up or through a link to a button or other object), you see the corresponding text or graphic in the window. You can scroll, resize, move, or close the window. Of course, that's all you can do. But with the appropriate choice of content, this feature can go a long way toward simulating a variety of applications—from a spreadsheet to a three-dimensional graphics program.

Code Generation

Prototyper can generate C and Pascal source code. You save your file from

continued

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within Prototyper, launch the appropriate code generator for your target language (C or Pascal), and then tell that program to generate code for a particular language processor. For C, the choices are Think C 3.0 (formerly Lightspeed C), MPW C 2.0, and MPW C 3.0. For Pascal, they are Think Pascal 2.0, Turbo Pascal 1.10, MPW Pascal 3.0, and TML Pascal II.

SmethersBarnes rightfully assumes that it is your responsibility, if you are going to be working with source code, to get a copy of one of these language processors and learn how to use it. The manual includes a section with brief summaries on how to operate the particular compiler you have chosen. The descriptions are concise but sufficient to build an executable file.

The code generated consists of one file for each of the windows or dialog boxes in your application, a main file containing the event loop, and two files for initializing and handling menus. There are also appropriate header files. For C, these header files contain function prototypes per the ANSI standard.

Examining the code that this program produced, I found it well-written, well-commented, and logically structured—more so than many programs that people write. The names are long and descriptive. You can specify two levels of commenting (minimal comments or more extensive ones). For both C and Pascal, you have choices in how to format the code—how much to indent (if at all) the various language elements, such as IF statements, switch and case statements, function argument declarations, variable declarations, beginning and ending brackets, and even comments.

At each of the points in the generated code where you might want to add functionality, there is a comment to that effect. One disappointment is that many of the features present in the interactive simulation disappear when you move to compiled code—e.g., demo windows, hierarchical menus, buttons in windows (as opposed to buttons in dialog boxes), and certain kinds of linked actions. Another problem is that once you edit the generated files and add your code, it is difficult to go back to the interactive tool and add features there. When you generate code a second time, Prototyper isn't smart enough to preserve your handwritten application code. You'll have to wait for future versions of Prototyper to fix these limitations.

Legend has it that the first version of Lotus 1-2-3 was prototyped over a weekend and then completed over the next year. Now the most recent version of 1-2-3 has consumed over 100 person-years of programmer effort. To cope with this changed world, software developers need to expand their repertoire of tools and techniques. One valuable technique is interactive, dynamic simulation of applications.

Prototyper is a well-conceived, accessible, and worthwhile tool that supports this technique. It would benefit from a few improvements: more drawing operations (i.e., better alignment functions, more graphics objects, and more text styles), an extension language like HyperCard's, and a smarter code generator. Nevertheless, it's a valuable tool. ■

Ray Valdés is president and founder of Sapphire Software, a technology consulting firm in San Francisco, California, that specializes in the design and development of graphics software. He can be reached on BIX c/o "editors."

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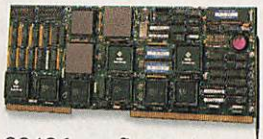
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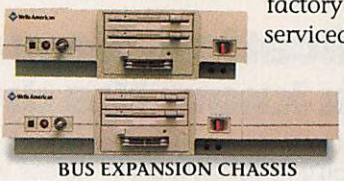
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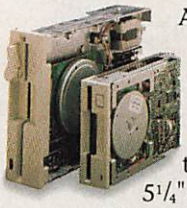
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microExplorer in Action!

TI and ExperTelligence make the Mac II a Lisp machine

Alex Lane

Texas Instruments' microExplorer is a Lisp machine on a NuBus board. Installed in a Mac II, the microExplorer acts as a coprocessor: It handles an application's Lisp internals, and the Macintosh takes care of I/O. The resulting machine looks like a Mac, but it's really a horse of a different color. Although the microExplorer has a slower clock and smaller memory than its big brother, TI's Explorer, it is, in all other respects, every bit as powerful.

Of course, to look like a Mac program, a microExplorer application has to use the Macintosh Toolbox. That's where ExperTelligence's Action! comes in. ExperTelligence developed the original Common Lisp interface to the Toolbox that's still part of the microExplorer's development environment. Action! embeds that Toolbox interface into a visual shell, thus hiding the details of the Toolbox from the Lisp developer.

The Explorer processor on the microExplorer circuit board is a microprogrammed device specifically designed for symbolic processing. The chip features a 32-bit data path and has a 128-megabyte virtual address space with demand-paged memory mapping. Many Lisp primitives and system functions—including device handling, garbage collection, and memory management—are implemented in microcode that's loaded into a control store every time the microExplorer starts up. The writable control store makes for an elegant way to upgrade the system without having to swap hardware.

The distinguishing feature of the Explorer processor—which to me makes the microExplorer a Lisp machine—is its tagged architecture for typed data. Since Lisp is by nature a dynamic and heuristic language (as opposed to static and algorithmic), it's often not feasible to typecheck arguments to functions in advance, so typing occurs at run time. Lisp machines, including the microExplorer, implement this type checking in hardware.

The microExplorer arrived complete with a TI representative who did the installation. Apparently, that's standard procedure—and given the system's $15,000 price tag, probably not a bad idea. The standard microExplorer board comes with 4 megabytes of RAM, but mine came with an additional 8 megabytes of RAM on a piggyback board. The software comes on an external 80-megabyte hard disk drive.

The physical installation of these two components—TI calls them "the board and brick"—was straightforward. The external drive contained a folder called `microExp` with more than 60 megabytes of material, including the microExplorer application, a start-up file, paging files, and the start-up Lisp environment. After ensuring that my Mac was running a post-6.0 OS and that MultiFinder was installed on the external drive, the TI representative spent a couple of hours setting up the software (which included setting up Action!) and giving me the tour.

In addition to the "board and brick," the minimum hardware requirements for a microExplorer system are a Macintosh II chassis, a 640- by 480-pixel monitor, an Apple extended keyboard and a single-button mouse, 2 megabytes of RAM, a tape drive or a floppy disk drive, and an 80-megabyte hard disk drive with 70 megabytes of free space (needed for swapping). But that doesn't leave much headroom on the Macintosh side of the machine. Launching the microExplorer in that configuration left just 128K bytes of memory free. After I boosted the Mac II to 4 megabytes of RAM, memory worries evaporated—as well they should have, in a machine with a total of 14 megabytes of RAM.

Exploring the microExplorer

The microExplorer launches like any Macintosh application. But from then on, it's almost all microExplorer and very little Mac. What comes up is a Lisp Listener window (i.e., the agent that reads Lisp expressions, evaluates them, and prints the results). The Listener also displays the amount of memory available to the microExplorer, and the names and versions of software tools it can access. At the bottom of the screen is a graphical display of current CPU, disk, and garbage-collection activity.

Garbage collection is a technique for reclaiming memory occupied by objects that are no longer accessible. In some Lisp systems, garbage collection is performed on a batch basis, which means that periodically the system appears to lock up while it scavenges for free space in memory. On advanced Lisp systems (including the microExplorer), garbage collection is nearly invisible so that the user never feels it happening. I had to look hard at the garbage collection telltale (at the bottom of the microExplorer screen) to catch the microExplorer in the act. The microExplorer system offers two options for garbage collection: temporal (sometimes called generational scavenging) and batch (which is useful, for example, when preparing clean disk images).

Next to the status display, the system shows the current user and the current package. (A Lisp package is a collection of symbol names; it's analogous to a C library.) The display feature I liked best was the mouse documentation window. It

continued

microExplorer/Action!

Company
Texas Instruments
P.O. Box 202230
Austin, TX 78720
(800) 527-3500

ExperTelligence
5638 Hollister Ave.
Goleta, CA 93117
(805) 967-1797

Hardware Needed
Mac II or IIx with 2 megabytes of RAM and an 80-megabyte hard disk drive

Software Needed
System 6.0 or higher or MultiFinder 6.0.1 or higher

Price
microExplorer processor with 4 megabytes of RAM and supplied software: $11,995
Additional 4 megabytes of RAM: $3495
Additional 8 megabytes of RAM: $5995
Development software: $3995
Action! software: $1995

Inquiry 883.

shows what mouse-selectable functions are available in different regions of the screen, and it describes those functions. Symbolics and Xerox Lisp machines work like this. It's an effective way to make users productive quickly.

The microExplorer's interface closely follows that of the TI Explorer. On the Macintosh, the Option key plays the role of the microExplorer's Meta key, and F5 serves as the System key. To simulate the microExplorer's three-button mouse, you use the Option and Apple keys in conjunction with a mouse-click to access functions attached to the second and third buttons.

Major software components in addition to the Listener include a Lisp compiler, an interactive debugger, several Inspectors, the ZMACS text editor, and a Macintosh Toolbox interface. The compiler converts Lisp functions into *macrocode*. The debugger helps you examine the environment in which an error occurs. The Listener uses a text-based debugger; there's also a window-based debugger that performs substantially the same functions, but graphically. Inspectors view data structures. There's one Inspector for examining standard Lisp structures, and another for examining *flavors*.

Flavors are part of an object-oriented facility featured in all Explorer systems. A flavor defines a data type and a set of operations (methods) that operate on that data type. You can combine flavors to yield a new flavor that inherits the properties of its constituents; object-oriented programmers call this "multiple inheritance." Both Inspectors support the examination of several flavors concurrently in separate panes, and they maintain an inspection history so that previously inspected objects can be easily reexamined.

The ZMACS editor is a clone of Richard Stallman's EMACS—the traditional text-editing tool for Lisp environments. As such, it provides hundreds of useful functions. One function I liked was the ability to select and compile parts of a ZMACS buffer. This came in handy when working with a body of Lisp code I'd acquired by means of a hand scanner. The file I loaded into ZMACS contained several errors that resulted from the scanning process. I was able to compile the buffer in manageable chunks, and by applying the debugger to the resulting errors, I sorted things out with remarkable speed.

The Macintosh Toolbox interface gives Lisp code the ability to access the Toolbox routines. Prior to the advent of Action!, that was how microExplorer developers gave their applications the look and feel that Macintosh users expect. The `tb` package is organized along the lines of *Inside Macintosh*; the Mac's ROM calls and arguments have been Lispified in a way that will be transparent to experienced Macintosh programmers. Of course, you wouldn't use a microExplorer for serious Mac-specific development; rather, the point is to deliver a powerful Lisp application that presents a Mac-like face to the world. That's where Action! comes in.

Ready for Action

Although Action! doesn't openly proclaim itself to be a CASE tool, that's what it is. It has five components: the User Interface Objects, the Smart Editor, the User Interaction Manager, the Menu and Keyboard Management System, and the Development Tool. Users spend most of their time with the first two of these.

The User Interface Objects are a group of Lisp flavors that represent the elements of the Macintosh interface—menus, dialog boxes, scroll bars, icons, and fields. These flavors all derive from the root flavor `Rect` (for rectangle); they're subdivided into the flavors `DisplayObject` (for pictures and text) and `ControlObject` (for buttons and scroll bars). The Smart Editor instantiates these flavors and, by way of dialog boxes and menus, helps you position, size, and align the interface objects and specify the actions associated with them. An Action field is usually associated with an interface object; the field is where you put the name of the Lisp form that should fire up when a user clicks on the object.

The User Interaction Manager and the Menu and Keyboard Management System work behind the scenes, trapping system events and dispatching messages to appropriate objects. The Development Tool builds a text file that documents the components of the interface under development. You launch Action! by double-clicking on its icon or by invoking it from the Listener. Once it's launched, you're operating in a dual mode. That is, the Mac's menu bar includes items that belong to Action and—as you begin to construct an application—items that belong to the application you're building. To keep the categories distinct, Action!'s items appear in red, prefixed by a bullet. If you press Command-Space, you switch modes; Action!'s menu items disappear, and you're no longer editing your application—you're running it.

When you choose the New item from Action!'s File menu, a window appears in which you can begin assembling User Interface Objects. You place these objects in the window with the aid of the Action! keypad. The keypad is a calculator-like device whose buttons represent interface objects. To select an object, you drag the mouse to the object's icon and release the button; an instance then appears in the window. You can move, group, ungroup, and align objects in the window—in short, you can arrange them any way you want.

One example in the Action! manual constructs a slide show with buttons labeled "start," "advance," and "reverse," and a `PictObject` that represents the slide. The `PictObject` is named `:proj`, and the code linked to the start button is this Lisp form:

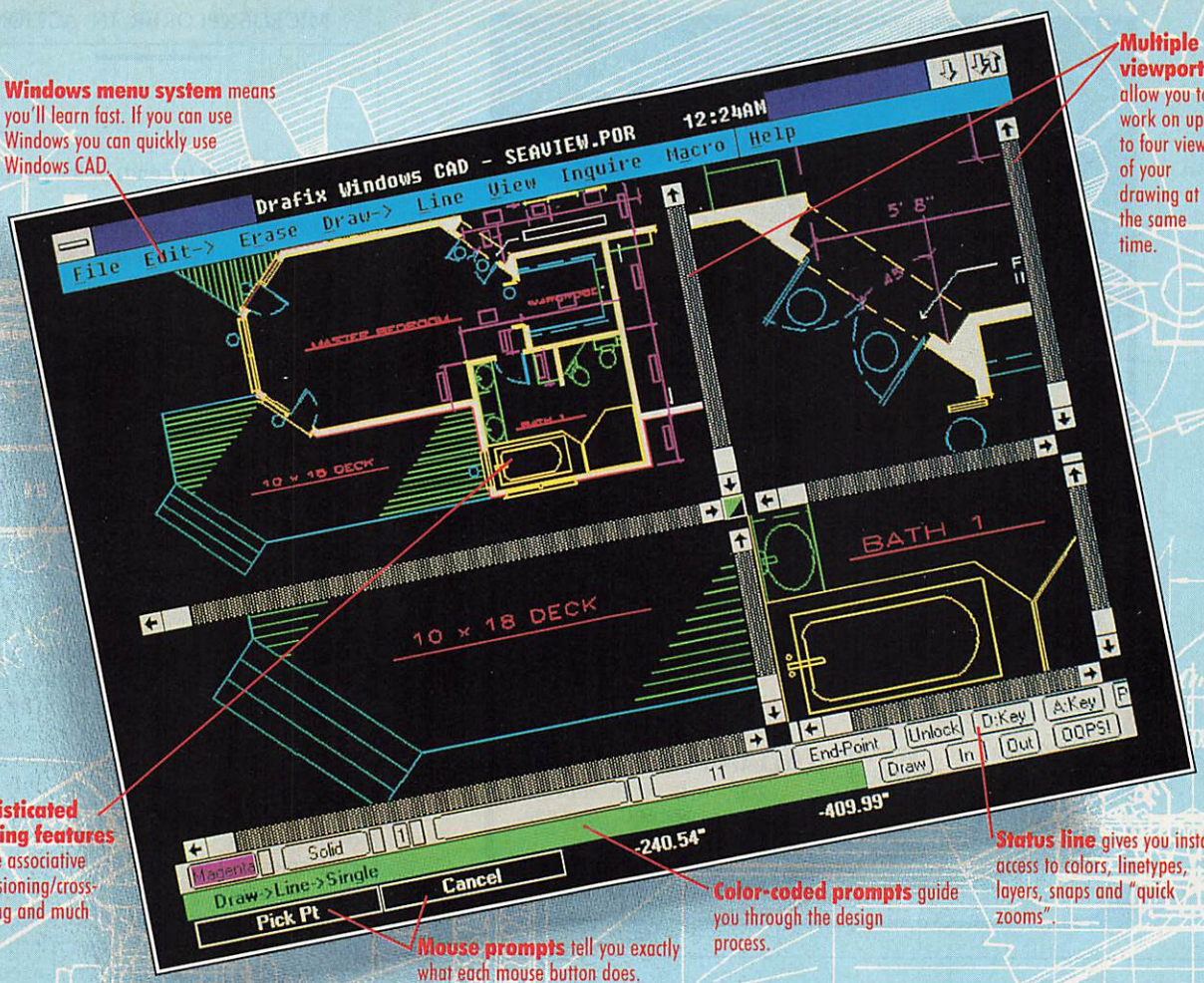
```
(tb:set-value :proj
 (setq *cnt* 6000))
```

In English, this expression sets the value of the `*cnt*` (associated with `:proj`, the `PictObject`) to 6000—the resource ID of the first picture in the slide show. Expressions linked to the advance and reverse buttons increment (or decrement) that resource ID, wrapping around

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On-Line "Help" system

Macro Programming Language

System Requirements ☐ '286 or '386 processor ☐ Microsoft Windows 2.1 or later ☐ 1 Mb internal memory or greater ☐ Windows-supported mouse

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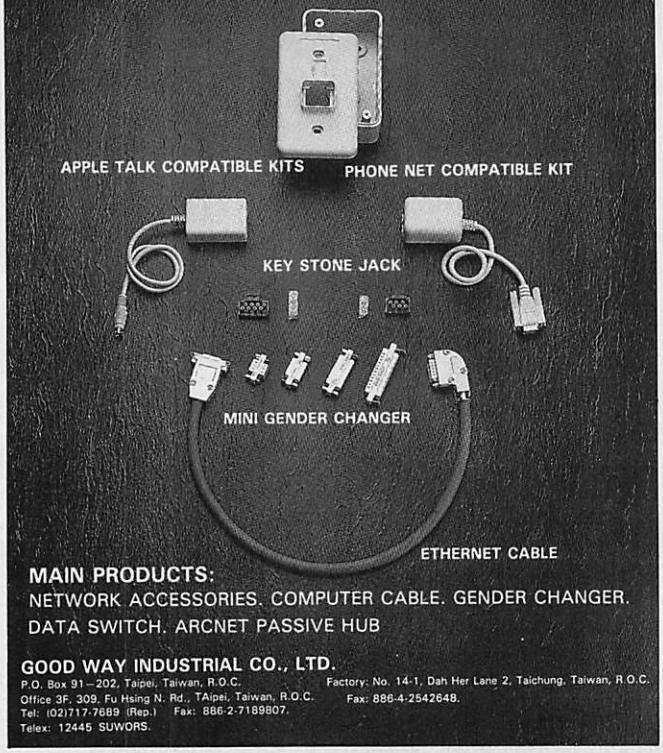
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to the beginning (or end) of the list of IDs if necessary.

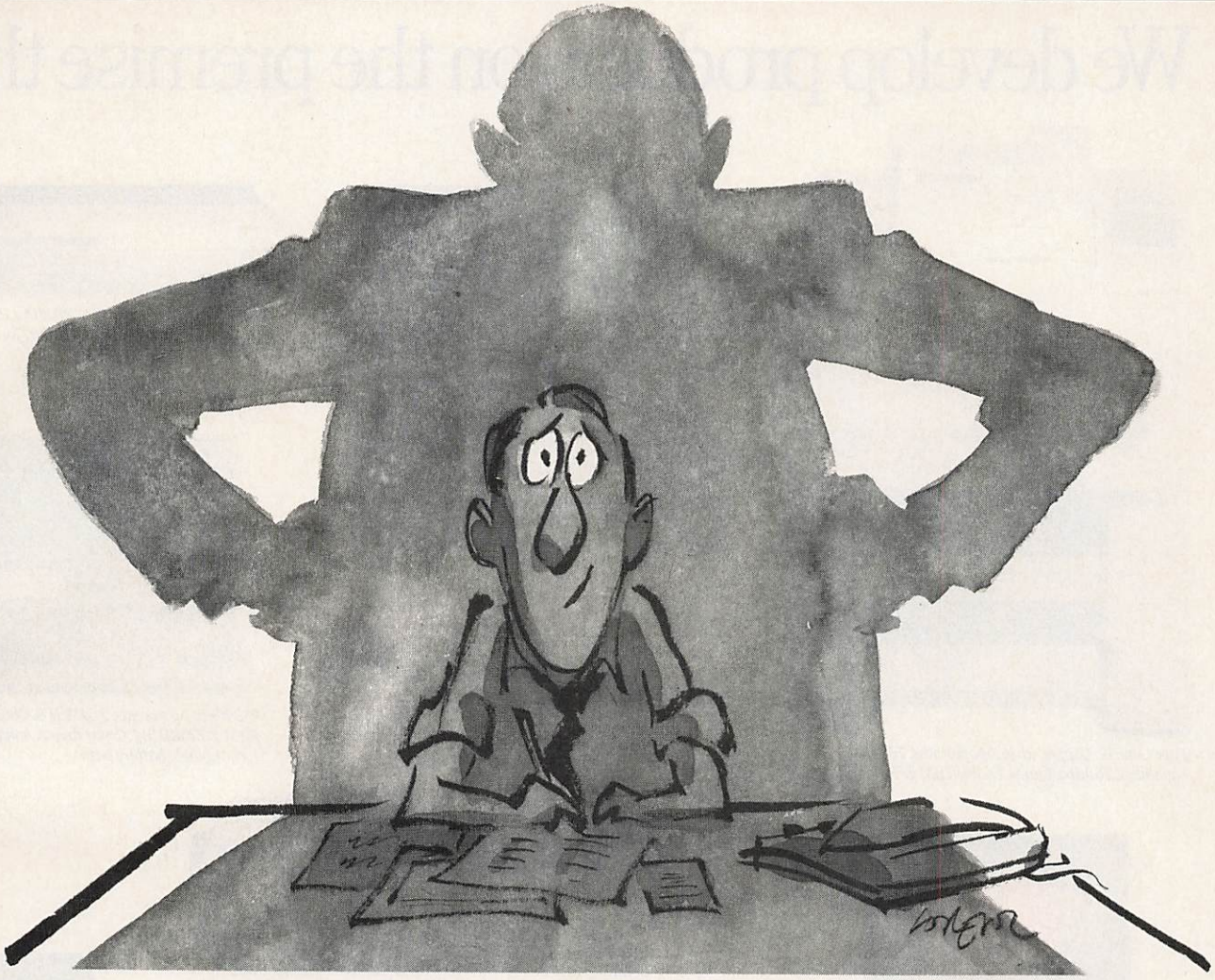
Another, more complicated example creates an address book. Here, several `FieldEditObjects` are used to represent name and address fields, and `ButtonObjects` handle New, Save, and Find actions. Find's action searches the address list for an entry that matches the fields specified in the main window. If that fails, an alert appears. Interestingly, the alert runs as a separate Action! application. This confused me at first, but it turns out that because an Action! application owns just one window, you must build multiwindow programs out of separate components that you store together in a folder.

Once you've got things working properly, you'll want to create a stand-alone, double-clickable application. The Lisp function `define-mac-application` does that. Of course, real applications aren't quite so simple. Action! can only help you build an interface. You're on your own when it comes to writing the microExplorer Lisp application to which that interface grants access. But Action!'s graphical, object-oriented approach makes the Mac-specific part of the project a breeze. You don't need a lot of Mac-specific knowledge—Action! successfully shields you from that. The documentation takes you through the development of several sample interfaces, and it does a good job of describing the User Interface Objects included with the package.

I tested the microExplorer at work, in the midst of a crowd that's done quite a bit of development work in Lisp on a variety of platforms. The souped-up Macintosh received a uniformly positive reception. Veteran Lisp hackers found that the microExplorer offers many of the capabilities they'd grown familiar with on Symbolics and Xerox Lisp workstations. Those who had worked with the Explorer saw the microExplorer as a less-expensive, code-compatible version of its big brother. Of course, less expensive is by no means inexpensive, but the microExplorer does offer the option of a scaled-down delivery system. You can develop on a 12-megabyte microExplorer, but you can deliver on a 4-megabyte microExplorer. That should put the benefits of hybrid Macintosh/Lisp technology within the reach of more users. ■

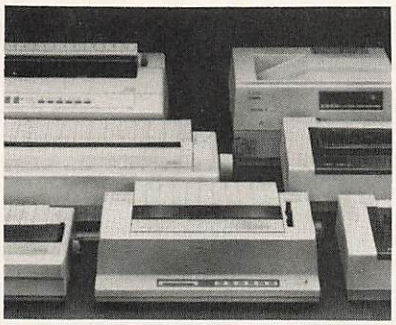
Alex Lane is a senior knowledge engineering consultant for Technology Applications, Inc., and lives in Jacksonville, Florida. He can be reached on BIX as "a.lane."

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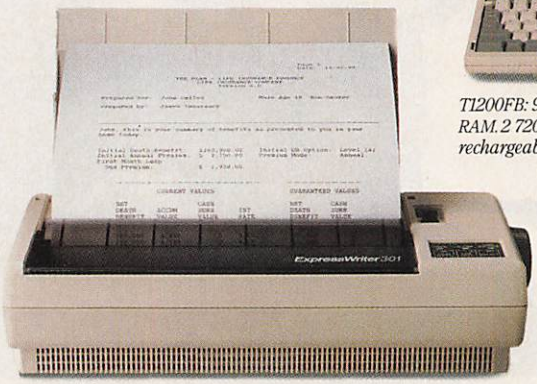
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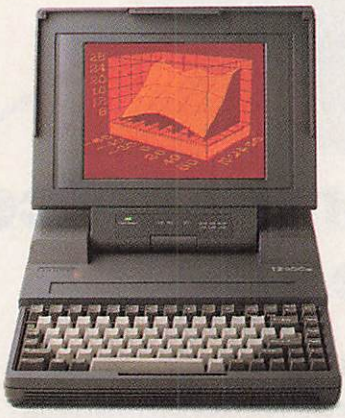
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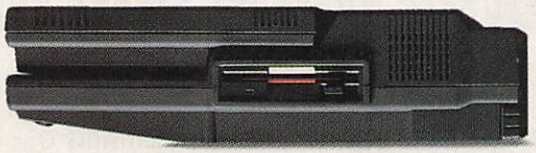
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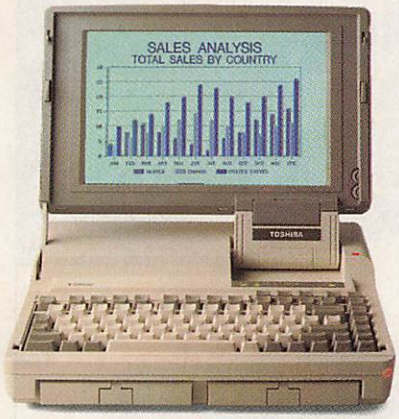


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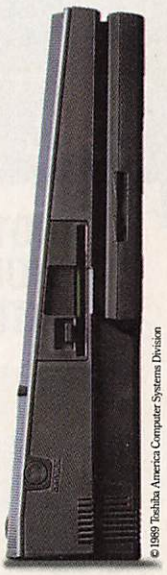
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T3200: 12MHz 286, 2 IBM compatible slots. 40MB hard disk, 1.44MB floppy, 1MB RAM expands to 4MB, EGA screen.

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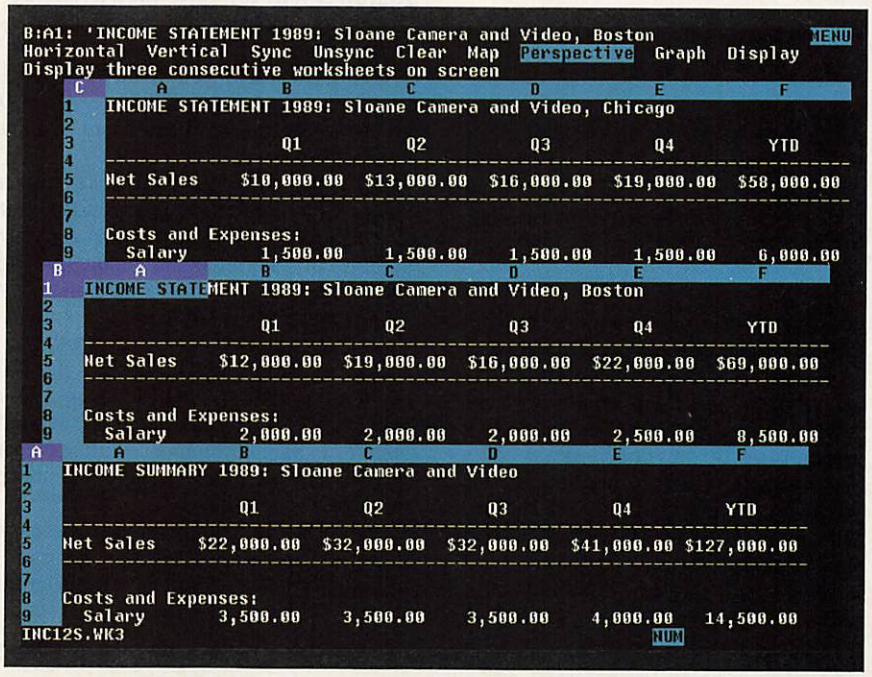
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For Power Users Only

The power and flaws of Lotus 1-2-3 release 3.0 make it a program for the few of us

Edward Reno



Lotus 1-2-3 release 3.0 uses a rigid windowing format.

At the risk of giving a false impression of my high regard for Lotus 1-2-3 release 3.0, I want to tell you about its major drawbacks. It has three: namely, slowness, hidden expense, and incomplete presentation graphics enhancements.

The biggest problem with 3.0 is that it is slow. However, the standard BYTE benchmark tests (see table 1) show that 3.0 was only marginally slower than releases 2.01 and 2.2 in basic calculation speed. In the Scroll Right test, 3.0's screen refresh capability blew 2.01 and 2.2 away. (That advantage will bring consolation only to those who still don't use the End key to navigate around the spreadsheet.)

When I used 3.0 on my real-world spreadsheets, I got a different view. I ran the Calc, File Retrieve, and File Save tests on 3.0 using a 927K-byte spreadsheet, which is what I commonly work with. Here, the real difference between 3.0 and 2.01 became obvious.

I used both an 80386- and an 80286-based system. On the 80386 machine (a PS/2 Model 80-111), 3.0 took over 40 percent longer to calculate my spreadsheet than did 2.01 or 2.2. That difference was amplified on the 80286 machine (an AT), where 3.0 took nearly four times longer than 2.01 and over 10 times longer than 2.2.

However, in saving and retrieving a file from disk, the results were mixed. On the PS/2, 3.0 and 2.01 took about the same time to retrieve the file, and 2.2 was the hands-down winner. Times for saving the file under DOS were also about the same, but 3.0 saved the file notably faster under OS/2. Release 3.0 didn't fare well at all on the AT, taking six times longer to retrieve a file.

I suppose I could run a theoretical calculation that would show that, during the course of my life expectancy, I would end up sacrificing several weeks because I used 3.0 rather than 2.01 on an 80386 machine. But I can live with that—as long as my spreadsheets don't get too big.

What I cannot live with, however, is 3.0 running on an 80286 machine—at least not on an 8-MHz machine configured similarly to mine. The 185-second Calc test that takes 39 seconds using the old version of 1-2-3 is a bit much. And a File Retrieve discrepancy of 386 seconds under 3.0 to just 56 seconds under 2.01 is intolerable. Those few weeks running 3.0 rather than 2.01 on an 80386 machine could easily become several years on an 80286 machine.

Part of the problem is that—unlike 2.0—Lotus wrote 3.0 in C rather than in assembly language. Release 3.0's speed is further compromised by its use of overlays in DOS and virtual memory in OS/2. In both cases, this means that disk swapping of code occurs in many operations, even in the Calc test.

Minimal Recalc and Background Calculation

Two features in 3.0 try to mask some of 3.0's loss of calculation speed. One feature, Minimal Recalc, was available as a Lotus-supplied add-in for 2.01. It causes

continued

Lotus 1-2-3 release 3.0

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the spreadsheet to recalculate only those cells affected by a particular change.

In addition, 3.0 also has background calculation, which lets the program continue to calculate as long as it is not being preempted by keyboard input. Since there are many pauses in all but the most intensive keyboard input, the theory is that your spreadsheet will be continuously updated.

The theory works fine on small or otherwise simple spreadsheets. But anyone with large and complex spreadsheets will find these features practically useless. On my 927K-byte spreadsheet, for example, when editing a formula that contained only a single-cell reference, I pressed Return to move the cursor out of that cell and on to another operation. I had to wait 8 seconds for 3.0 to write the new value of the cell to the screen. On the AT it was much worse; it took 133 seconds to write the data to the screen. I promptly turned off background calculation.

Requirement for Extended Memory

There are also some memory management issues for 80286-based systems. When Lotus says you need at least 1 megabyte of available RAM to run 3.0 under DOS, the word *available* hides a dual requirement.

First, the additional 384K bytes over a base 640K bytes must be extended, not expanded, memory. Depending on your system, this could mean reconfiguring 384K bytes of your expanded memory (assuming you already run large spreadsheets) for use as extended memory.

I also found that a 927K-byte 3.0 .WK3 file took only 884K bytes in .WK1 format. If you are playing at the ragged edge of expanded memory with some of your files, you may have to add more memory.

An 80386 machine can easily escape these problems. It just has to run a memory manager that conforms to the Virtual Control Program Interface (VCPI) specification. Some examples are Qualitas's 386Max, Compaq's Extended Memory Manager (CEMM), and Quarterdeck's Extended Memory Manager (QEMM).

These problems have a conceptually simple solution: Buy an 80386 system with lots of memory. Lotus is offering an upgrade to 3.0 for $150 until the end of the year. But the real expense of upgrading to 3.0 will be for new hardware. None of the release 2.01 add-ins will run with the add-in manager that Lotus has built into 3.0. The problem is that the power user who really needs 3.0 is also the one who is most likely to have add-ins in the first place. In my case, unless Symantec comes out with a 3.0-compatible version of SQZ! pretty soon, I may be forced to upgrade my hard disk drive.

Incomplete Presentation Graphics Enhancements

The good news about 3.0's graphics is that you can display graphs on the same screen with cell entries and print graphs directly without going through the PrintGraph program.

A new automatic graphing feature allows 3.0 to guess what data it thinks you are looking to graph. There are also new types of graphs, some of which are wholly new, such as the High-Low-Close-Open graph, for those who cheat a little on their corporate CompuServe or Dow Jones subscriptions and load in the stock prices for their own portfolios. In additon, a new mixed graph lets you

continued

Table 1: *Lotus 1-2-3 release 3.0 proved to be too slow for large spreadsheets on an 80286-based IBM PC AT. All times are in seconds.*

	BENCHMARK RESULTS						
	PC AT[1]			PS/2[2]			
	DOS 3.3/ 1-2-3 2.01	DOS 3.3/ 1-2-3 2.2	DOS 3.3/ 1-2-3 3.0	DOS 4.01/ 1-2-3 2.01	DOS 4.01/ 1-2-3 2.2	DOS 4.01/ 1-2-3 3.0	OS/2 1.1/ 1-2-3 3.0
Savage	3.4	3.8	4.0	1.2	1.2	1.3	1.1
Recalc	2.1	2.9	4.0	0.8	1.0	1.2	1.1
Scroll Right	35.0	34.5	2.3	10.3	9.1	0.3	0.3
Large Spreadsheet[3]							
Calc	39.0	16.0	185.0	8.7	6.0	12.4	12.2
File Retrieve	56.0	66.0	386.0	97.2	35.0	84.0	98.0
File Save	47.0	46.1	113.0	61.2	61.2	59.3	40.0

[1] IBM PC AT 5170 with an 8-MHz 80286, an 80287 math coprocessor, 512K bytes of RAM on a system board, a 2-megabyte Intel AboveBoard AT, an AST Advantage! with 640K bytes of extended memory, and a 71-megabyte MiniScribe 6085 hard disk drive.
[2] IBM PS/2 Model 80-111 with a 20-MHz 80386, an 80387 math coprocessor, 4 megabytes of RAM, a QEMM memory manager, and a 110-megabyte hard disk drive.
[3] Worksheet is a forecasting model that was built for business use using Lotus 1-2-3 release 2.01. In .WK1 format, the worksheet takes up 884,117 bytes. In .WK3 format, the worksheet takes up 926,982 bytes.

Note: Tests run under 2.01 and 2.2 used the .WK1 format. Tests run under 3.0 used the .WK3 format.



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combine a line and clustered bar graph. Other features include the ability to create horizontal graphs, stacked graphs that convert into surface charts, and double *y*-axes graphs.

Added to these goodies are enhanced color, hatching, and gray-scale capabilities. Text is a bit easier to work with; you can add up to two footnotes per graph, and, similar to Lotus's Symphony, you can do logarithmic scaling on any axis.

The bad news for this three-dimensional spreadsheet is that, strangely, a 3-D graphing capability is missing. Also missing is the ability to have directly interactive and nameable settings sheets, as in Symphony. The irritation is compounded by all these capabilities having been built into 2.2.

The one significant exception involves print settings, which you can save and retrieve by name in 3.0, although you cannot view these settings in tableau format on the screen. Curiously enough, however, you can print them out.

Finally, although 3.0 has some print enhancements, it has no full-featured presentation printing features like those in Funk Software's Allways. The rub is that those features are included in 2.2.

The Glass Is Really Half-Full

Release 3.0 contains new features that will delight named-range addicts. One of the most satisfying is the ability to use as-yet-undefined range names in a formula you are composing. You can place a range name where you think it belongs, even before you've defined the coordinates for the name. You can also point and shoot range names when you are building formulas and when you are editing. These features also let you create a new range name whenever you want, even if you are far into a formula.

Formulas can be up to 512 characters long. You can also attach a note of up to 512 characters to any range name. This will ease the pain of your not being able to use Note-It or similar cell annotation add-ins in 3.0.

Finally, you can name macros directly, not just in branching statements, with any name of up to 15 letters. This allows you to exceed the previous limit of 27 master macros.

New @ Functions

Release 3.0 has 14 new @ functions. The maximize-the-cash-flow crowd will revel in `@VDB`, which lets you simultaneously compute double-declining-balance method and straight-line method depreciation and then automatically select whichever

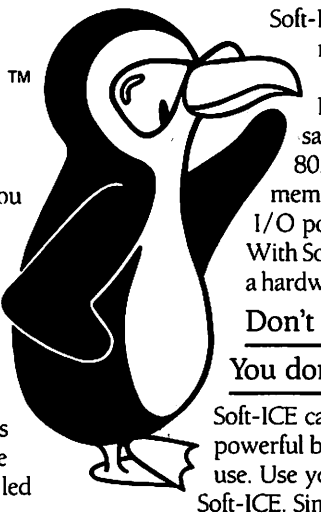
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I found two relatively minor bugs with 3.0 that Lotus is addressing.

value is greater.

Statistical gurus will appreciate the addition of @STDS and @VARS and their related database statistical functions, @DSTDS and @DVARS. These features let you calculate the sample standard deviation and variance, in addition to the population standard deviation (@STD and @DSTD) and variance (@VAR and @DVAR), which 1-2-3 has always allowed users to calculate.

I think everyone will be grateful for the reappearance of the simple, old-fashioned @TODAY, which succumbed between 1985 and 1989 to the roundabout @INT(@NOW). Release 3.0 also has some worksheet auditing functions—particularly useful with 3-D spreadsheets.

A new database function, @DGET, lets you go into a database and pluck out a specific detail in a record. Finally, the @DQUERY function will, if more fully implemented through optional DataLens drivers, have the ability to take an entire database query language (e.g., Structured Query Language, or SQL) as its arguments—that's a powerful feature.

Printing Features

A new range of printer layout options is controlled from the Print menu. You can now point to and select print styles and fonts from the Print menu. If you don't like the preset options, you can use the setup string in the Print menu.

Release 3.0 also handles background printing. You can specify more than one print range in a single-range statement, the cell reference for the contents of headers and footers, and a particular number for starting pages. You can even print the number and letter coordinates in the worksheet frame along with your data.

Perhaps the most significant print enhancement in 3.0 is the ability to directly print graphs from the Print menu and on the same page as worksheet data. You can print the graph from the Print menu, but you cannot make any changes in its settings at this point. Instead, you must exit the Print menu and go back into the Graph menu, where you can fiddle with the settings until you have them the way you want them, and then go back to the Print menu.

To get graphs on the same screen as cell data, 3.0 goes to bit-mapped screen presentation in EGA and VGA mode. The somewhat jagged-looking font that results is not as pleasing to look at as the older-style full-character font. At installation, you can also specify two displays.

Gotcha!

I found two relatively minor bugs with 3.0 that Lotus says it is addressing. First, if you run a reverse @SUM function over a range of just two rows, top to bottom, or two columns, left to right, you are asking for trouble. When 3.0 gets down to the limit of two rows or columns, it hiccups when you delete the upper or left boundary in a reverse @SUM, or any other @ range function. For example, instead of



making the expected adjustment from @SUM(A3..A2) to @SUM(A2..A2), it returns the value for @SUM(A2..A1). To add to the confusion, the bug asserts itself in 3-D contexts as well. I don't consider this bug serious since, as a matter of prophylactic work habits, I avoid reverse @ range functions. But other users may get into a pile of trouble over this.

Another problem occurs when you use the Data Fill command with dates. The problem is that if you begin a sequence with February 28 or 29 and try to step it out by monthly, quarterly, or yearly intervals, the command fails. Admittedly, the likelihood of this bug affecting any spreadsheet in a material way is probably beyond 3.0's new 18-decimal floating-point range.

Multiple Worksheets, Multiple Files

The most important enhancements in 3.0 revolve around its 3-D and new database management capabilities. Depending on your memory configuration, you can get up to 256 separate 1-2-3 worksheets into active memory. These worksheets can be all in one file or, through the new File Open command, in as many as 256 separate files, all active in the same session.

The integration between multiple worksheets, even when they run across files, is seamless. You have to get used to the 3-D coordinate references that are cluttered up by worksheet letter references (e.g., A:A1..C:B6, which cuts across three worksheets, A, B, and C). Where different files are being referenced, you have the extra baggage of file path and filename in double-angled brackets.

But 256 active worksheets is not the end of it. Release 3.0 can now link to files on the disk, and you can reference them in formulas that also include active files. (This is a technology that Multiplan had in 1982.)

My only complaints about 3.0's 3-D capability have to do with the window management and the translation utility. When working in 3-D mode, you are restricted to three rigidly formatted, overlapping windows. You can, however, zoom to full size in a single window and then divide that window in the conventional horizontal and vertical ways.

The problem with the translation utility, which converts 3.0 worksheet files for use with 2.0, is its speed. The translation utility does its job, appropriately flagging those 3.0-specific parts of a file that won't translate fully into a 2.0 environment. But the process is terribly slow.

Database Management: The Secret Revolution

Release 3.0 supports database structures that are effectively relational. Its database structure lets you retrieve records across multiple databases. The program organizes data in a row-column table, with each row corresponding to a record and each column to a field within the record. Thus, retrieving across multiple databases means retrieving from more than one such table with a single command or formula and criterion range. (Of course, the target records in the different database tables must share a common data element.)

Because of 3.0's 3-D architecture, those different tables can exist on different worksheets in the same file, with the criteria and output ranges themselves existing on still other worksheets in that same file. The databases can even be

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spread over different files. With file linking, you can also access 1-2-3 files that are not active, but only disk resident.

In addition, external databases are accessible, in principle, to 3.0 through what Lotus calls DataLens drivers. Lotus supplies a single DataLens driver for dBASE III database tables. It also supplies a sample table in dBASE format so that you can try out the driver.

The DataLens technology is currently incomplete, however. In particular, the new @DQUERY function, which supposedly will allow you to nest entire foreign database query languages under it, is not yet operational. If and when it is fully implemented, and if Lotus can persuade other DBMS software vendors to use DataLens drivers, 1-2-3 stands a chance of maintaining its commanding position in the power-user market.

Other major enhancements to 3.0's database management facilities are fully complete, however. The most powerful is the Data Table 3 functionality. Its concept is simple enough; it's a Data Table 2 with a *z*-axis. It is no more complicated than that in its simplest "what-if" form.

Moreover, you can draw input from databases and use database statistical functions such as @DSUM, @DMAX, and @DSTD for sifting the contents of databases into three dimensions. When combined with the ability of 3.0 to query multiple databases—on disk as well as in active memory—there is little limitation for what you can do with database management in 1-2-3. Other significant database management enhancements include a free-form version of data tables and sorts on up to 256 keys.

Does It All Add Up?

Release 3.0's improvements—particularly the database management and 3-D worksheets—are worthwhile. But those improvements come with a sacrifice in speed, additional hardware costs, and disappointing graphics. Furthermore, program developers using the new Lotus Development Environment have yet to produce any add-ins.

An imperfect instrument, Lotus 1-2-3 release 3.0 is still in the process of formation. Despite its flaws, I like 3.0 and have decided to upgrade. In my opinion, 1-2-3 has always been the most important thing happening on the desktop—3.0 has only confirmed that opinion. ■

Edward Reno is vice president of planning and development for the Computers and Communications Information Group at McGraw-Hill. He can be reached on BIX as "ereno."

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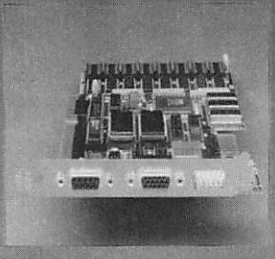
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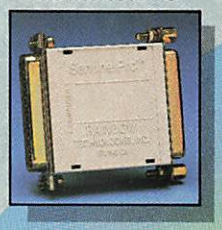
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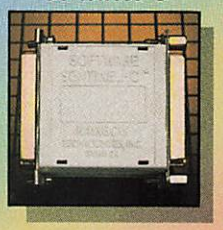
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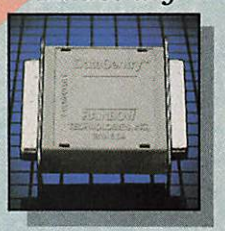
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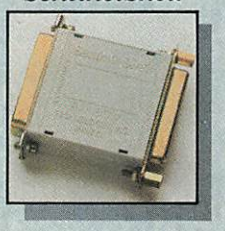
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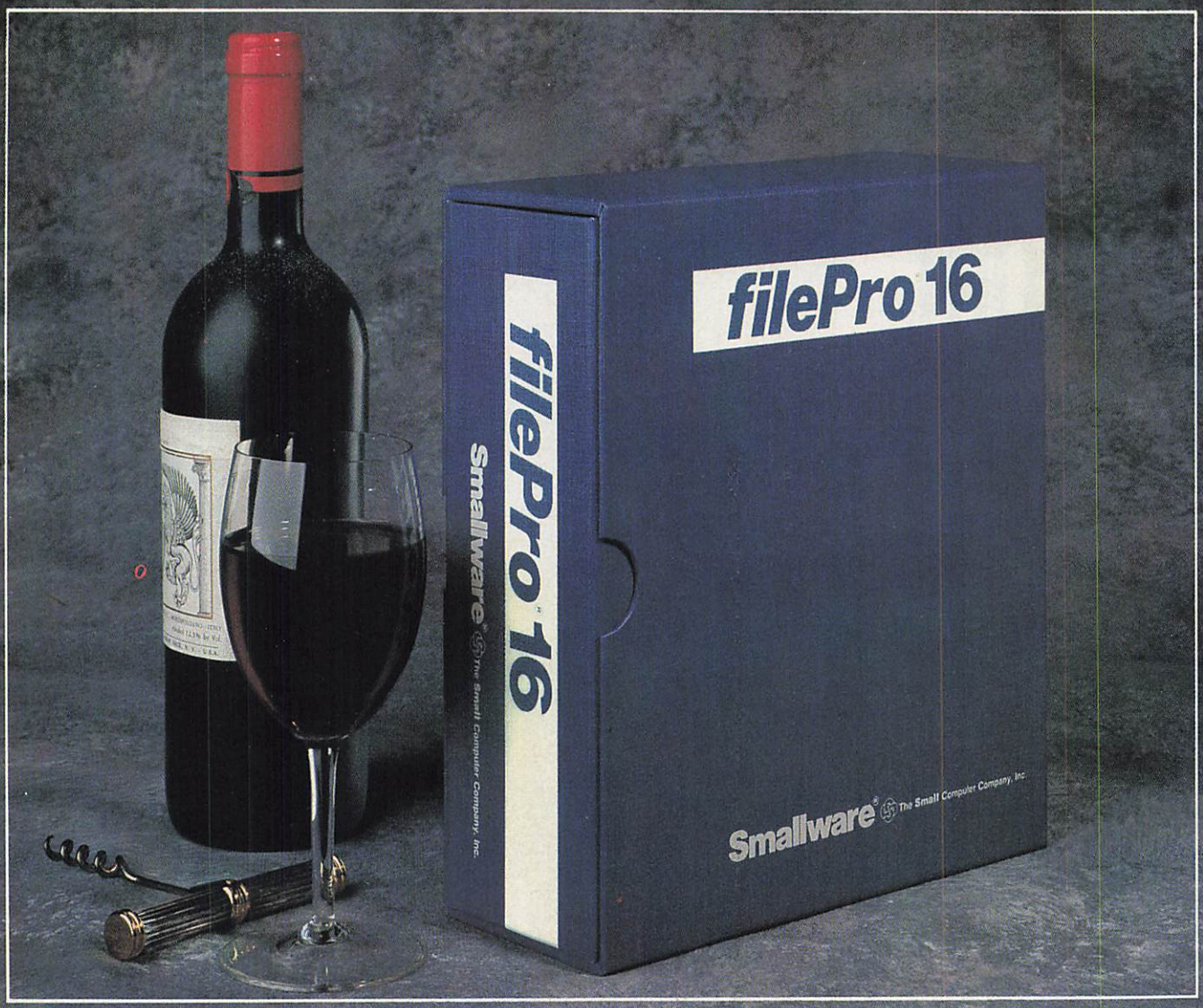
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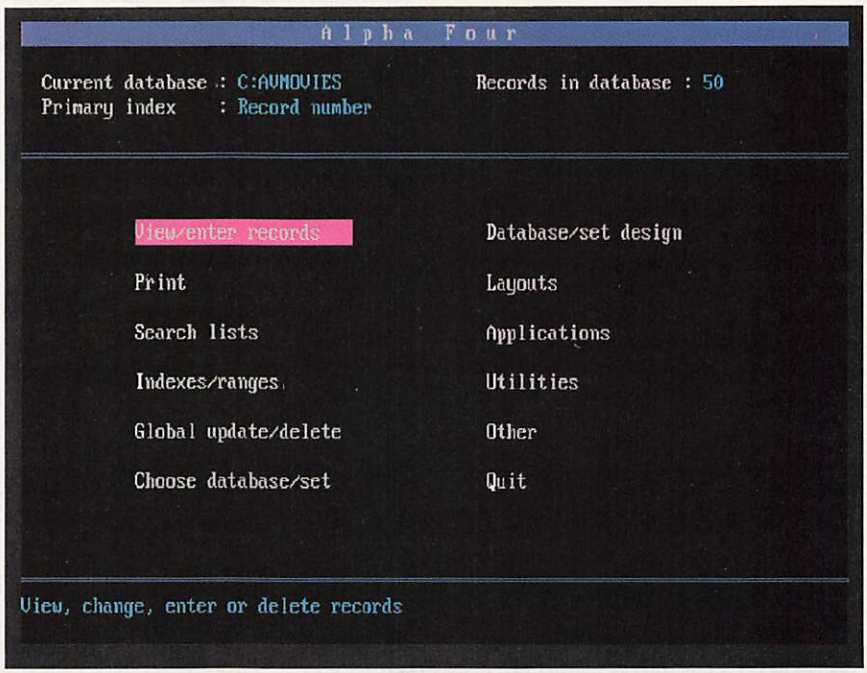
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Alpha Four: No Programming Required

This relational DBMS features dBASE compatibility and ease of use, but at a performance cost

Malcolm C. Rubel



Unlike dBASE IV, Alpha Four is totally menu-driven.

Although dBASE is popular, it has never been easy to use. Alpha Four may solve this problem. It provides almost complete compatibility with dBASE III Plus files while also providing a full range of screen, report, label, mail merge, and other capabilities that are already set up.

With all that it does, Alpha Four takes a lot of hard disk space—2.4 megabytes, to be exact. I also found a little hitch in it while installing it. The program modifies the existing CONFIG.SYS file, or it creates a new one with Alpha Four's file and buffer requirements; however, when I installed the program on drive F, the installation program made a CONFIG.SYS file on drive F instead of on drive C.

Alpha Four comes with over 120 different printer configurations, covering the most popular printers. Special configurations are available for printing envelopes on a Hewlett-Packard LaserJet. The only important item missing is a generic PostScript printer driver.

Alpha Four includes an excellent tutorial that provides good examples of both simple and complex database management tasks. The documentation is also well written and complete.

The program is almost totally menu-driven, and moving from one menu to another is logical and intuitive. A person with little or no database management experience won't have any trouble figuring out what comes next. I wish that other programs were laid out as well. Good online help is also available.

dBASE Compatibility

Alpha Four can use dBASE III Plus data files directly. It works with database files (.DBF), memo files (.DBT) and index files (.NDX). However, Alpha Four cannot use dBASE IV files, because it does not support the master index file type (.MDX) or the memo file (.DBT) that dBASE IV uses.

I did find one incompatibility between Alpha Four and dBASE—it has to do with templates. With dBASE, you can choose not to store formatting characters, which are used as a part of a template, as data. The picture function @R handles this. With Alpha Four, the picture-formatting characters are automatically part of the field value when it is stored. In other words, in dBASE you can store the telephone number "(212) 555-1212" in a character field with a length of 10 (just the digits) using the picture function, while with Alpha Four, you must specify a length of 14. If you try to create a template for the field, you will run out of space before you run out of numbers. In this case, you will have to suffer the extra 4 bytes per record that this implies.

Although Alpha Four and dBASE share the same database file structure and the same indexing routine, little else about the two programs is similar. Alpha Four cannot run user programs. There is no "dot prompt" to contend with or use.

continued

Alpha Four 1.05

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Instead, you define the necessary pieces of an application from different specification screens and work surfaces. Alpha Four can use the individual pieces, or you can integrate them into a complete application. Database tables are related to other database tables in sets, with the links defined and established only when the set is constructed. You define data-entry screens, reports and labels, filters, and mail merges from their own modules, and you can call them independently or as part of a larger application.

As with dBASE, you can set ranges and filters with Alpha Four. You can change the active index, set a filter, and save it all from within one screen. While Alpha Four does not provide you with a point-and-shoot filter builder, it does provide you with access to all fields, functions, and logical operators while you are building your filter expression. Alpha Software is also good enough to recognize and tell you that filters slow down processing and that you should, where possible, try to index on the filter expression, set that as the active index, and then indicate the range for the desired data.

Forms Design and Field Rules

The Alpha Four forms feature lets you design screen-entry forms visually. The forms designer is WYSIWYG, and it lets you print directly from the forms design. With this feature, you don't have to create the same design twice, once for the screen and once for printing.

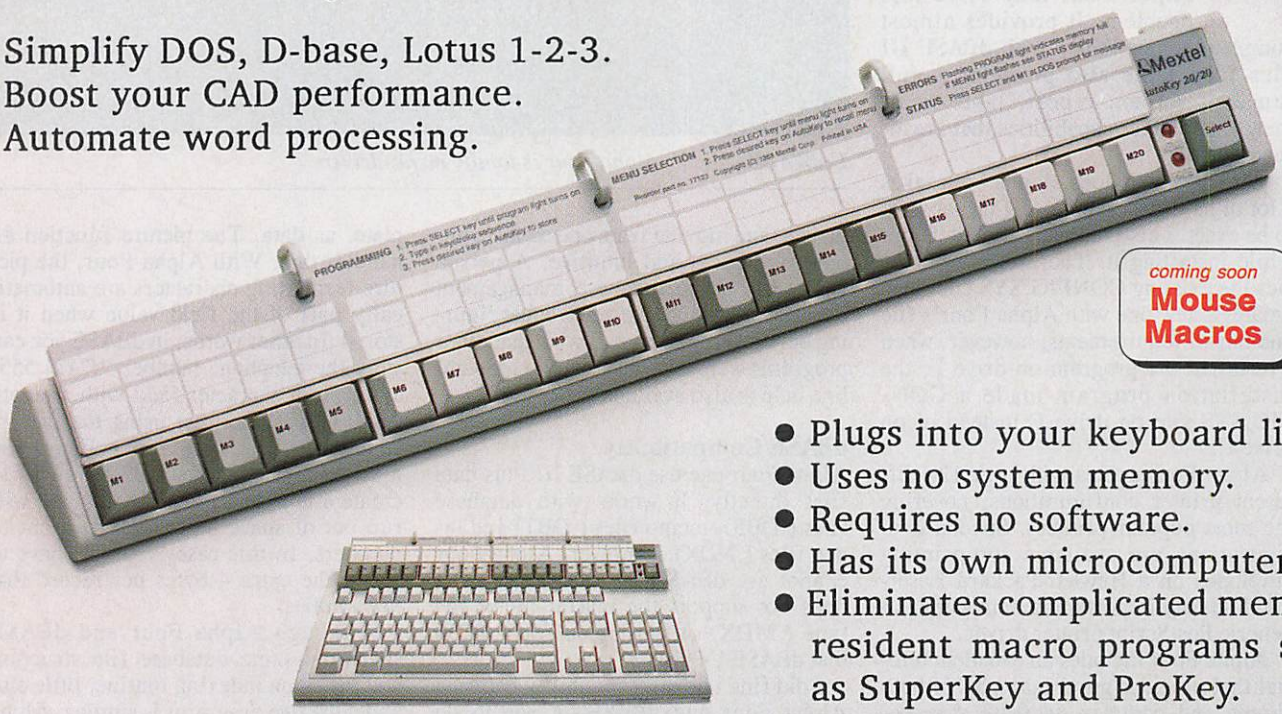
A major difference between the Alpha Four forms designer and dBASE is that with Alpha Four, you don't use any editing rules in the screen form, the way you do with dBASE. To handle this necessary function, Alpha Four uses the "field rules" option from the Database/Set Design utility. With dBASE, you must specify the acceptable values as a part of the data-entry screen, and you must also specify the format template for output as a part of your report program. While this gives you the flexibility to handle the same piece of data differently in different areas of the program, in most instances, it simply means more work. Alpha Four has gotten around this by designating the formats and editing parameters as an integral part of the database design process.

The field rules act more like a data dictionary than anything else. You can create calculated fields, enforce case for alpha data, and supply the editing template and the mask and print template for

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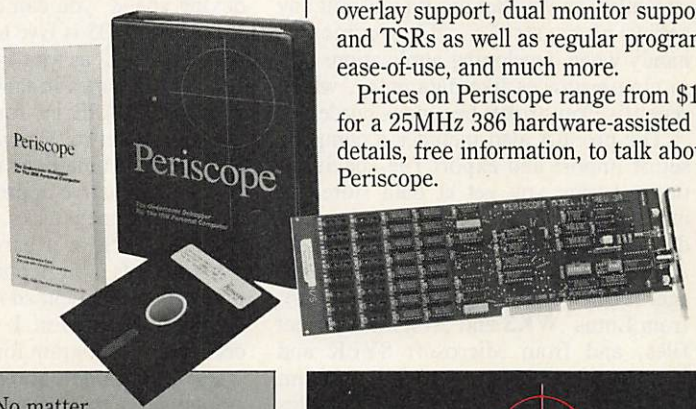
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Table 1: *My tests showed that Alpha Four is somewhat slower in large or compound indexes than dBASE IV. All times are in minutes:seconds.*

ALPHA FOUR VS. dBASE IV

	Alpha Four	dBASE IV
Locate on numeric field (1000 records)	0:04	0:02
Locate on character field (1000 records)	0:03	0:02
Index 1000 records on numeric field	0:04	0:03
Index 5000 records on numeric field	0:30	0:24
Index 10,000 records on numeric field	1:06	0:48
Index 1000 records on compound key	0:10	0:03

each field. You can also indicate whether the mask is to be strictly enforced or whether exceptions can be made to it. You can supply either a default value or a calculated default expression as a part of the field rules.

Field rules also let you elect whether or not a field requires an entry. You can even make the field rule dependent on a value in another field. You also have the option of using a valid expression that must evaluate to a logical "true" before the program accepts the entry.

You can specify a condition for which the field is skipped and no entry is required (e.g., if you have a male patient, you don't ask if he's pregnant). You can have the user enter critical data twice to make sure that it's right, and you can supply a prompt for each field. The program lets you perform field lookups either from a table in memory or from a database on disk. You can set the size of the window that pops up and whether it pops up automatically or only on entry of illegal data. Bad data can be that which is already in the table or that which is not. All this is available without any programming.

Alpha Four has even tamed memo fields, which have long been the toughest aspect of screen design with dBASE. Alpha Four simply lets you choose a window for editing memo fields.

Reports, Labels, and Browsing

The report writer included in Alpha Four is powerful. Reports can have up to nine levels of detail and include calculated fields. You can print data in either regular or compressed mode, or with bold, underlining, and italics to highlight important parts of the report. You can even have memo and character fields wrap in specified spaces. Summary reports are also supported.

Probably the most impressive part of the report portion of Alpha Four is that you can make two passes through a report. On the first pass you can generate summary statistics. On the second pass, you can use these numbers (e.g., sales per region as a percent of total sales).

The label-printing program lets you determine the size of a label, how many labels you want across a sheet, how many spaces you need between labels (across and down), the number of copies you want to print, and the labels' contents. You can specify what information goes where and what to do with blank information.

One of Alpha Four's best features is its ability to define up to 26 different browse tables for each set of data. You can define fields to be included in the browse, and you can select the order in which they are to appear. You can also include calculated fields. Unlike dBASE, you can show the contents of memo fields in the browse table.

Macros and Other Good Stuff

Alpha Four provides a keyboard macro capability so you can record and edit any series of keystrokes. This comes in handy when developing applications and in circumstances like data entry, where repetitive keystrokes become a burden.

The product also includes a complete set of import and export file specifications, letting you get at data stored in other programs and also letting you write data to them. You can import data from Alpha Software's Alpha Data Base Manager II (the company's flagship product), from Lotus .WKS and .WK1 worksheet files, and from Microsoft SYLK and VisiCalc DIF files, as well as from dBASE II, PFS: File, and ASCII tables and character-delimited format files. Alpha Four will export in these file formats as well as in MultiMate and WordPerfect merge file formats.

Alpha Four includes the ability to develop and print form letters. As with everything else about Alpha Four, this feature is powerful but still easy to use. Along with all the basic features, Alpha Four lets you pause for operator entry during printing, using calculated fields in the middle of your letter and printing information conditionally. For example, you can automatically generate a different type of form letter that thanks contributors based on the amount they gave.

Last, but certainly not least, Alpha Four contains the ability to define custom menus that let you call submenus, run macros, call another application, or run another application. The generator also allows you to add a prompt line and a help file, if desired. While not terribly sophisticated in its design, the Alpha Four applications generator lets you develop good, solid, basic applications.

The Downside

Alpha Four does a better job than most of the competitive products I've seen. This doesn't mean that I'm a complete fan of the product. Alpha Four is, by definition, limited in what it can do. With a database management product, such as dBASE, which includes a programming language, you will always be able to do things that a defined product like Alpha Four cannot.

Alpha Four does not have a programming language and is not designed to execute even a single line of user program code, so you cannot do anything that's not built into the product. It would help if Alpha Software could put a RUN command in the product that allowed you to swap Alpha Four out of memory and run another program.

On the other hand, if you have heard anything about Alpha Four's lack of indexing speed, you can discount most of it. Version 1.05 is five to 10 times faster than 1.0 and, as you can see from the benchmark times in table 1, close to the speed of dBASE IV for simple indexes but still slower for a compound index.

Overall, Alpha Four represents an excellent alternative approach to handling data management tasks. But at $595, it's not that much of a bargain. I wish the program was a bit peppier than it is, but it's still an excellent ad hoc query device for small databases. I would definitely consider the program for an environment where I had nonprogrammers and novice computer users who want to look at data for themselves. ■

Malcolm C. Rubel is president of Performance Dynamics, a New York consulting firm that specializes in DBMS software. His latest book, dBASE IV Power Tools, *has just been published by Bantam. You can reach him on BIX c/o "editors."*



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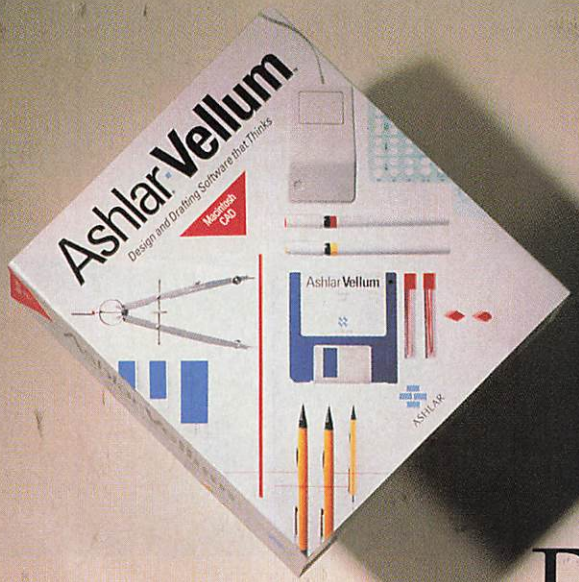
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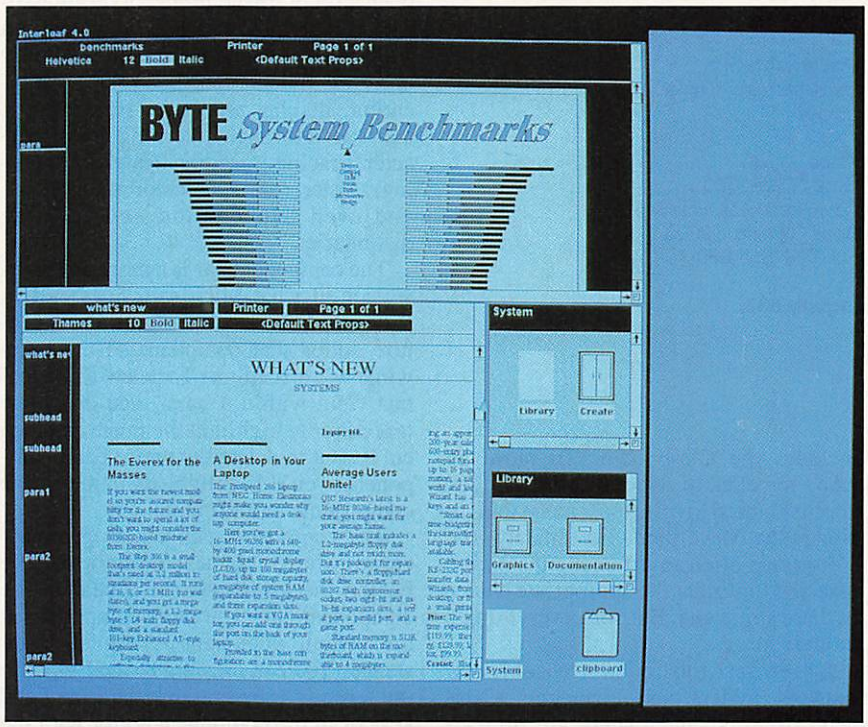
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Jon Udell



Interleaf's Technical Publishing Software lets you easily mix text and graphics in a document.

Interleaf's Technical Publishing Software (TPS) blends two styles of computer-based publishing. The first, represented by troff and TEX, is stream-oriented and works with a global description of a document's format. The second (and newer) style, best exemplified by PageMaker, works in a WYSIWYG mode with individual pages.

Both methods have advantages: troff and TEX powerfully automate the pagination of large documents, and PageMaker shines when you need to lay out custom pages that mix text and graphics. TPS's union of the two styles is, for the most part, a happy one that has made it one of the most interesting desktop publishing packages around. The latest version, release 4.0, enhances both halves of TPS's personality.

Release 4.0, ranging in price from $2500 for the core version to $15,000 for the full version, runs under Unix on Sun, Apollo, and DEC workstations. I used the full version on a Sun386i. That's a heady combination of hardware and software, but there's hope for PC and Mac users.

Interleaf has already ported release 3.0 to PCs and Macs. These versions, known respectively as IBM Interleaf Publisher and Interleaf Publisher, have recently dropped into the sub-$1000 price range.

The advent of DOS extenders with built-in virtual memory (on 80386 PCs) and System 7.0 with virtual memory (on 68030 Macs or on 68020 Macs equipped with paged-memory-management units) might tempt Interleaf to move its latest version over to these platforms. The company isn't making any promises, however.

First Impressions

On the Sun workstation, TPS can run in a SunView window using your choice of Sun or Interleaf conventions for mouse-button behavior, or it can claim the workstation's entire screen (again, with your choice of mouse conventions). I preferred the SunView approach, which let me iconify and de-iconify the TPS application and switch among windows containing other tasks, such as Unix and DOS terminals and SunView's Organizer. That flexibility, however, requires you to think in terms of two different windowing models and two different desktops. Moving or sizing the SunView window that contains TPS (or any other SunView application) works one way. Within the TPS window, moving or sizing the window that contains a TPS document works another way.

Although the mechanics of TPS's desktop differ from those of Sun's, the two share a common philosophy that I find less congenial than the Mac's. Both turn what are simple click or click-and-drag operations on the Mac into menu-driven affairs. For example, to close a TPS document window, you click on the document's name to pop up a menu that

continued

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Documentation
User manuals; tutorial; application guides

Price
Core TPS: $2500
Advanced Graphics: $4500
Book Catalog: $2500
Full TPS: $15,000

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includes the Close item. To move an icon, you click to select it and then click another button to bring up a menu that includes the Move item. Fortunately, the software is often smart enough to anticipate and highlight the appropriate choice in these situations. But still, everything's modal.

Chief desktop icons are cabinets, drawers, folders, and documents. Cabinets, drawers, and folders are directories; their icons differ, so you can metaphorically classify what you store in them, but they behave identically. Documents are where the action is. To create a document, you click in empty desktop space (or in an open cabinet, drawer, or folder) to pop up the menu of actions that are available, select `Create->`, slide right to pop up the submenu signified by the arrow, and select `document`. Such telescoping hierarchical submenus appear everywhere and are one of the hallmarks of Interleaf's interface.

The document window is bounded by Header boxes, a component bar, and horizontal and vertical scroll bars. Each Header box acts as a gateway to menus that control sets of document properties. The Name box's pop-up menu accesses the `Rename`, `Close`, and `Save` commands. The Printer, Font, Page, and Text boxes each govern other sets of properties.

Style, Structure, and Content

You use the vertical, left-aligned component bar to view and edit the components of a document. In the default empty document, there is a single component name: `para`. When you click in the document's main window and start typing in text, the text appears on the screen as 12-point Thames Roman (similar to Times Roman) spaced 1.16 lines apart.

These properties flow from the default `para` component. To change them, you select the component's name in the component bar, activate a pop-up menu, and open a set of linked *property sheets* associated with the component. Here you can specify a `para`'s margins, font family and size, indentation, horizontal justification, display attributes (underlining and strike-through), kerning (intercharacter spacing), leading (interline spacing), color (for spot color separation), and even hyphenation and spelling dictionaries.

The component bar is a more powerful version of what Microsoft Word calls a style sheet. But it also serves as a structure editor that complements the main window's text editor. To delete a range of text from within a `para`, you'd use the text editor to highlight the range and then cut it. But to delete the entire `para` component, you'd highlight its name in the component bar and cut it.

The component editor also gives access to the component masters that lie behind the *instances* that appear in the component bar. The `para` component in the default document is one such instance. You can create a second `para` in the text editor by pressing the Line Feed key, or in the component editor with the `Create->para` command. Now select the new `para` in the component bar, access its property sheet, and change its font. The ensuing pop-up menu prompts you to apply the change locally or globally. The first choice affects only the `para` whose property sheet you've accessed. The second affects all existing `para`s and, because it updates the master that's used to stamp out new instances, all future `para`s as well.

Working with masters takes some getting used to. They're reclusive: You cannot edit them directly; you can only transfer properties to them by way of instances. However, the component bar's `Create->` menu lists all the masters in a document. In addition to `para`, the default document provides masters that govern subheads, lists, bullets, and tables. To add a new master, you create an instance of one of the known masters, adjust its properties to fit your needs, rename it, and globally apply the change. This procedure simultaneously creates a new master and that master's first instance.

Although masters normally transmit style to the instances that derive from them, they can also transmit content. Take a look at one of the pages in the What's New section of this magazine. In the design of a template for that section, I used a shared-content master to define a `firstpara` component that includes the bold divider at the beginning of each article. Once that was done, the `Create->firstpara` command (TPS adds the new component to the `Create` menu on the fly) conjured up a new component that contained the divider. Because all the dividers in the document shared the master's content, a change to any of them—for example, in color, width, thickness, or vertical offset—propagated through the master to all the others.

Text in Graphics in Text

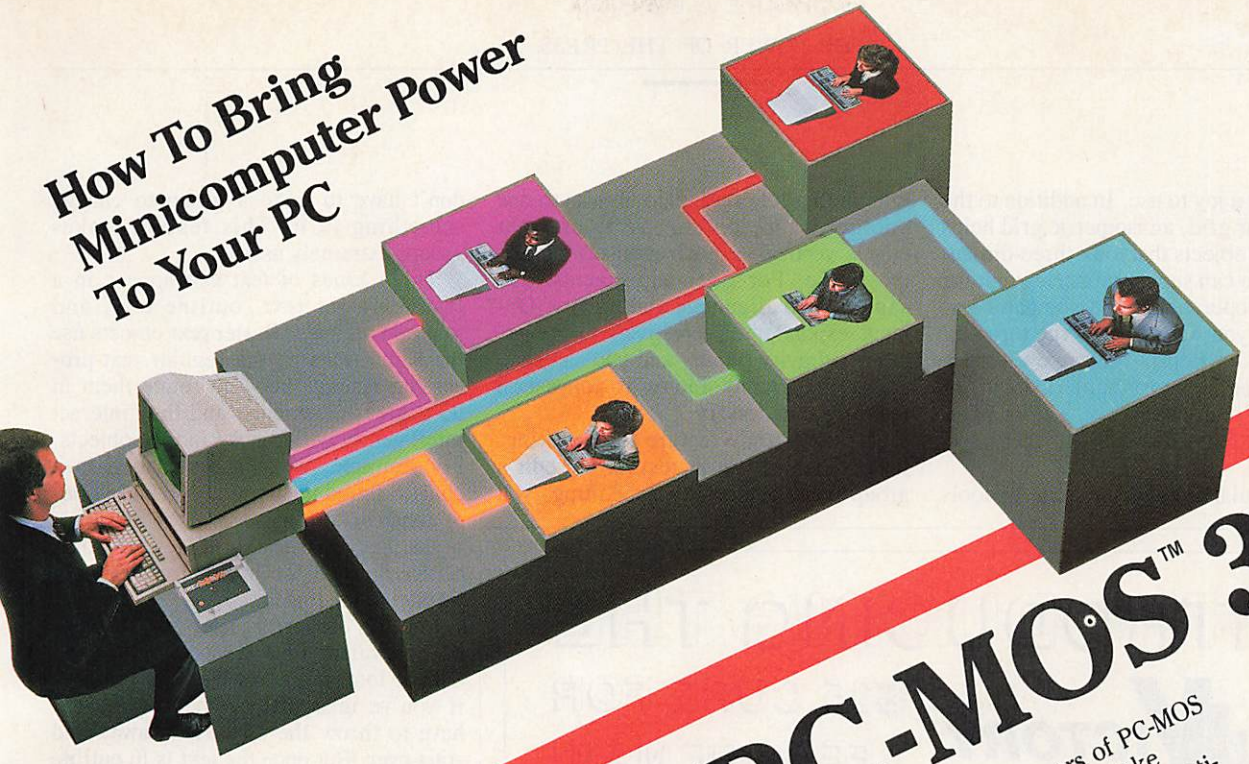
That bold divider was a graphical, not a textual, element. TPS graphics live in *frames* that are, in turn, tied to components. You create frames in the document window, not in the component bar—they're part of the content of components, not components themselves. As such, frames anchor to the text of your document. But, like components, frames have adjustable properties. For example, you can specify that a frame will appear at its anchor's location, after the text in which the anchor occurs, or at the top or the bottom of the anchor's page. Frames can also fill the page, and they can overlay or underlay text and other frames on the page.

Other useful frame properties include width and height, which you can specify in terms of a column of text, a whole page, or absolutely, and offset, which fine-tunes the placement of the frame either horizontally or vertically, depending on the method of anchoring. Like components, frames are instances of masters. Once you adjust one to your liking, you have built a frame master that you can name and reuse.

When you select and open a frame, you enter the diagram editor—a highly sophisticated, object-oriented drawing program. The basics will be familiar to anyone who's used MacDraw or Adobe Illustrator—lines, ovals, boxes, and fill patterns behave much as they do in these popular Macintosh applications. But the power of the TPS diagram editor is simply breathtaking. The arc and spline

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editors are a joy to use. In addition to the rectangular grid, an isometric grid helps you create objects that look three-dimensional. You can supply numeric input for nearly all operations, and you can be as precise as you want (that's true throughout the TPS system). You can even specify a scaling factor for numeric input, so that if you're drawing, say, a floor plan, you can express distances in feet or in inches.

I particularly liked the suite of tools that align a set of selected objects to one another's top, bottom, left, or right edges, vertical or horizontal centers, or the frame. For finer adjustments, you can use grid alignment and gravity. Objects respond quite sensitively to one another's gravity points, and you can even adjust the gravity radius if congestion makes that necessary.

Another handy feature is subediting, which enables you to recursively edit a group of objects. With subediting, you don't have to undo a group to change something in it. This feature makes groups extremely useful.

Three kinds of text can appear in a frame: raster text, outline text, and microdocuments. Raster text objects use the same fonts as the regular text-processing system. You can rotate them in 90-degree increments, and they interact intelligently with other kinds of objects. For example, while adding labels to a chart, I found it easy to lay down a series of construction lines, snap the baselines of the text labels to those lines, and then center the text labels horizontally with respect to the lines.

You can convert a raster text object to its equivalent in a Bitstream-supplied outline font. It's a one-way conversion—if you've misspelled something, you'll have to throw the conversion away and start over. But once the text is in outline form, you can size or rotate it arbitrarily, change the weight of its edges, fill it with a pattern, and twist it into unusual (and, you hope, artistic) shapes.

Microdocuments are TPS documents that live within bounding rectangles inside graphical frames, which, in turn, live inside components of regular TPS documents. Confusing? Well, yes, there are a lot of Chinese boxes here, but microdocuments are an intriguing invention. The problem with raster and outline text objects is that, while they're fine for short phrases and one-liners, you often need more text than that in a diagram, and you'd like that text to behave as text, not as graphical objects. Microdocuments do that. Nearly all TPS's text-processing power is available within the microdocument editor. Microdocuments can even participate in the main document's table of contents and index processing. That makes them a good choice for captions and legends.

Layout Problems

With this formidable collection of tools, I set out to produce templates for a few pages of BYTE. To my surprise, I was unable to solve a layout problem satisfactorily. Look again at the What's New section. See how the columns run around the photograph at the top of the page? In a multicolumn format, TPS doesn't do well with that sort of text/graphics interaction.

Frames work beautifully when they're no wider than a single column; the frame anchors to and flows with the text. When the frame gets wider than a column, there are a couple of possibilities: It can straddle the page (the straddle acts as a

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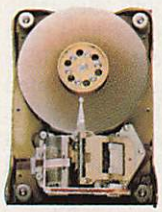
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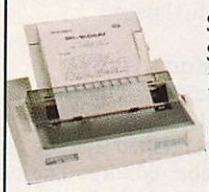
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text-flow barrier), or it can overlay the page (but then the frame won't obstruct text flow).

A text-shaping feature lets you manually push text around an overlay frame, but that's a custom operation and can't be made part of a reusable template. A final option, used in the newsletter example provided with the software, is to put each column's text into a separate microdocument; then it's easy to put the columns where you want them. But again, that's a custom operation that doesn't yield a reusable template. Text can't flow between microdocuments, so in a production environment, you'd be stuck doing lots of electronic paste-up.

I was trying to get TPS to do something it wasn't designed to do. It's not really a layout system, and it's not intended for newspaper and magazine work. The essence of layout is that each page gets special treatment. But TPS's dominant mode is document-oriented rather than page-oriented. True, its diagram editor is so powerful that you can ignore the document mode and create highly customized mixtures of text and graphics within frames. Nevertheless, in document mode TPS's strength is automatic pagination, not custom layout.

Who needs this capability? Technical documenters, business folk, scientists, engineers, commercial book publishers, database publishers—anyone who produces lots of pages, needs high quality and fast turnaround, wants to define and reuse design standards, and doesn't want to fuss over each individual page.

Charts, Tables, and Equations

TPS supports its diverse users with several additional special-purpose tools. Three that I haven't mentioned are the equation, chart, and table editors. The equation editor does mathematical typesetting. It parses expressions made of letters, digits, parentheses, brackets, and mathematical keywords, and it produces typeset equations.

The chart editor is the nicest that I've worked with. It's data-driven—you cut tab- and new-line-delimited sets of numbers from a text file and paste them into a chart's data sheet. The system supports the usual collection of chart styles but offers excellent control over variation within those styles. Using data on 66 machines that have been tested in the BYTE Lab, I developed a stacked-bar chart that displayed nearly 600 data points. The result was clear and precise on-screen and even better when printed on a LaserWriter IINT.

TPS's attention to detail is such that you can set the width and length of the hash marks along a chart's axes (among other chart properties) in terms of whimsically named rsus (for "ridiculously small units"). An rsu is equal to a millionth of an inch. The manual notes dryly that you have to add 3000 rsus to a chart parameter to see even a slight difference in 300-dot-per-inch printed output.

Charts inhabit frames, so it's easy to add further embellishments using the diagram editor. You can move and size charts and lay pictures or microdocuments on top of them. I even found a way to mimic the BYTE format for benchmarks. Sometimes application benchmarks are shown as left-to-right bars and system benchmarks as mirror-image right-to-left bars on the same page. The diagram editor couldn't flip the system benchmarks to the other orientation, but TPS's screen-capture tool turned the chart into a raster image, which I then flipped and aligned to achieve the desired result.

Tables are interesting hybrids. When you create a table in the component bar, you specify the number of rows and columns that it contains. The result isn't a single component name, however, but rather a list of names—one for each row. From any row component, you can access property sheets that govern that row instance, the row master (and, by extension, all rows), or the whole table. When you click in a cell, you can access property sheets that govern that cell, and you can apply changes to only that cell or to its whole column. Text wraps within cells, and a row grows automatically when the contents of any of its cells require it to do so.

Document and Project Management

TPS recognizes that the kinds of documents it does well usually represent the work of a team rather than an individual author, and it works hard to support the team approach. The *book* is a meta-document implemented as a special directory that joins into a single entity a collection of documents that may have been produced by multiple authors on multiple workstations. The book's documents retain their individuality, but they can also behave as an aggregate for purposes of pagination, indexing, and printing. A *catalog* is to a book what a component bar is to a document. Catalogs can export properties to the documents in a book; that's a useful way to control the style of a collection of documents.

A set of what Interleaf calls "effectivity tools" aids in the control of versions, revisions, and annotations. The mechanism entails tagging components with attributes and then applying control expressions to select components that match one or more attributes. For example, if you have to maintain a software manual for a product that runs under multiple operating systems, you might use the attributes "Unix" or "VMS" to mark the variable parts of the book. Or, if several editors are reviewing a document, you might use the attributes "Frank" and "Sylvia" to selectively show or hide their comments.

Not everyone on a writing team needs a TPS workstation. The system happily imports ASCII files that intersperse component names (e.g., <para>) with textual content. That's an important point to bear in mind. For example, a single TPS workstation run by a competent artist/typesetter might be adequate to serve a team of PC-based technical writers.

Toward an Open Architecture

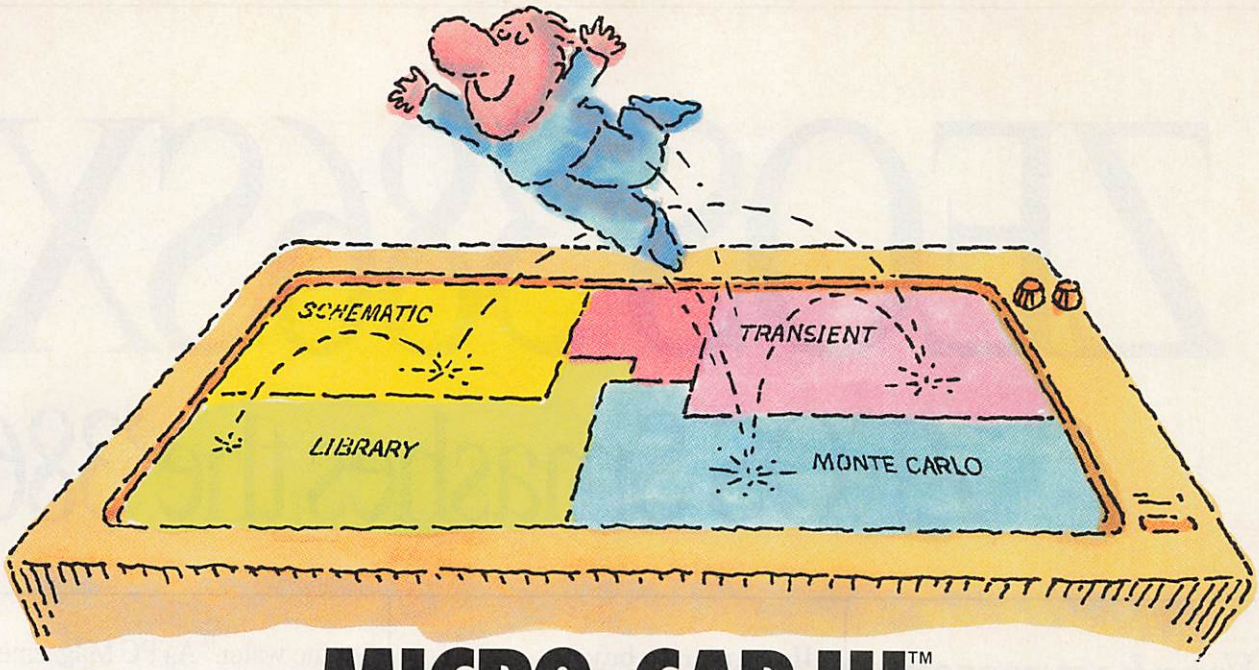
TPS 4.0 takes a small step in the direction of what the company calls an "open architecture": A Lisp interpreter is embedded in the system, and a small set of Lisp programs comes with the installation. The names of these programs appear on the Custom pop-up menu; icons in the Custom cabinet contain the Lisp code.

These "Leafware" utilities can run Unix commands from within the TPS desktop or set TPS system parameters. It's an embryonic capability, but one that holds much promise.

Building extensibility into TPS—as most CAD vendors have done with their products—invites third-party developers to customize the product for more specialized markets than Interleaf itself can address. It's a great idea, although it's not yet clear that Leafware will open up the TPS product to the extent that AutoLisp has opened up AutoCAD.

TPS 4.0 is a remarkable product. From a PC or Mac perspective, it's like having TEX, PageMaker, Adobe Illustrator, and Microsoft Chart all rolled into a single package. There's so much there, I'll bet many users will tap only a fraction of its capacity. But for those who deal heavily in the kinds of documents that TPS does well—from display advertisements to textbooks—TPS 4.0 will get the job done with speed, style, and precision. ■

Jon Udell is a BYTE senior technical editor at large. He can be reached on BIX as "judell."

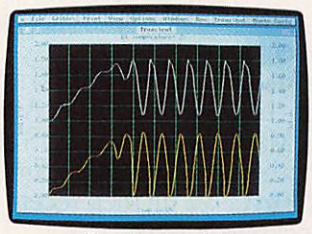


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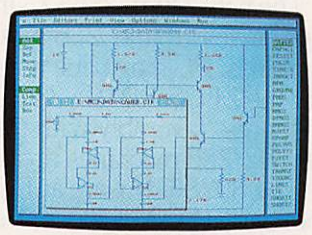
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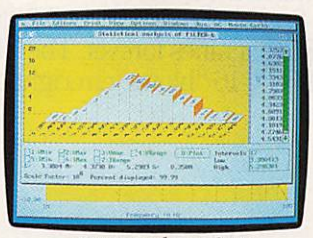
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PC Magazine, May 30, 1989

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Performance Comparisons using PC Labs Benchmark Series Release 4:

	80386 Instruction Mix	Floating Point Calculation	Conventional Memory
ZEOS 386/16 Desktop	3.58	13.62	0.58
ZEOS 386/20 Desktop	2.87	10.82	0.38
IBM PS/2 Model 70-E61	4.08	16.04	0.75
Compaq Deskpro 386/16	4.12	15.47	0.75

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PC Magazine, On "What Makes an Editor's Choice"

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Performance Comparisons using PC Labs Benchmark Series Release 4:

	80386 Instruction Mix	Floating Point Calculation	Conventional Memory
ZEOS 386/25 Desktop	2.29	8.37	0.33
ZEOS 386/33 Desktop	1.67	6.43	0.27
IBM PS/2 Model A	2.27	8.33	0.60
Compaq Deskpro 386/25	2.36	8.59	0.37

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	80286 Instruction Mix	Floating Point Calculation	Conventional Memory
ZEOS 286/12 Desktop	4.78	18.84	0.72
IBM PC AT (8MHz)	8.96	35.60	1.32
IBM PS/2 Model 50	7.20	28.34	1.05

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Performance Comparisons using PC Labs Benchmark Series Release 4:

	80386 Instruction Mix	Floating Point Calculation	Conventional Memory
ZEOS 386/20 Desktop	2.87	10.40	0.39
IBM PS/2 Model 70-121	3.24	12.72	0.61
Compaq Deskpro 386/20e	2.91	10.54	0.40

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Present Address _____ (Street Apt. # City State Zip)

Social Security Number _____ ( ) _____ (Home Phone)

Date of Residence _____ (Month Year) Monthly Payment $_____ ☐ Buy ☐ Rent ☐ Other

Previous Address _____

_____ Dates of Residence _____ (From To)

Your Employer _____
(If self-employed, see rear panel.)

Date of Employment _____ (Mo. Yr.) Position _____

Monthly Income _____ (Gross $ Net $)

Employer's Address _____ (Street)

_____ ( ) _____ (City State Zip Business Phone)

Previous Employer _____ Address _____

_____ Dates of Employment _____ (From To)

Other Income _____ I have received since (Date)_____
Income from alimony, child support or separate maintenance payments need not be disclosed if you do not wish to have it considered as a basis for repaying this obligation.

Monthly Income _____ (Gross $ Net $)

Name and Address of Nearest Relative Not Living With You _____

_____ Relationship _____

b. Credit Information

Include joint information, if joint account requested.

Bank Account _____ (Bank Name) ☐ Checking ☐ Savings

Address _____

Bank Account _____ (Bank Name) ☐ Checking ☐ Savings

Address _____

Bank Loan Reference _____ (Bank Name Address)

_____ Payment _____ Balance _____

Bank Card Reference _____ (Bank Name Address)

_____ ☐ VISA ☐ Mastercard Payment _____ Balance _____

(please check appropriate box):

☐ **Joint Credit** with another person. Complete all information.
☐ **Individual Credit** but rely on income or assets of another person as a basis for repaying the credit requested. Complete all information
☐ **Individual Credit** Complete sections "a" and "b" only.

Please complete all appropriate sections, *providing at least two years' residence and employment history.* This will enable your information to be processed as quickly as possible. If you are self-employed, please be sure to complete section "d" below.

Other Credit Card Reference _____ (Bank Name Address)

_____ Payment _____ Balance _____

Other Credit References _____ Payment _____ Balance _____

Account No. _____ Expires _____

Driver's License No. _____ State _____ Expires _____

c. Joint Personal Information

Joint Name _____ (First Initial Last)

Date of Birth _____ (Mo. Day Yr.) Social Security Number _____

Address _____ (Street Apt. #)

_____ (City State Zip)

Date of Residence _____ (Mo. Yr.) Home Phone ( ) _____

Employer _____

Date of Employment _____ (Mo. Yr.) Position _____

Monthly Income _____ (Gross $ Net $)

Employer's Address _____ (Street)

_____ ( ) _____ (City State Zip Business Phone)

d. Self-Employed Information

Complete this section only if you are self employed.

Business Name _____

Business Address _____

☐ Proprietorship ☐ Corporation ☐ Partnership Business Phone ( ) _____

Description of Business _____

Your Position _____ In Business Since _____

Your annual income from business _____ Business' annual income _____ (gross) (net)

You must provide at least one of the following:

1. Business Bank _____

( ) _____ (Telephone) _____ (Personal Banker's Name)

2. Accountant's Name _____

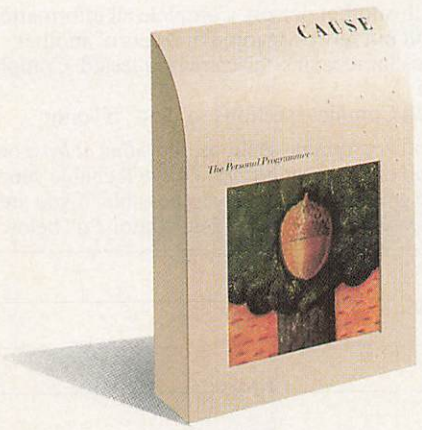
( ) _____ (Telephone)

3. Financial statement on business attached.

(EXC. AK, & HI)

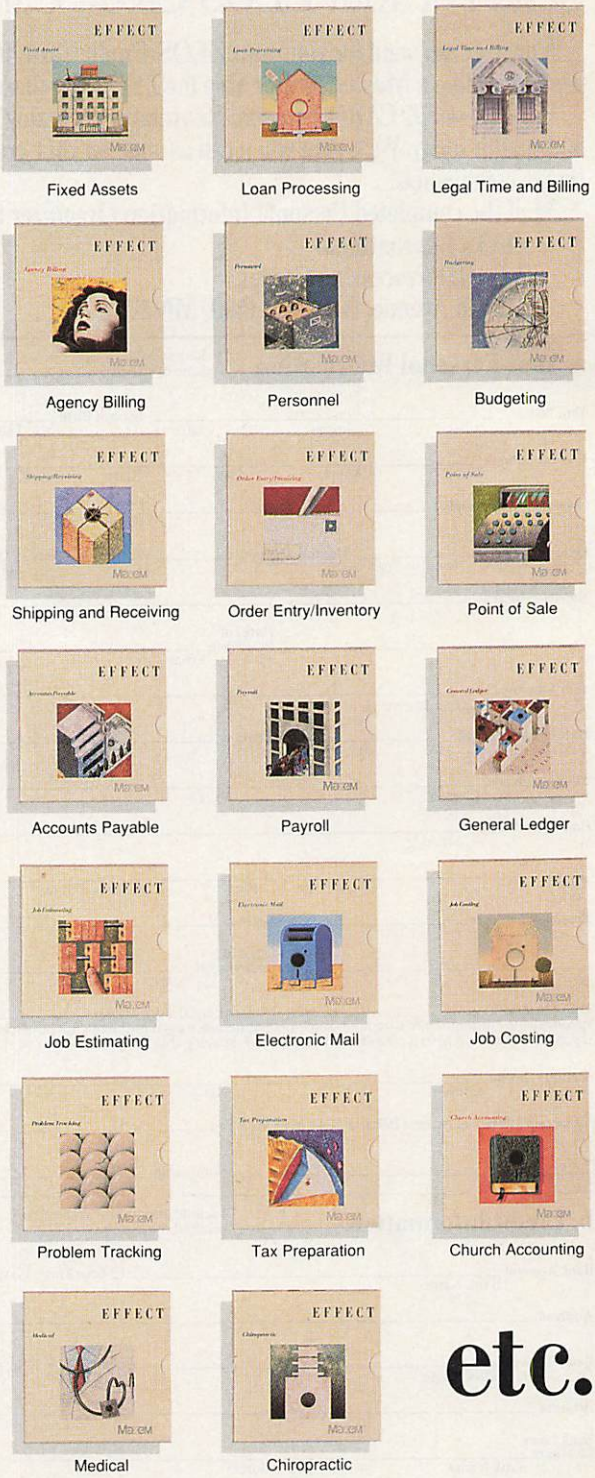
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Reviewer's Notebook

Reviewer's Notebook is a compilation of brief reviews and updates to previously published evaluations. BYTE will publish Reviewer's Notebook each month on a space-permitting basis.

Lab Report: Three Singular Systems

Of the slew of systems that the BYTE Lab benchmarked this past month, we found three worthy of note: the AST Premium/386C, the Swan 386SX, and the Wedge Turbo 286.

We've come to expect quality from AST, and the **Premium/386C** doesn't disappoint us. The system features a 20-MHz 80386, switchable to 8 or 4.77 MHz, plus an efficient memory architecture, an AST trademark. A proprietary interface board supports up to 16 megabytes of dedicated 32-bit memory. Four banks of sockets for single in-line memory modules on the board can support four 256K-byte or 1-megabyte SIMMs each. It also delivers the cache: 64K bytes of 25-nanosecond static RAM.

Our unit came with a 90-megabyte hard disk drive. The floppy disk drive controller supports up to three floppy disk drives. A 1.2-megabyte 5¼-inch floppy disk drive is standard. One parallel and two serial ports are built into the system board, saving an expansion slot. The system sports a total of four 16-bit and two 8-bit slots, with two 16-bit and two 8-bit slots free. Two slots are occupied by the floppy disk drive controller and the 16-bit AST VGA Plus card that was shipped with the unit we received.

The AST expansion slots can take advantage of an extended bus architecture. The extra pins allow intelligent peripherals to share control of the system bus to relieve some of the processing load from the main CPU.

The system's benchmark results (see table 1) place it in the upper tier of 20-MHz machines. Although it falls behind the Dell System 310, the ALR FlexCache, and the Compaq Deskpro, it leads most of the 20-MHz pack with a CPU index of 3.26 and an overall application index of 16.14.

The quality of the Premium/386C shows in its sturdy construction and the system documentation. AST's comprehensive manual comes complete with glossary, index, and technical appendixes. It even covers software utilities bundled with the system. These utilities include disk caching, memory management, print spooling, low-level disk formatting, and system setup.

But quality doesn't come cheap. The Premium/386C's basic configuration (without a hard disk drive or monitor) costs $4395. Add $800 for a 40-megabyte drive and controller, or $1750 for a 90-megabyte ESDI drive and controller.

If you're searching for a 32-bit hybrid at 16-bit prices, the **Swan 386SX** is worth a look. At $1399, its price competes with that of most 80286s, while its performance matches that of many 16-MHz 80386 machines.

Like most SX vendors, Swan Technologies optimized space inside the Swan box. The 40-megabyte hard disk drive, mounted vertically, attaches to the standard drive bays. This leaves two half-height bays free beneath the 1.2-megabyte 5¼-inch floppy disk drive. A 16-bit Adaptec modified frequency modulation disk drive controller card with 1-to-1 interleave manages the drives.

The extra space means that the Swan is ready for future enhancements. In addition to the extra drive bays, the unit provides two 8-bit and six 16-bit expansion slots. Our unit had both 8-bit slots filled with an I/O controller and an 8-bit VGA card. The disk drive controller occupied one of the 16-bit slots. That still leaves plenty of room for expansion cards.

The motherboard uses SIMM architecture for memory upgrades. Our unit came with 1 megabyte of 100-ns RAM.

continued

Table 1: *The AST Premium/386C's CPU and application indexes place it among the fastest of the 20-MHz 80386s. The Swan 386SX posted respectable benchmarks for a machine base-priced at $1399. The Wedge Turbo 286's CPU index was well below that of comparable 20-MHz machines.*

BENCHMARK RESULTS

	Low-level indexes				Application-level indexes					
	CPU	FPU	Disk I/O	Video	Word processing	Spreadsheet	Database	Scientific/ engineering	Compilers	Cumulative
AST Premium/386C	3.26	7.42	2.31	2.28	3.12	2.60	2.61	4.50	3.31	16.14
Swan 386SX	1.90	3.06	2.07	1.23	2.25	2.23	2.01	2.38	2.14	11.02
Wedge Turbo 286	1.58	1.60	1.40	1.07	1.92	2.02	1.40	1.82	1.62	8.78

For a full description of all the benchmarks, see "Introducing the BYTE Benchmarks," June 1988 BYTE.

Tucked beneath the vertical drive bay, the SIMM modules are hard to get at even after you remove the hard disk drive. As with many 80386SX models, no memory caching is available. The Swan 386SX uses the Chips & Technologies NEAT (for New Enhanced AT) CHIPSet for bus, memory, and peripheral control.

Benchmark results (see table 1) place the Swan 386SX in the middle of the SX pack, behind the Compaq 386s and ahead of the IBM PS/2 Model 55 SX. But its price undercuts that of any 80386SX machine we've seen yet. A Swan 386SX with VGA and a 32-megabyte hard disk drive sells for $2298. A 40-megabyte model goes for $2498. Utilities, including Disk Manager for formatting your disk, and a well-structured (though unindexed) manual come with the package.

Competing with the new 80386SX machines is a flock of souped-up 80286-based systems. The **Wedge Turbo 286** employs a 20-MHz Harris 80C286 processor running at 24 MHz. Unfortunately, the Turbo 286 does not deliver a performance advantage.

It's hard to figure out why this machine is so lackluster (see table 1). We might blame the 10-MHz FPU for the poor cumulative application index (8.78) that places the system below every other 20-MHz machine we've tested; that hurt it in the scientific/engineering applications. And the generic disk drive controller limits disk-intensive applications.

But neither of these factors accounts for the CPU index of 1.58, well below that of other 20-MHz 80286s such as the Wells American 286/20 (2.74) and the Dell System 220 (2.72). We tried changing the CPU speed by the CMOS setup, by hot-key switching, and by software utilities. Nothing provided the extra boost. We could switch speeds between slow and fast, but the fast setting just wasn't fast enough.

The Wedge comes standard with 1 megabyte of memory (expandable to 8 megabytes), a 1.2-megabyte 5¼-inch floppy disk drive, a 40-megabyte hard disk drive, an NEC MultiSync GS monitor, a 101-key Enhanced keyboard, and DOS 4.01. The system also offers three 8-bit and five 16-bit slots for future expansion. The disk drive controller takes up a 16-bit slot, and the VGA card occupies an 8-bit slot. Another 8-bit card delivers a parallel port and a 9-pin serial port, as well as an additional 25-pin serial port and a game port accessible from rear-panel cutouts. Component manufacturers have provided documentation.

Presumably, the Wedge Turbo 286 is designed to counter the 80386SX onslaught with greater performance at a cheaper price, but at $2595, a fully configured Turbo 286 is nearly the price of the Swan 386SX. The Wedge we reviewed didn't deliver the goods.

—Stanford Diehl

AST Premium/386C
AST Research, Inc.
2121 Alton Ave.
Irvine, CA 92714
(714) 863-1333
$6540 as reviewed
Inquiry 856.

Swan 386SX
Swan Technologies
A division of Tussey Computer Products
3075 Research Dr.
State College, PA 16801
$2795 as reviewed
Inquiry 857.

Wedge Turbo 286
Wedge Technology, Inc.
1587 McCandless Dr.
Milpitas, CA 95035
(408) 263-9888
$2480 as reviewed
Inquiry 858.

400-dpi Printer Shines in Graphics

What can an extra 100-dot-per-inch resolution from your laser printer do for you? Plenty, if you use complex graphics or scanned images in your work. For this reason, 400-dpi laser printers have sprung up like mushrooms after a rainstorm. One of the latest offerings comes from Genicom, whose 6100 Series laser printers offer a wealth of features without resorting to PostScript.

An 8-page-per-minute Canon LPB-SX laser engine drives the unit, which has both a Centronics parallel port and connector, and an RS-232C serial port using a DB-25 connector. The printer supports IBM Graphics Printer, Diablo 630, Hewlett-Packard LaserJet Series II, and HP 7475A plotter emulation modes. It comes with 15 ROM-resident outline fonts supplied by URW, a German typeface foundry.

The $4295 Model 6140 comes with 1 megabyte of RAM; the $4995 Model 6142, which I looked at, comes with 3 megabytes. A $699 plug-in card supplies



An 8-page-per-minute Canon engine drives the Genicom 6142 laser printer.

22 additional font outlines.

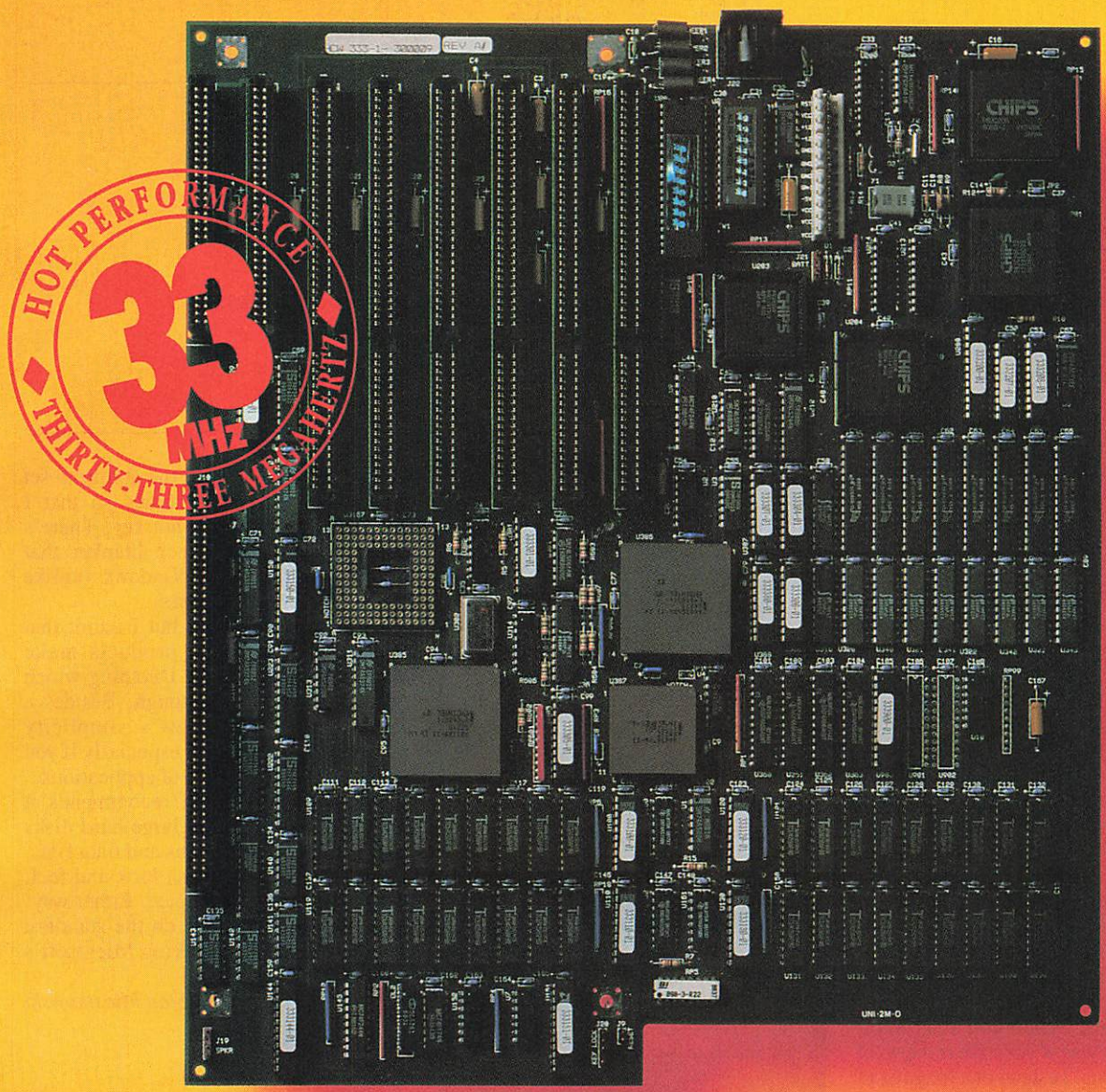
The printer uses the ASCII Coded Escapement page description language working with an ACE driver on the computer. Like PostScript, ACE is device-independent, but it relies on concise operators (many are only two characters long) to describe the page. The company supplies drivers for Windows 1.04, 2.01, and 2.03; AutoCAD 2.62 releases 9 and 10; GEM 3.0; Ventura Publisher 1.0 and 1.1; and Microsoft Word 3.x and 4.0.

Using a 33-MHz PC Link 386 running Windows 286 version 2.1, I printed from many Windows applications. A three-column Aldus PageMaker 3.0 document using many fonts and a simple graphic printed in 40 seconds. A Micrografx Designer 2.0 drawing of a silhouetted image printed in a minute.

My version of AutoCAD (2.52) was incompatible with the Genicom driver, but I configured AutoCAD to use the ADI plotter driver, set the printer to HP 7475A plotter mode, and coaxed plots out of AutoCAD. I even got plots with fill patterns out of MacDraw 1.1 on a Mac II by configuring the MacPlot plotter driver for a Hewlett-Packard plotter.

I scanned in several images on an HP ScanJet scanner using Hewlett-Packard's Scanning Gallery software at 300 and 400 dpi. I saved these images as TIFF files and imported the images into PageMaker. The quality of the printed 400-dpi images looked worlds better than the 300-dpi images. However, because 400-dpi images contain more information, I couldn't print out either a full-page scan

continued



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Trademarks: IBM PC, XT, AT, PS2 and OS/2: IBM. Intel 386: Intel Corp.; Windows/386: Microsoft Corp. DESQview: Quarterdeck

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or a complex graphic with shading unless the printer had 3 megabytes of RAM.

Since this printer costs as much as a decent PostScript printer, you must first decide if the extra resolution is worthwhile. If you're printing newsletters that have only text, the answer is no—the additional detail is hardly noticeable. But if you're working with scanned images, it certainly will make a difference.

Budget yourself for the Model 6142 with the extra memory. As long as Genicom supplies printer drivers for popular applications (an OS/2 driver would be nice), lack of PostScript compatibility shouldn't be an issue. —*Tom Thompson*

Genicom Model 6142
Genicom Corp.
One Genicom Dr.
Waynesboro, VA 22980
(800) 443-6426
$4995
Inquiry 865.

Windows Made Clearer

Microsoft Windows, like all graphical user interfaces, is an acquired taste. GUI or no, it forces you to contend with plenty of pull-down text windows, and you still need to know what filenames start what applications.

Now several products are attempting to take the pain out of using Windows. I looked at two of them: ClearView from Wang Laboratories and PubTech File Organizer (PFO) from Publishing Technologies. Both replace Windows' MS-DOS Executive.

At $79, Wang's ClearView is the less expensive of the two. It marks the company's first move into mass-market software. The name "ClearView" pretty much says it all. When you start Windows, it gives you a *very* clear view of your applications. Instead of a long list of filenames, ClearView puts Macintosh-like icons on the screen—and little else.

You can, of course, add icons for your own applications, using a choice of standard icons. ClearView's Windows Organizer let me set up custom menus using both icons and (optionally) text. You can also customize the placement and sizing of the windows that appear when you start applications. Since I almost always use my editor when I first start Windows, I set up a custom start-up file that immediately opens the editor in one window while displaying additional application choices in another.

PFO outperforms ClearView, but at $199.95, it's also considerably more expensive. PFO's opening screen looks strikingly similar to a Macintosh Desktop. It has icons for applications and disk drives, folders for files and subdirectories, and even a "garbage can."

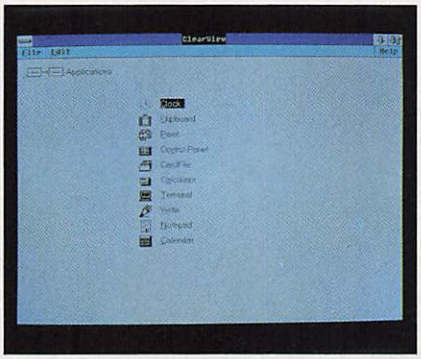
The Macintosh analogy doesn't stop there. When you click on a text file icon, the document automatically opens in PFO's own text editor, a fuller version than Windows' limited editor. You can also click on and drag icons across the screen to copy, move, or delete individual files or groups of files. If you want to print a text file, you just drag the file icon to the printer icon.

Like ClearView, PFO lets you customize window size and placement and set up multiple standard application configurations. I especially liked the ability to set up my common applications so that I could call them with a hot key. There's even an automatic screen blanker that actually works with Windows (unlike most commercial blankers).

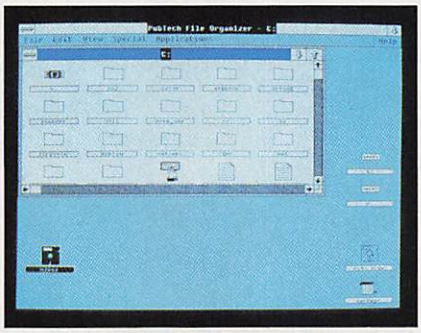
I'm not an icon fan, but I admit that these two icon-based products make Windows easier to use. Deciding which one's for you will be tough. Besides a lower price, ClearView's simplicity makes it easier to learn, especially if you work with only a couple of applications.

PFO's sophistication recommends it for those working with large hard disks chock-full of applications and data files. If you like the Macintosh look and feel, PFO's definitely the choice. Either way, these products improve on the standard Windows interface, making Microsoft's GUI truly easier to use.

—*Stan Miastkowski*



At $79, Wang's ClearView is an inexpensive Windows enhancement.



PubTech File Organizer mimics a Macintosh Desktop.

ClearView
Wang Laboratories, Inc.
One Industrial Ave.
Lowell, MA 01851
(508) 459-5000
$79
Inquiry 859.

PubTech File Organizer
Publishing Technologies, Inc.
7719 Wood Hollow Dr., Suite 260
Austin, TX 78731
(512) 346-2835
$199.95
Inquiry 860.

PowerMouse Courts 1-2-3 Users

The PowerMouse 100 from ProHance combines a mouse and a programmable keypad to make editing Lotus 1-2-3 spreadsheets a snap. Just don't throw away your conventional mouse if you also run graphics programs.

This slick-looking critter plugs directly into a serial port. Its 40 labeled keys can be programmed with one or more combinations of keystrokes and mouse movements. The mouse ships with a 9- to 25-pin adapter, a program disk, a user's manual, and instructions for 1-2-3 use.

At first, the mouse's size and array of buttons made it awkward to handle. But the more I used it, the faster my fingers found the right buttons.

continued

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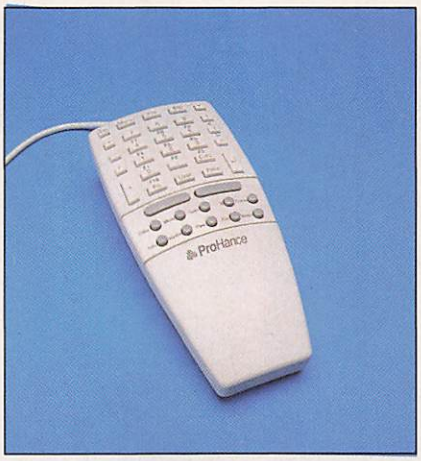
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Installation is quick: You plug in the mouse and run the install program, and you're ready for a spreadsheet. The PowerMouse works beautifully in Lotus 1-2-3, allowing you to move around easily within a large spreadsheet. It takes time to learn how to enter numbers. I'd choose the keyboard over the PowerMouse when keying in lots of digits.

PowerMouse shines once the information is in the spreadsheet. Clicking one button allows you to move and copy data, insert rows or columns, and set up and move between windows. You can do `@SUM(.)` functions by clicking and dragging the mouse. The Fn key plus 1 through 0 emulates the F1 through F10 keyboard commands. All the preprogrammed keys are stored on a disk in files called *key definition tables.*

ProHance software allows you to edit the tables while you're in 1-2-3 or with the vendor's off-line editor. This lets you personalize existing table files or create new tables for other programs. PowerMouse worked with all the text-based non-mouse-driven software that I tried.



PowerMouse's programmable keys play into the hands of spreadsheet users.

Once you create a table, PowerMouse can work its magic.

However, the software drivers are the mouse's downfall. The software version that I tested worked only with non-mouse-driven software. When you move the mouse up, down, left, or right, the software generates keyboard cursor keys. Although this works well with 1-2-3 and other nonmouse software, the product just isn't usable with graphics software. The absence of a Microsoft-compatible mouse driver is a conspicuous omission.

ProHance says that it is integrating Microsoft compatibility with programmable drivers and plans to provide free updates to registered users when the software becomes available later this year.

Overall, PowerMouse worked like a champ with 1-2-3 and my other text-based software. But $195 is a lot to spend for a mouse that can't do graphics. Lotus users, however, will probably think the price is right. —*Michael Wiggins*

PowerMouse 100
ProHance Technologies, Inc.
1307 South Mary Ave., Suite 104
Sunnyvale, CA 94087
(408) 746-0950
$195
Inquiry 861.

QuickC Smooths QuickAssembler Programming

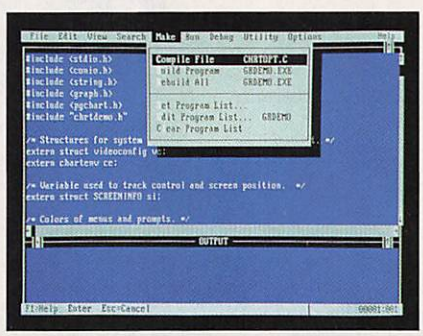
Now that Microsoft is bundling QuickC with The QuickAssembler, programmers can write, debug, and execute assembly language programs within the comfort of a Windows-like interface. When more speed is needed in a C language program, developers can write assembly code in a separate module called from the C program. Also, QuickC's online help system, the Quick Advisor, has been enhanced to allow the inclusion of QuickAssembler instructions, directives, operators, and MS-DOS and IBM PC ROM BIOS services. C language programmers still have access to help on the C run-time library functions.

Microsoft also boosted the environment's debugging capabilities by adding support for viewing registers and the numeric processor's status. Unfortunately, you can't mix C language source code and assembly language displays. Users needing this feature will have to rely on Microsoft CodeView. Also, the debugger supports only C language syntax for expressions. This is inconvenient because users must enter all hexadecimal values in the debugger with a leading 0x.

The QuickAssembler supports the full syntax of the latest version of Microsoft Macro Assembler, as well as a few enhancements. The QuickAssembler .STARTUP directive, for example, now automates the process of setting up the DS, SS, and SP registers during initialization of assembly language programs.

Microsoft now includes a history-oriented debugger that creates a script of actions during program execution and a program "builder" utility. Both of these tools fit seamlessly into the environment.

A setup program typical to most Microsoft products installs the package. I ran into some snags, however. The README file in my copy claimed that the segmented-executable linker could be used with the QuickC environment. But this linker version spilled text onto the QuickC windowed display and didn't complete the LINK process. README also claimed that the libraries installed by QuickC could safely replace the standard Microsoft C Compiler's libraries. This caused problems when I tried to use these libraries with the standard compiler to recompile a Windows application. A barrage of "unreferenced externals" messages appeared.



QuickC gives programmers a Windows-like interface.

The environment works at speeds equivalent to those of previous releases of QuickC, which is disappointing to users who expected QuickC and QuickAssembler to rival the speed of Borland's Turbo environment. For others, the Quick Advisor more than makes up for this loss. Nevertheless, cautious buyers may want to wait for the next release or two when the compile speeds should more closely resemble Borland's. ■

—*Michael Blaszczak*

The QuickAssembler with QuickC
Microsoft Corp.
16011 Northeast 36th Way
P.O. Box 97017
Redmond, WA 98073
(206) 882-8080
$199
Inquiry 862.



Intel 80386SX

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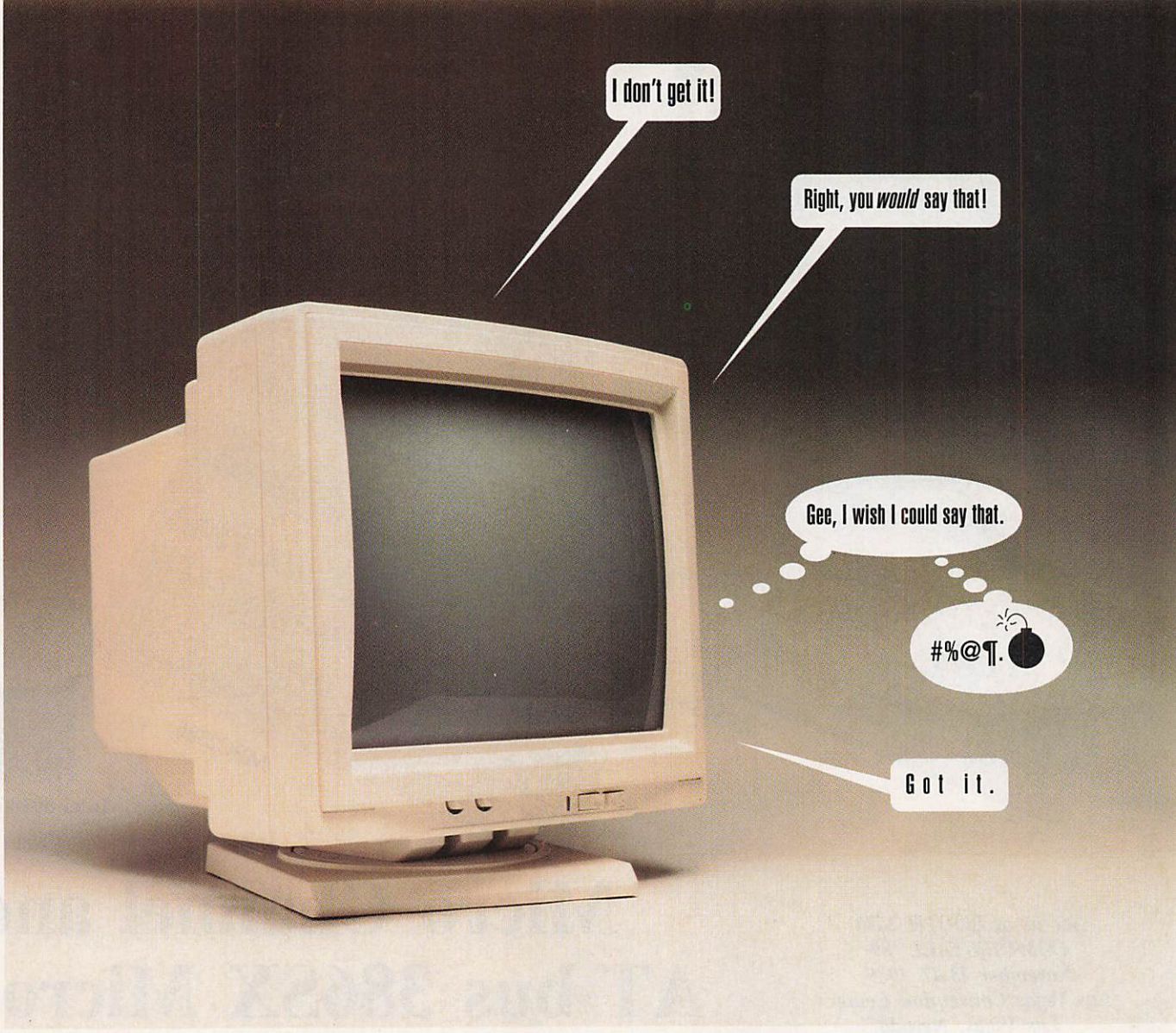
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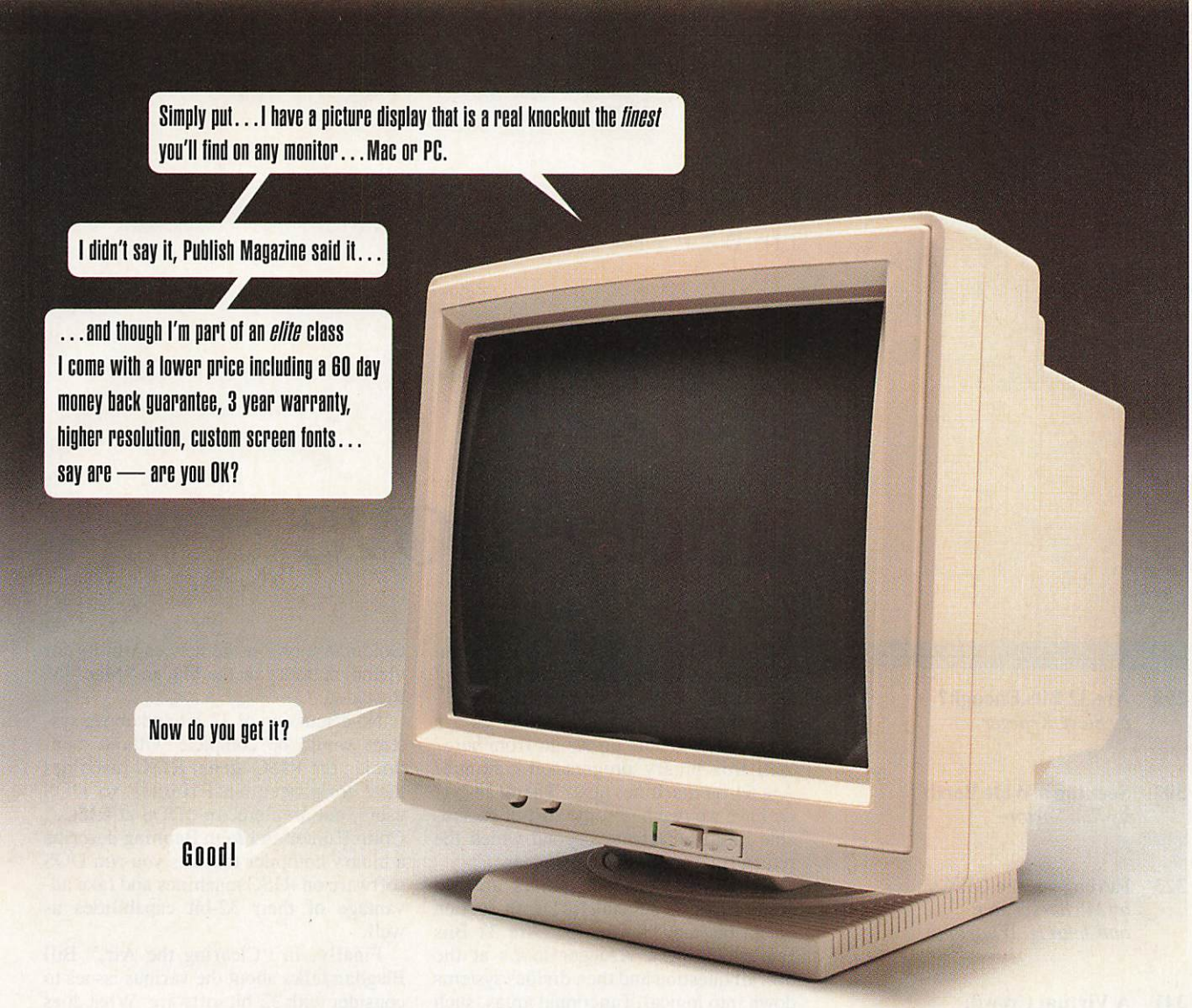
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32 Bits and Above

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376 **Upward Mobility**

In the last 15 years, the microcomputer industry has moved from 8-bit machines to 16-bit machines to 32-bit machines, and a lot of us are wondering: Where do we go from here? Will this binary progression continue? Are 64-bit machines next? Then 128-bit? Or have we reached some sort of reasonable limit, a plateau, beyond which the return isn't worth the investment?

These questions and others are answered in this special In Depth section on 32 bits and above. In "Are 32 Bits Enough?" Steve Krueger looks at the overall question and then divides systems down into logical, functional areas, such as buses, memories, instructions, and addresses, and discusses the pros and cons of raising the width of each.

When it comes to memory interfaces, wouldn't logic say that wider is always better? But it isn't. In "Seeking a Wide Berth," Ron Sartore tells you when and why it isn't and discusses 32-bit memory architectures in detail.

It would be hard to discuss 32-bit hardware without exploring the latest offerings from Intel and Motorola. In "Revenge of the CISCs," Michael Slater and John H. Wharton provide a definitive examination of Intel's 80486. They also look at Motorola's 68040 in as much detail as was available at press time.

One element that 32-bit systems seem to share is an increased capability for virtual memory. In a special series article, "A Virtual Crowd," BYTE explores virtual memory on DOS, OS/2, Macintosh, and Unix systems. In "Virtual Memory: The Next Generation," Robert Moote describes in detail the demand-paging virtual-memory capabilities of Intel's 80386 and 80486 processors. In associated text boxes, Julie Anderson examines "VM Under OS/2" while Ben Smith looks at "VM in Unix." And then Phil Goldman looks at the new capability for virtual memory on the Mac in "Mac VM Revealed."

No discussion of 32-bit and above systems would be complete without mentioning the RISC arena. RISC machines have long been "off limits" to DOS users, but no more. In "DOS at RISC," Colin Hunter and John Banning describe a binary compiler that lets you run DOS software on RISC machines and take advantage of their 32-bit capabilities as well.

Finally, in "Clearing the Air," Bill Blagdan talks about the various issues to consider with 32-bit software. What does it buy you? How well does it use the capabilities of the 32-bit hardware? Should you consider DOS extenders? In other words, what do the words "32-bit software" mean to you?

The future may well look to 64 bits or beyond, but for many of us, the investment involved in a 32-bit system is as much as we can even think about. For now, getting the most out of 32 bits offers challenge enough.

—Jane Morrill Tazelaar
Senior Technical Editor, In Depth

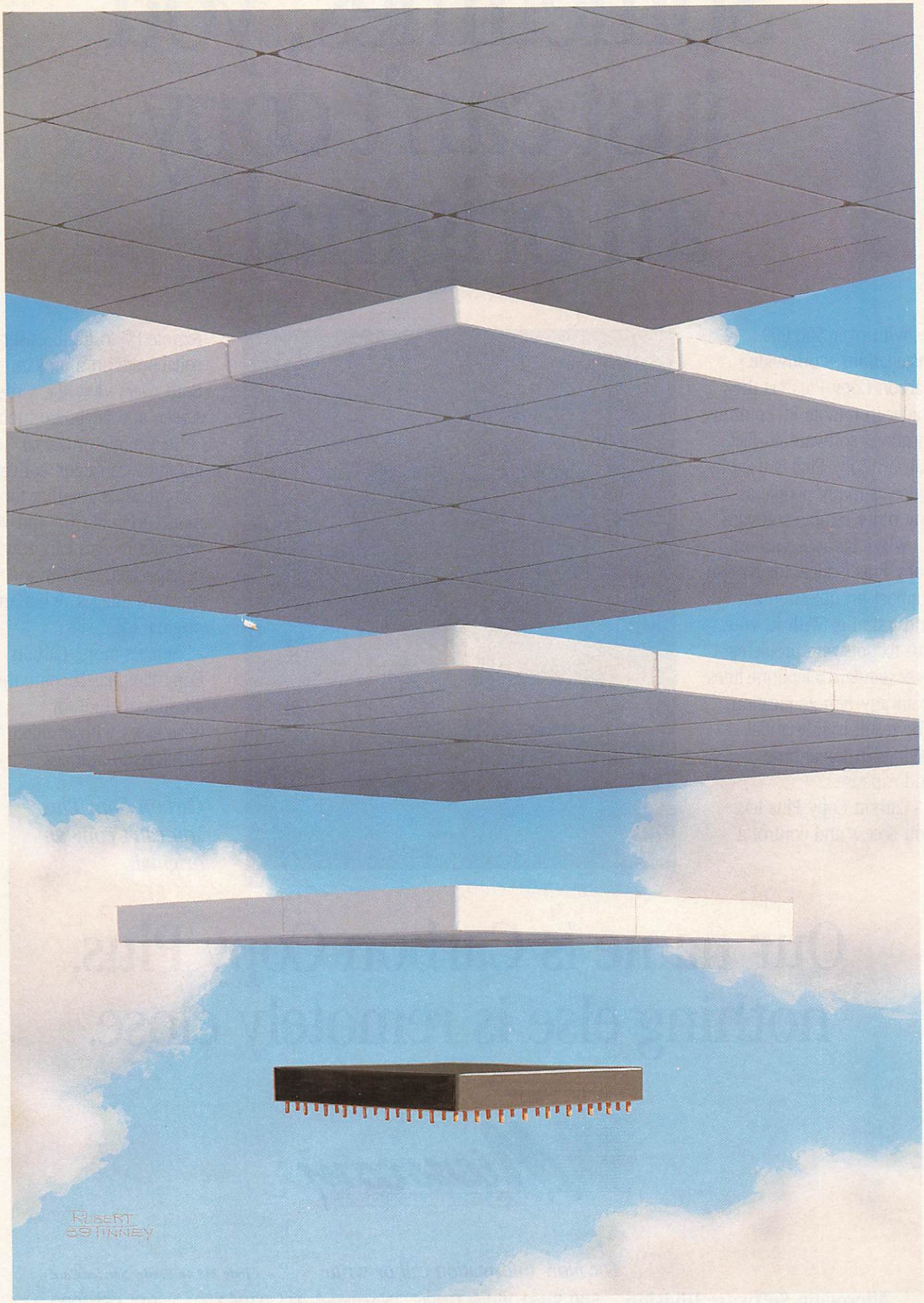


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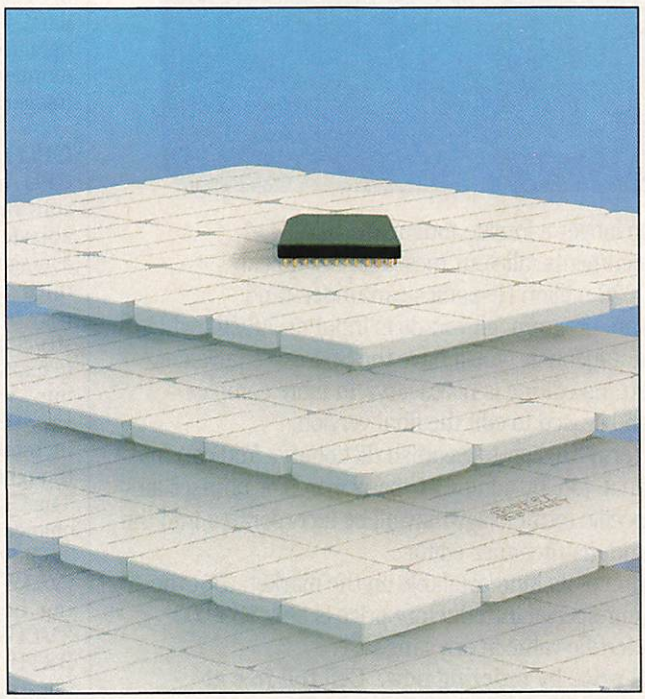
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Are 32 Bits Enough?

Microprocessors have grown from 8 bits to 16 bits to 32 bits. Do we need to keep them growing?

Steve Krueger



In the mid-1970s, it had become clear that the data width of microprocessors would grow from the 8 bits that were common then. At that time, there were many good reasons why microprocessor words would get bigger: We needed 16- and 32-bit data types, larger and more powerful instructions, and more addressing, and we've gotten them in the 32-bit microprocessors. Is a similar group of forces driving today's 32-bit microprocessors to larger word and instruction sizes? Maybe, but today's arguments are less persuasive and more ambiguous than those that have pushed us this far.

Since the 1970s, many changes have occurred in the way we use microprocessors. High-level languages have displaced assembly language for most applications. The RISC and CISC (complex-instruction-set computer) styles of computer architecture have become distinct. Processor speeds have increased much more rapidly than memory speeds. Memory sizes have increased a thousandfold. Microcomputer hard disk drives are available in the capacities and performances that were to be found in the minicomputers of the 1970s. And system architectures have copied their larger predecessors with direct memory access, multimaster buses, multiple buses, and intelligent peripheral controllers.

I'll divide systems into different parts for ease of discussion: CPU data, instructions, and addresses, and other vital parts of the system—cache memory, main memory, buses, and I/O devices. Different forces and engineering trade-offs govern each of these parts.

CPU Data

Today, CPUs need to support the same data types used in their operating systems and application programs. A compiler will produce most of the instructions that are run on a new microprocessor. Today's CPU architect needs to consider the data types supported by the most important programming languages: C, FORTRAN, COBOL, Ada, and Pascal.

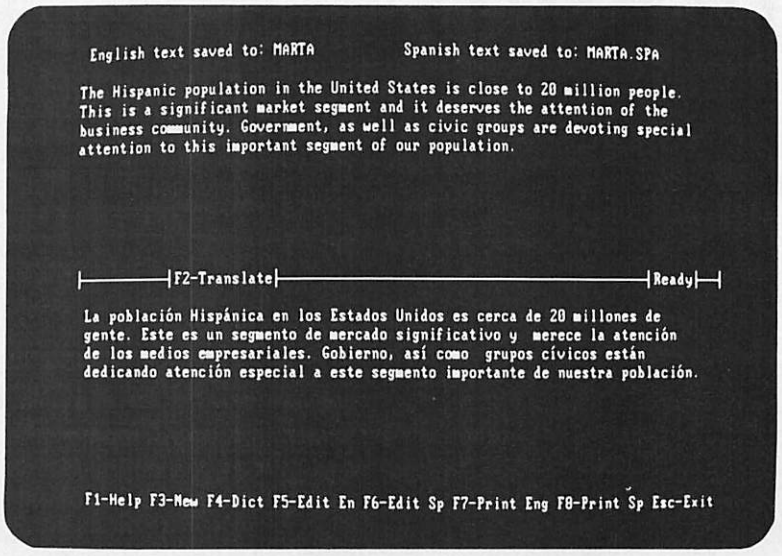
These languages have similar requirements, even if the emphasis is different. In C and Pascal, the most important types are the integer, the character, and the pointer. In FORTRAN, most data is either integer or real. In COBOL, the main data types are string, integer, and fixed-point decimal. Ada combines the requirements of all these.

The sizes of the data used in C on 32-bit microprocessors vary significantly (see table 1). Since standards govern the character and floating-point types, they aren't subject to variations (although character representations for some other

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Table 1: *Standards determine the size of some of C's data types.*

SIZES OF C DATA TYPES

Type	Number of bits	Standard
char	8	ASCII
short	16	
int	16-32	
long	32	
float	32	IEEE
double	64	IEEE
pointer	16-32	

languages, such as Japanese, use more bits). Binary integers are represented in 16 to 32 bits. A few implementations of C provide a *long long* type of 64 bits.

Since this structure of data typing is the most common, most CPU architectures will stick with a primary data size of 32 bits, but they will also support 8-bit data, at least for characters, and 64-bit data for double-precision floating-point numbers and, possibly, double-precision integers (long long).

CPU Instructions

CPU instruction-set architectures have split into a CISC camp that offers variable-length instructions with a short average length and a RISC camp that features fixed-length instructions that are easy to fetch and decode. The RISC instructions have only moderate pressure to expand beyond the nearly universal 32 bits, while CISC instructions already vary in size from 8 to 96 or more bits in increments of 8 or 16 bits (which can be thought of as the basic instruction size). The CISC scheme is under no pressure to change, either.

Only the very-long-instruction-word (VLIW) computers are currently pushing beyond 32-bit instructions (see "VLIW: Heir to RISC?" in the August BYTE). The Multiflow Trace computers (an example of VLIW) use instructions as large as 1 kilobit. However, it will be more than five years before this technology has an impact on the CPU market.

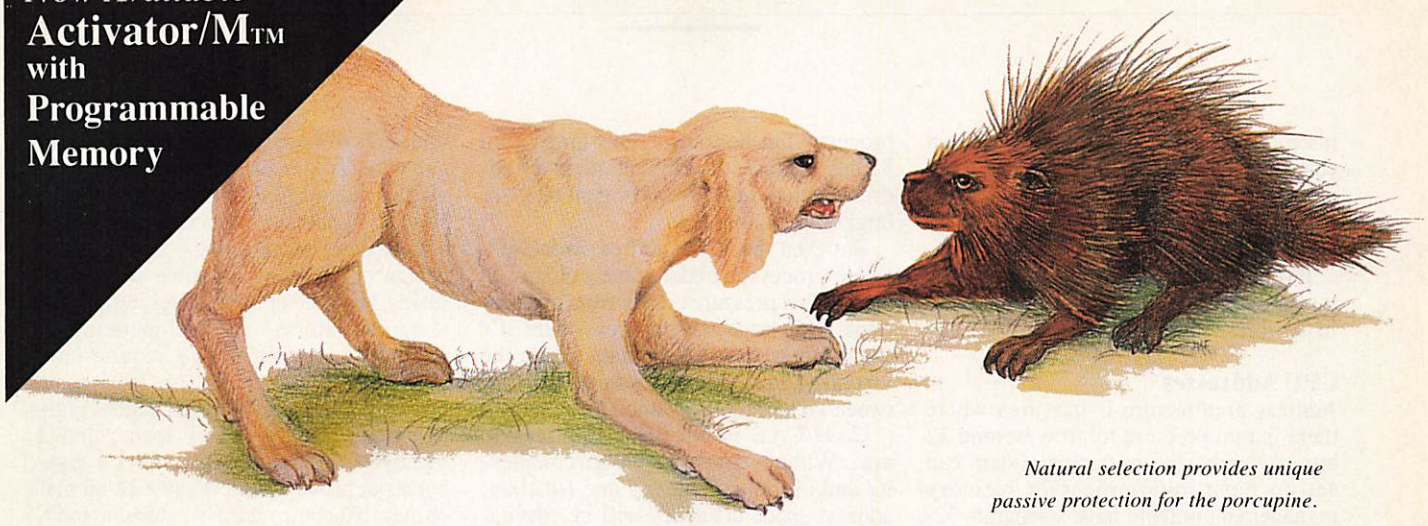
What will happen soon in microprocessors is *superscalar* execution. In superscalar execution, the microprocessor attempts to start two or more conventional instructions on each cycle. The decode logic must test for resource conflicts and data dependencies to schedule the few

continued

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instructions currently available without changing the result of the program. A superscalar processor will become starved for instructions unless several instructions are fetched in each cycle.

Basically, I see no pressure to increase instruction word size in microprocessors in the foreseeable future.

CPU Addresses

Address architecture is one area where there is real pressure to grow beyond 32 bits. Already, the operating system can set up most microprocessor memory management units to have a separate 32-bit address space for each process. The combined memory addressed by all the processes can be considerably larger than 32 bits. In fact, the physical memory addresses that most MMUs generate are larger than 32 bits.

But even the 32-bit address space of a single process is under some pressure to grow. This pressure comes from applications with large data spaces where it's important to keep all the data within the virtual address space rather than split between virtual memory and files.

CAD/CAE is one such application area. With the growth of design complexity and of tool complexity and function, address-space crunches will be inevitable. Within five years, ICs that have more than 10 million transistors will be under development. If each transistor and wire is represented by just 20 bytes in virtual memory, such a design will take about a gigabyte of virtual memory. The sophisticated applications that make a design of this scale possible will themselves be tens of megabytes large; the temporary storage used in operating on the design as a whole will require hundreds of megabytes. So, by 1995 some large CAD applications will need 2 gigabytes of process address space, and 2 gigabytes is close enough to the 4 gigabytes per process limit of most 32-bit machines that some address-extension techniques will be needed.

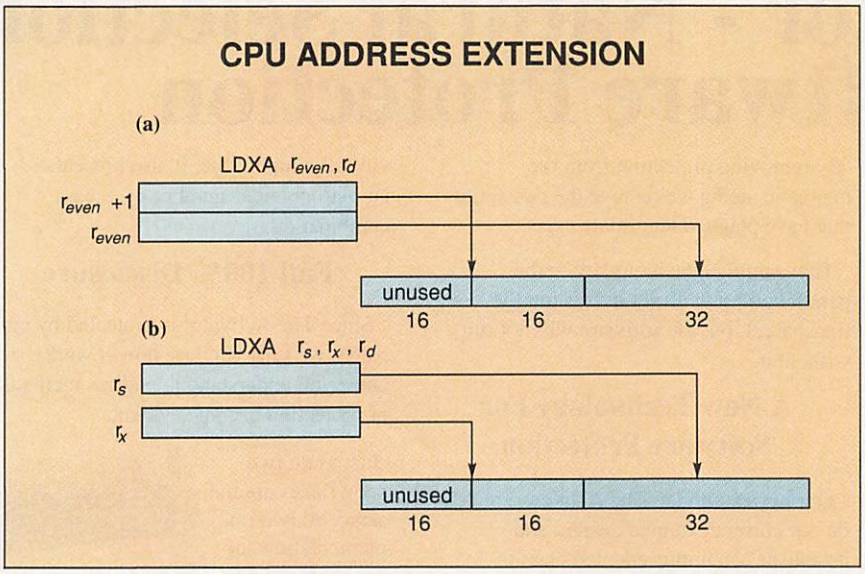


Figure 1: *Two registers are combined to produce a 48-bit address:* **(a)** *48-bit extended address in a register pair;* **(b)** *48-bit extended address in two registers.*

However, for the majority of applications, 4 gigabytes of address space per process is more than enough. With that much space, a text editor could edit a 1-million-page document, and spreadsheets could be thousands of times larger than on a 640K-byte IBM PC. Thus, I don't think address extension within a process will be a crucial issue in the early 1990s.

When longer addresses become an issue, engineers won't choose to lengthen the machine word. Instead, they will use a variety of tricks to give larger addresses to those few processes that need them without increasing the size, complexity, or run time of the more common small processes. This is a continuation of the "small model" and "large model" used in compilers for Intel 80x86 architectures for the same reasons: size, complexity, and speed.

One of the tricks would be to provide `long_ptr` forms of memory-reference instructions that use a register pair to contain a 40-, 48-, or 64-bit address (see figure 1a). These could be loaded and

Table 2: *You can calculate the processor's memory bandwidth requirement with the equation MIPS × (SZI + (FRW × SZD)) = PMB. You can also determine the main memory bandwidth requirement with the equation PMB × CMR = MMB.*

	SYSTEM BANDWIDTHS					
Native processor MIPS	SZI[1]	FRW[2]	SZD[3]	PMB[4]	CMR[5]	MMB[6]
3.8	2.2	0.5	4.5	16.9	1.2-8.0%	0.20-1.35
5.1	2.0	0.5	4.2	20.9	1.2-8.0%	0.25-1.67
10	4.0	0.3	3.8	51.4	1.2-8.0%	0.62-4.11
22	4.0	0.3	3.8	113.1	1.2-8.0%	1.36-9.05
45	4.0	0.3	3.9	232.6	1.2-8.0%	2.79-18.61

[1] SZI = The average instruction size in bytes.
[2] FRW = The fraction of instructions that read or write memory data.
[3] SZD = The average size of data access in bytes.
[4] PMB = The megabytes per second of instructions and data at the processor.
[5] CMR = The cache-miss rate.
[6] MMB = The megabytes per second of memory traffic.

stored with `long_ptr` data if a 64-bit integer type is supported.

Another trick (especially appropriate for load/store architectures like RISC machines) uses an extra source register for the most significant part of the address (see figure 1b). This allows those applications that can statically allocate regions of the extended address space to certain classes of data (e.g., like types, or groups of data referenced together) to treat extended address space as segments, possibly saving many loads and stores of the high-order address word.

The compiler would generate ordinary memory references for small model programs and the majority of the references in gargantuan model programs. These would reference the first 4 gigabytes of the process's address space, the same part referenced if the high-order part of the address is zero.

System Bandwidth

The system bandwidth requirements govern the widths of the various data paths outside the processor. Table 2 shows the bandwidth requirements from the processor to cache memory and from cache memory to main memory points within the system.

The PMB column of table 2 shows the memory-access bandwidth created by several realistically hypothetical processors. The first two are similar to currently common CISC processors. The rest are similar to RISC processors, current and future. Notice that the volume of data that must be supported grows from about 17 megabytes per second with a processor similar to current ones to over 230 megabytes per second with a high-speed RISC processor such as may be expected in the future. Main memory will be able to supply only about 40 megabytes per second if you assume a 32-bit-wide main memory and a 100-nanosecond access time. Cache memories can fill the gap.

Cache memory is a fast memory that stores recently referenced data. If a subsequent reference needs the same data, the cache can supply it much more quickly than main memory. Today, cache memories for microprocessors range from 256 bytes to 64K bytes. With this range of sizes and when processing an average program, the cache can supply the needed data on over 90 percent of the memory references.

The percentage of references that the cache memory can satisfy is called the *hit rate*. For the most common sizes (4K bytes to 64K bytes), you can expect the hit rate to be in the range of 92 to 98.8 percent. Conversely, the *miss rate* is the percentage of references where the cache memory cannot supply the needed data. The hit rate and miss rate always total 100 percent, so a hit rate of 92 percent corresponds to a miss rate of 8 percent.

If a high-speed cache memory can satisfy 92 percent of the references, then main memory need only satisfy about 8 percent. Thus, from the 232.6 megabytes per second of traffic generated by the fastest processor in table 2, the main memory needs to supply only about 18.6 megabytes per second (see figure 2). Often, however, several requests that the cache memory can't satisfy arrive in quick succession, placing a much higher peak demand on memory performance. As a rule of thumb, the main memory should be able to supply two to three times the average bandwidth required.

Cache Memory

Three design trends are apparent in cache memories. First, almost every system will have caches. Second, the caches will be integrated onto the chip with the CPU. And third, in many of the highest-performance systems, the on-chip caches will be too small for the system performance desired, so a second level of cache will be connected directly to the CPU's pins.

The data width of on-chip instruction and data caches will be at least as wide as the CPU needs and may be wider to support the bandwidth required. If the CPU supports only 8-, 16-, and 32-bit data,

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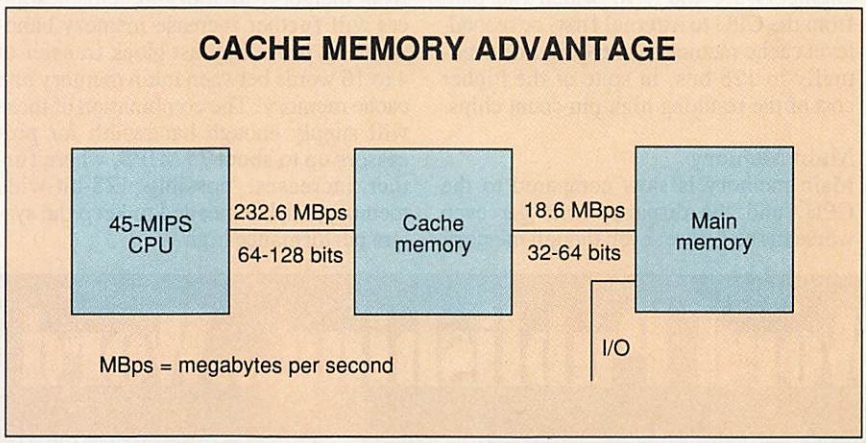


Figure 2: *Cache memory cuts main memory bandwidth by satisfying most memory requests.*

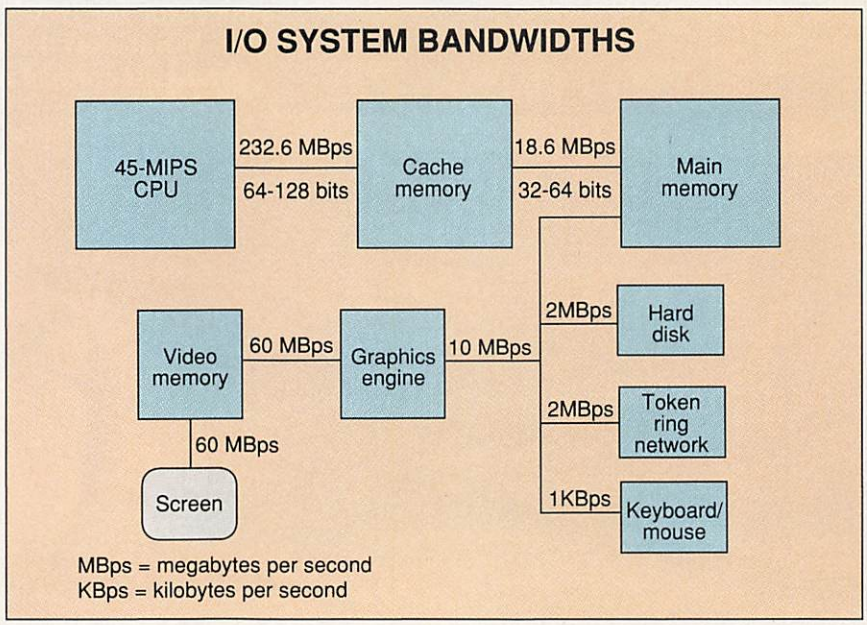


Figure 3: *Different I/O devices have different bandwidth needs.*

the data-cache width will be 32 bits. If the CPU also supports 64-bit data, the data-cache width will need to be 64 bits.

The data width of the cache memories may be wider to accommodate the higher bandwidth requirements of superscalar, vector, or other high-performance architectures. Extra data width costs little in on-chip cache memories where connections between the CPU and the cache are easily provided. Extra data width is more expensive in external caches, which are constrained by the cost of providing additional data pins on the CPU chip.

And yet, a large difference in speed exists between internal and external signals so that an external cache is slow compared to an on-chip cache. To reclaim the bandwidth lost over slow pins, engineers are likely to widen the path from the CPU to external first- or second-level cache memories to 64 bits and eventually to 128 bits, in spite of the higher cost of the resulting high-pin-count chips.

Main Memory

Main memory is slow compared to the CPU, and the disparity will get even worse in the future, even though memory itself will continue to get faster. Main memory will have difficulty supplying the bandwidth that high-speed processors need, even after the caches have reduced it. A 32-bit-wide memory system constructed out of 80-ns DRAM chips will have an access time of about 150 ns for a bandwidth of about 27 megabytes per second, just enough for the 22-million-instruction-per-second RISC processor in table 2. In practice, the system bus will add at least 100 ns to the access time and reduce the bandwidth to 16 megabytes per second, enough for the 10-MIPS processor but not enough for the higher-performance processors.

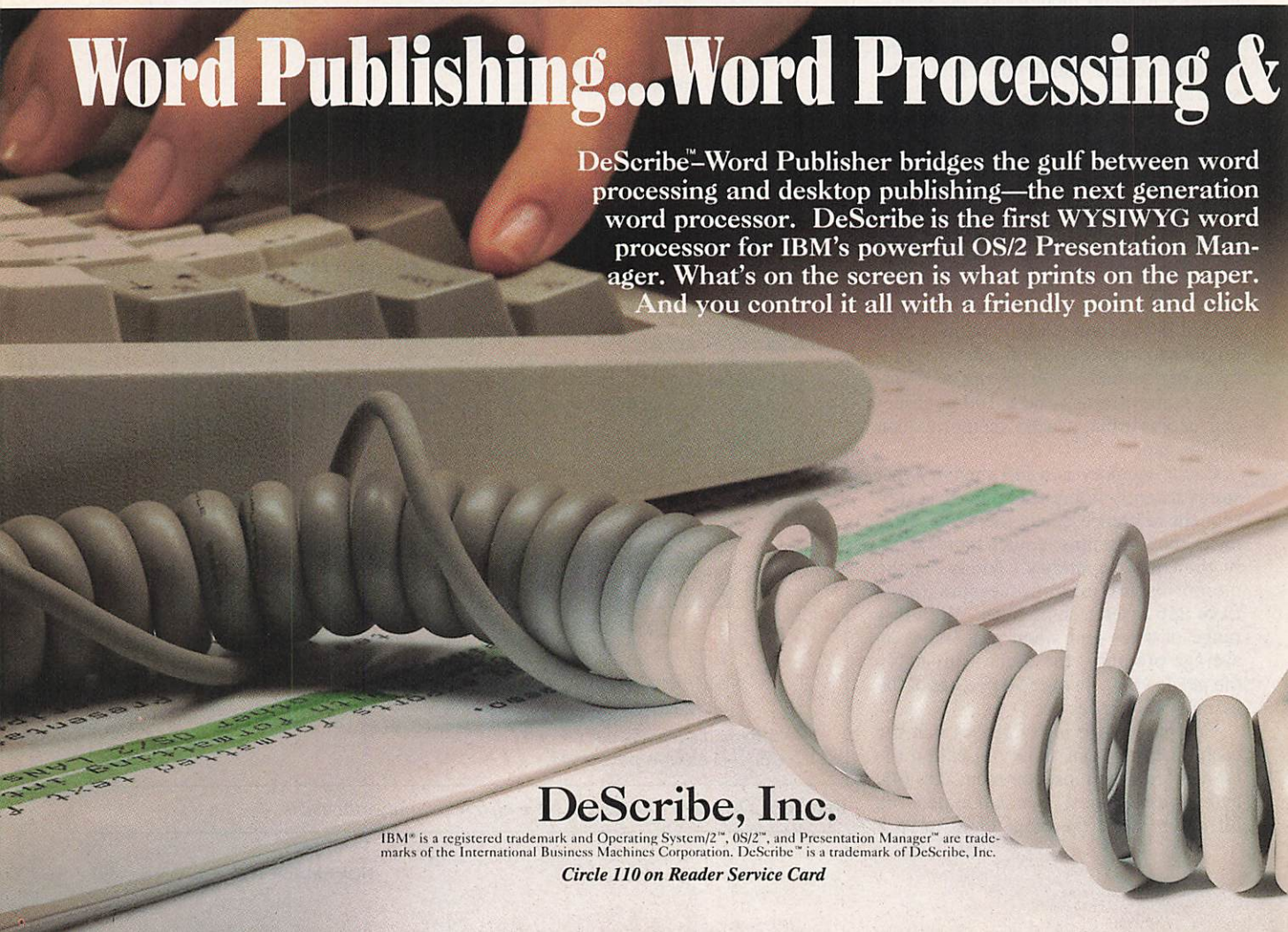
For systems with processors faster than 20 MIPS, memory will be 64 bits wide, doubling the bandwidth available from memory. Memory-systems designers will further increase memory bandwidth by providing fast block transfer of 4 to 16 words between main memory and cache memory. The combination of these will supply enough bandwidth for processors up to about 75 MIPS, where further increases, possibly 128-bit-wide memory, will be needed to keep the system performance high.

System Buses

System buses are another place where you can lose bandwidth. The amount of time that the system bus adds to a memory access will decrease the memory bandwidth available. The system bus adds time for arbitration, address propagation, and data propagation. The physical size and electrical properties of the bus limit the minimum propagation times, which won't get below 50 ns on expansion buses with several slots.

Engineers designing system buses can lessen the effect of propagation time by using wider buses and by including block transfers. Wider buses transfer more data on each bus cycle, effectively doubling the bandwidth available. Expansion buses have grown from 8 bits to 32 bits as memory and I/O performance needs have dictated. Block transfers send several words of data in a single bus transaction, saving the arbitration and address propagation delays after the first word. If the memory system can supply data that quickly, the average time per word decreases and the bandwidth increases.

The last design trend is already firmly entrenched in the industry and will cer-



tainly continue: separating the memory bus from the I/O or expansion bus. Because memory bandwidth is so crucial to high-performance computers, engineers will pay close attention to high-performance memory buses within the cost constraints of the final system. 64-bit memory buses will be common. On the other hand, I/O buses will be limited to 16 or 32 bits to control costs and match the width of I/O devices. In servers and other systems where I/O bandwidth is crucial to performance, multiple I/O buses, not wider data paths or higher speed, will supply the needed bandwidth.

I/O Devices

I/O devices don't need wide buses (see figure 3). Even a SCSI-2 disk peripheral transfers at a maximum of only 2 megabytes per second, which is also the peak transfer rate for a 16-megabyte-per-second token ring. An FDDI (fiber distributed data interface) network, at 12 megabytes per second, will tax today's slower I/O buses but is easily supported on the Micro Channel, the NuBus, or EISA.

Probably the only I/O device that taxes a high-performance I/O bus is a graphics frame buffer. Fast redraw of the video screen is important to the perception of high performance. One simple benchmark is to copy a full-screen image from memory to the screen buffer. For a system with adequate performance (and reasonable crispness), the copy should take less than $\frac{1}{10}$ second; for a high-performance system, less than $\frac{1}{60}$ second.

For a megapixel display with 8-bit pixels, this image consumes a megabyte. So for a $\frac{1}{10}$-second copy time, the CPU must access the frame buffer with at least 10 megabytes per second of bandwidth. For a $\frac{1}{60}$-second copy time, the CPU needs at least 60 megabytes per second of bandwidth to the frame buffer, far beyond the attainable bandwidth on the Micro Channel, the NuBus, or EISA.

An even tougher benchmark is a full-screen move from the frame buffer to itself, as when you move a window on the screen. With the same megapixel display, this would require over 20 megabytes per second of bandwidth to the frame buffer for the lowest acceptable performance. This is barely attainable with the Micro Channel, the NuBus, or EISA. As a result, engineers will have to choose either to attach frame buffers to the systems-memory bus, or to use a graphics processor directly attached to the frame buffer and communicate with the main processor over the I/O bus.

Strike Up the Bandwidth

Systems will grow in bit width in a number of places, but there is little reason for CPU designers to make major changes in CPU architecture in the next few years and probably the next decade. By 1995, however, almost every CPU will have some minor changes to support extended addressing beyond 32 bits per process.

Many CPUs will support double-precision floating-point processing with 64-bit data paths and arithmetic. Memory and memory buses will expand to accommodate the higher bandwidth demands of high-performance CPUs. Bandwidth issues will dominate systems design. ■

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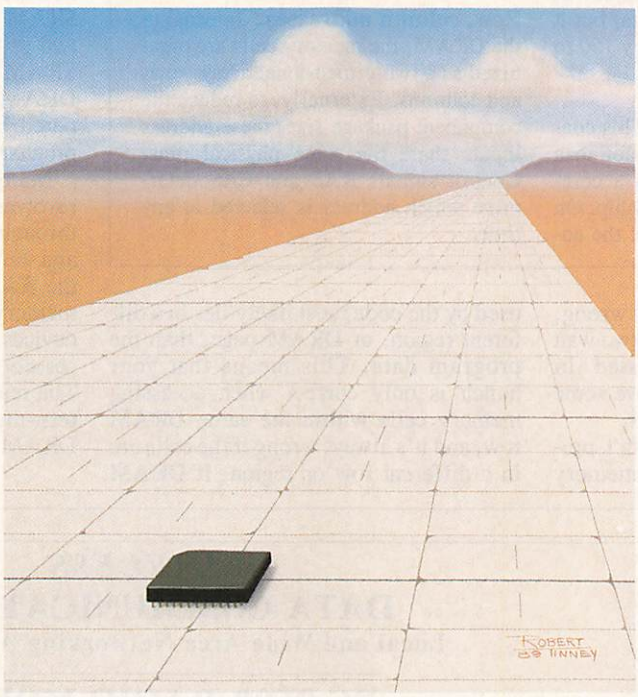
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Seeking a Wide Berth

Wider memory isn't necessarily faster; application demands, memory design, and control logic all affect performance

Ron Sartore

Although 32 bits has now become synonymous with power and performance in today's microcomputers, the truth about wide memory is subtler and more complex than many people realize. It's true that when moving blocks of wide data from one part of the system to another, 32-bit memory architectures easily outrun 8- and 16-bit designs. But transporting data is only a part of what computers do. Many operations and data types don't require 32 bits: ASCII characters, for example, are only 8 bits wide, and some operands are only 1 or 2 bytes wide. In these cases, the extra memory width is wasted and can even introduce inefficiency into the system.



Designing wide memory is not conceptually difficult: Think of it as stacking the bytes side-by-side instead of one on top of the other. In principle, wider memories provide more data faster and more easily. Yet doubling or quadrupling memory width is riddled with trade-offs: When you're operating on small pieces of data, it can seem like doing surgery with a bulldozer. Applications that don't mate well with the memory architecture may find their performance crippled, even when running on the fastest processors. How can this be? Can the memory interface actually be *too* wide?

The answer requires an analysis of what you do with memory. Wider memory is good when the proper memory control is in place. The most fundamental issue is that no matter how wide the memory is, high performance for byte operations must still be maintained. Thus, the trick in memory-system design is to provide both quick byte manipulation and fast wide-data movement. It is counterproductive to focus on one and ignore the other.

Sizing Things Up

Memory-controller design is not greatly influenced by the total size of memory or the data-path width. In fact, the most important design factors are how many controllers are used and what section of memory they watch.

Controller sophistication can vary from a simple step-and-fetch-it approach to complex schemes involving more control logic than memory components. Different memory-control algorithms for the same memory board can affect the result of a benchmark program by more than 10 percent.

For example, it's possible to keep a DRAM chip accessed (i.e., keep the row address strobe [RAS] active on completion of an access) on the hunch that the next access will be within the same row. (To enable this scheme, the controller must contain address comparators.) If the hunch is right, you will have a zero-

continued

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Explaining DRAM

Access time After the initiation of row address strobe (RAS), this is the minimum time required for the DRAM to return data that is guaranteed to be valid.

CAS (column address strobe) This control signal performs several functions. First, it indicates that the address pins to the device contain a desired column address. Whether the address is latched or passes through directly determines clocked page mode and static column mode, respectively. Second, CAS is used to enable the data output driver for read cycles. To access a column, a row access (RAS is active) must be performed first and persist throughout one or more column accesses.

Cycle time The access time plus the RAS precharge equals the total cycle time for the DRAM. This means that a 100-nanosecond chip, for example, will take 100 ns to return valid data, but it can be accessed only once every 150 to 180 ns.

RAS (row address strobe) This control signal is the major activator to a DRAM component, initiating a complex series of events within the chip. On initiation, it latches the state of the address pins to be used for the row access. Once initiated, it must then be followed through, because an aborted cycle will corrupt the contents of an entire DRAM row.

RAS precharge After a completed access, RAS needs to take a "breathing spell" to ramp up for the next access. The duration of this delay is typically half the access time; thus, an 80-ns DRAM might require 40 to 60 ns for precharge.

Refresh The charge of each bit within a DRAM is held by a *very* small capacitor (on the order of 50 femtofarads). When the bit isn't accessed, the charge slowly decays and will be lost if not refreshed. A refresh cycle is a type of read cycle that reenergizes a whole row of bits. About one in 100 cycles must be devoted to this task.

Row, column addresses Internal to the DRAM, the memory cells are organized as a two-dimensional array, rows and columns. Externally, to reduce the component package size, these address inputs share the same physical pins. Control signals RAS and CAS determine which address is selected at any time.

wait-state transfer; but if it's wrong, there will be a penalty of at least two wait states while a new row is accessed. In short, this approach will improve some benchmarks while hurting others.

One reason this scheme doesn't produce more benefits is that the memory used by the code most likely lies in a different region, or DRAM page, than the program data. This means that your hunch is only correct when accessing memory cells within the same DRAM row, and it's always wrong if the cells are in a different row or region. If DRAM chips permitted you to access two (or four) rows simultaneously, you could then treat DRAM as both main storage and cache and eliminate wait states when changing from one memory area to another.

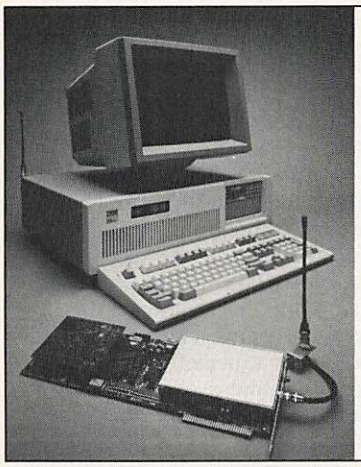
DRAM vs. SRAM

Since much of the discussion on large memories involves DRAM, it's necessary to understand the terms and concepts of the device itself (see the text box "Explaining DRAM" at left). What makes DRAM chips attractive is their high ratio of storage density to price: Because DRAM uses one transistor per bit, whereas static RAM uses four to six transistors per bit, DRAM will provide four times the storage of SRAM for an equivalent price, at any given technology level. DRAM chips also offer better board-packing density because they double up address pins (row and column), while SRAM chips receive all addresses at once, which requires more physical pins but is faster.

In fact, the major disadvantage of DRAM is speed, especially compared to SRAM. The access time for DRAM is two to three times longer than it is for SRAM of the same technology, and DRAM performance is further hampered by the time consumed for RAS precharge and refresh cycles.

Many memory-system architectures revolve around optimizing DRAM usage through techniques such as interleaving and burst transfers. Interleaving hides the RAS precharge delay by alternating memory addresses in different DRAM devices, so that one DRAM device is accessed while the other is precharging. The result of interleaving is that the system-memory cycle time equals the DRAM access time, just as it would for

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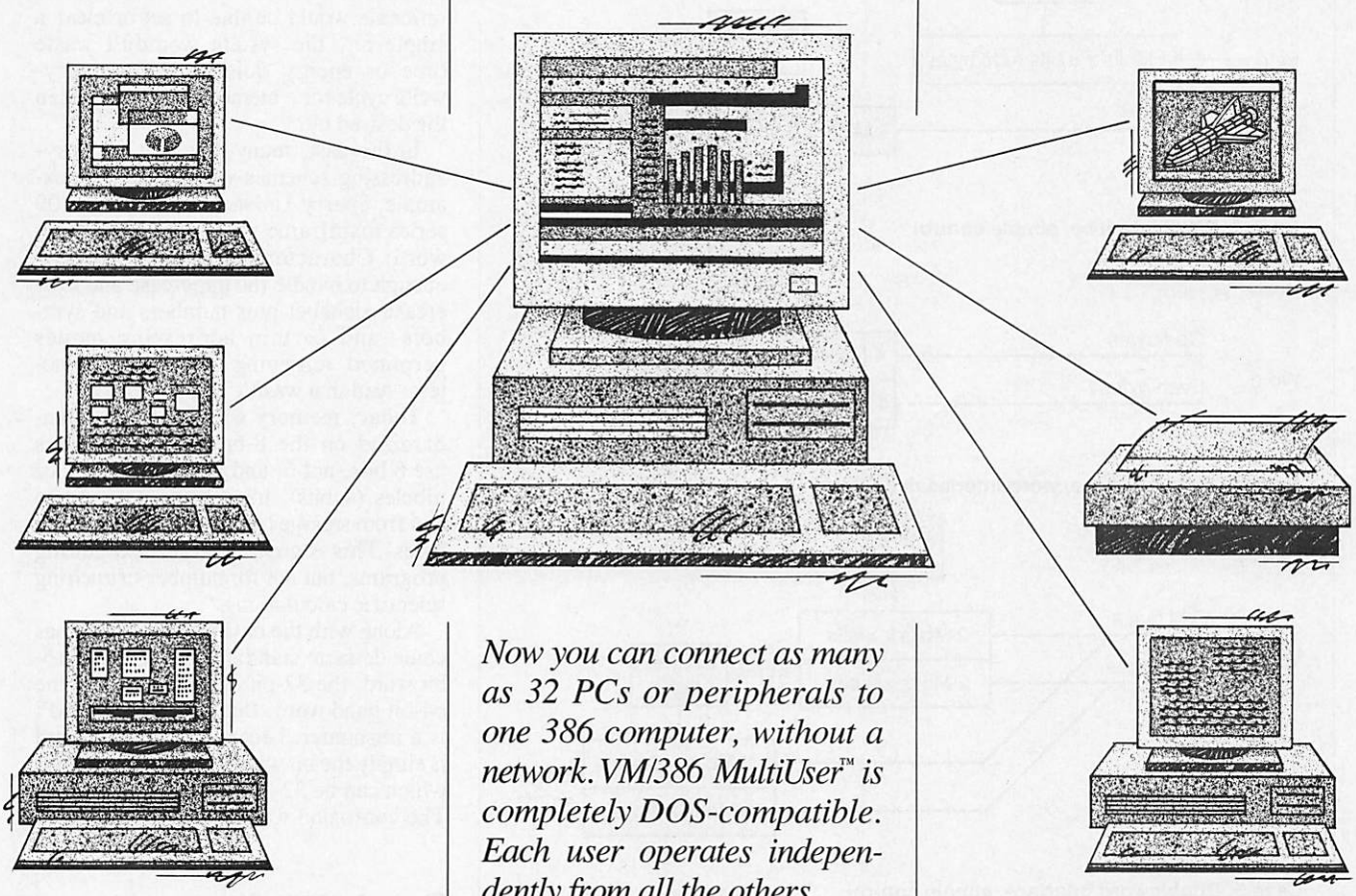
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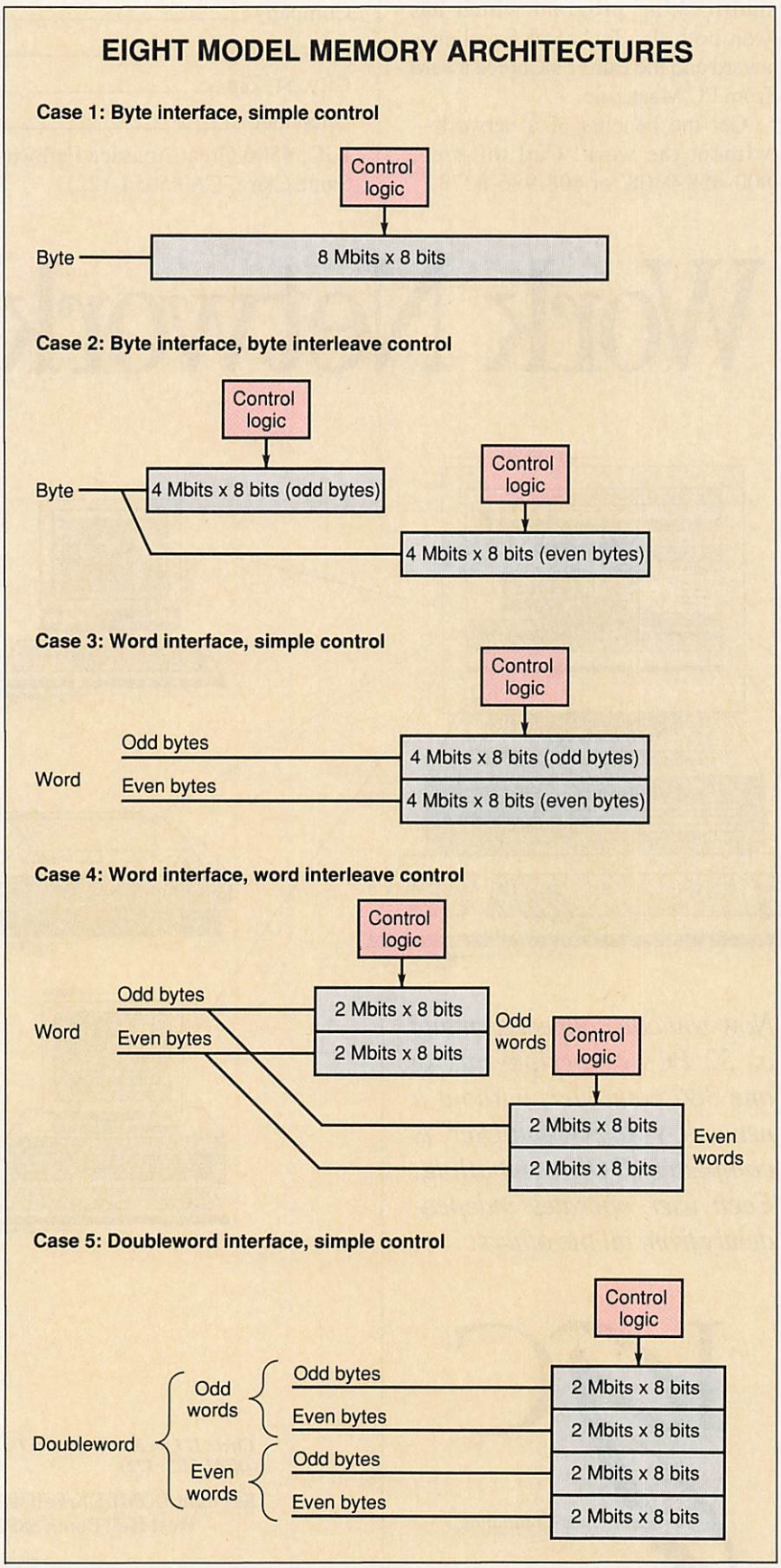
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SRAM. Burst transfers boost performance by moving blocks of data from DRAM to a high-speed SRAM cache or to the processor.

Choosing Configurations

Assuming that DRAM chips are a desirable component in the construction of a system's main storage, how should they be arranged? Within a given system, the designer can specify any number of bits as the memory-access width. So how is an optimal memory word defined?

If a computational problem involved operating on a single bit, a designer might wish the processor permitted a memory-word interface that was only 1 bit wide! As absurd as that sounds, the rationale would be that to set or clear a single bit, the system wouldn't waste time or energy doing a read-modify-write cycle for a memory area wider than the desired bit.

In the past, many different memory-addressing schemes were tried. For example, Sperry-Univac's successful 1100 series mainframe was based on a 36-bit word: Characters were 6 bits wide—enough to handle the uppercase and lowercase alphabet plus numbers and symbols—and certain addressing modes permitted retrieving 3-bit half-characters. And that wasn't very long ago!

Today, memory addressing has standardized on the 8-bit byte. Characters use 8 bits, not 6, and half-characters, or nibbles (4 bits), must be transferred to and from storage by the processor in 8-bit bytes. This is great news for text-editing programs, but not for number-crunching scientific calculations.

Along with the definition of a byte has come de facto standardization on the 16-bit word, the 32-bit doubleword, and the 64-bit quad word. But the 16-bit "word" is a misnomer, because a memory word is simply the bit width of memory access, which can be 32 bits as easily as 16 bits. The confusion would be alleviated if 16

continued

Figure 1a: *Eight different model memory architectures:*
(Case 1) *An 8-bit (byte) noninterleaved memory (akin to that of an IBM PC XT).*
(Case 2) *An 8-bit (byte) two-way interleaved memory, or "pseudo 16."*
(Case 3) *A 16-bit (word) noninterleaved memory (akin to that of an IBM PC AT).*
(Case 4) *A 16-bit (word) two-way interleaved memory, or "pseudo 32."*
(Case 5) *A 32-bit (doubleword) noninterleaved memory (like most found in 80386 machines).*

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bits of data were called a double byte.

At the same time that the industry was resolving text-character representation between EBCDIC and ASCII (guess which won), a similar turmoil was brewing over number representation. Here, the IEEE stepped in to coordinate matters. Currently, IEEE standard 754 (version 10) specifies a 32-bit representation for single-precision floating-point numbers (a 23-bit significand with an 8-bit exponent plus 1 sign bit). Double-precision floating-point numbers use 64 bits of memory, and extended double-precision floating-point numbers use 80 bits.

Memory performance is too much a function of application requirements and controller design to be easily improved with a quick fix.

Another driving force behind larger memory widths has been in the representation of the program itself. Both program control (such as jumps or calls) and data access require address content within the code: If a program is to access large amounts of memory, it also needs to be able to retrieve and operate on large addresses. This holds true for direct addressing, indirect access (where memory contains the next address), and indirect access with a code offset.

The Dilemma

Many of today's personal computer benchmarks (including BYTE's) use the term *word* to denote 16 bits. In doing so, a benchmark that measures 16-bit-word moves to an even- or odd-word boundary encounters memory-transfer inefficiency when it communicates with non-word-width memories. If you want to compare 8088s with 80286 and 80386/80486 machines, you must have rules and consistent tests; but choosing a stock word width doesn't really seem fair when comparing machines that use different widths. The examples that follow demonstrate the implications of this.

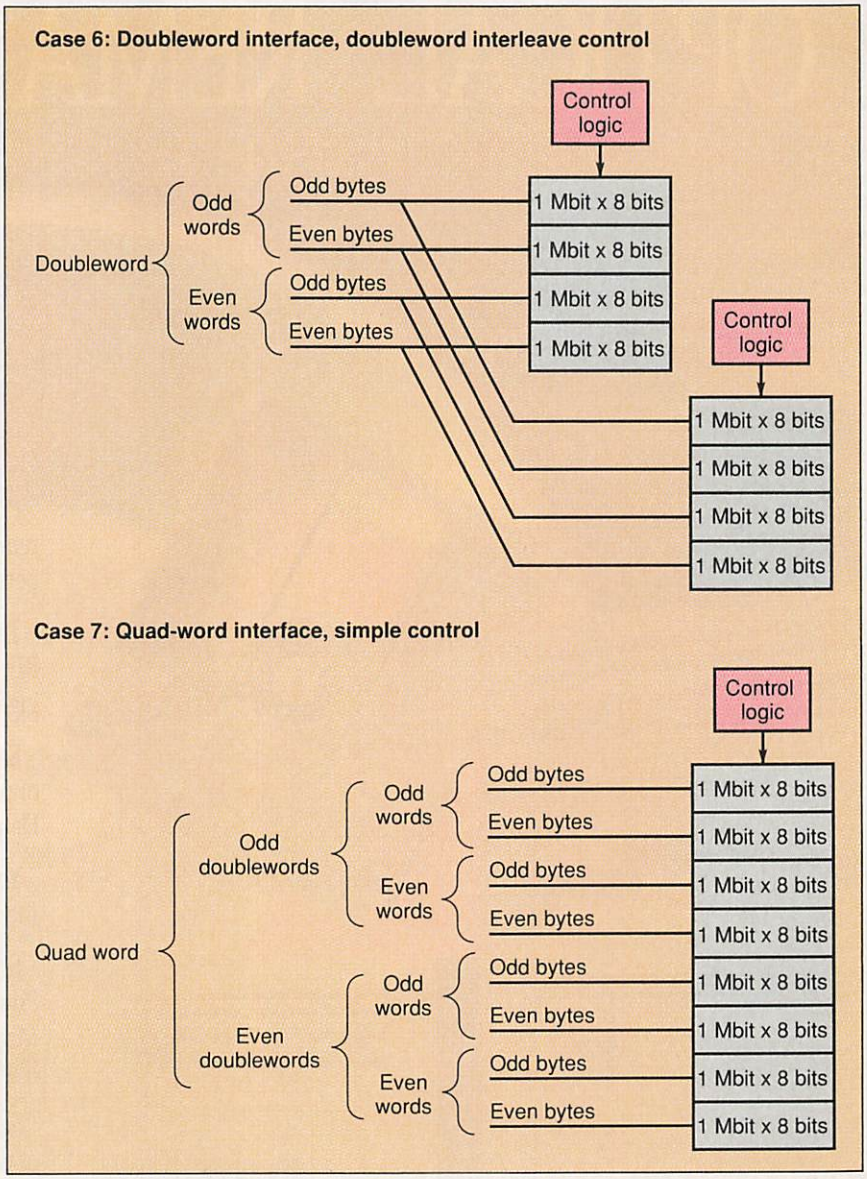


Figure 1b: (Case 6) *A 32-bit (doubleword) two-way interleaved memory, or "pseudo 64."* **(Case 7)** *A 64-bit (quad-word) noninterleaved memory.*

To really understand the trade-offs inherent in the choice of memory width, you can construct a series of imaginary memory architectures and test them in different situations to compare their performance. The simulated memory can be accessed in two "ticks" of the clock and has a three-tick cycle time.

The simplified example uses eight different memory architectures. Block diagrams representing the eight imaginary memory organizations are shown in figure 1. Case 8 doesn't exist in any personal computer and is a perfect example of control-logic chips rivaling the number of memory chips.

For the first scenario, imagine handling a byte string move in an address transition of 1 byte. To keep it fair, start all systems "ready to access," and for brevity, transfer only 8 bytes. You can also assume that the starting address is a common word boundary for all systems and that data is moved to an adjacent (lower) byte. A symbolic representation for each case will use the following notation:

C = cycle (intermission between accesses to the same memory element)
r*n* = first half of read cycle, byte *n*

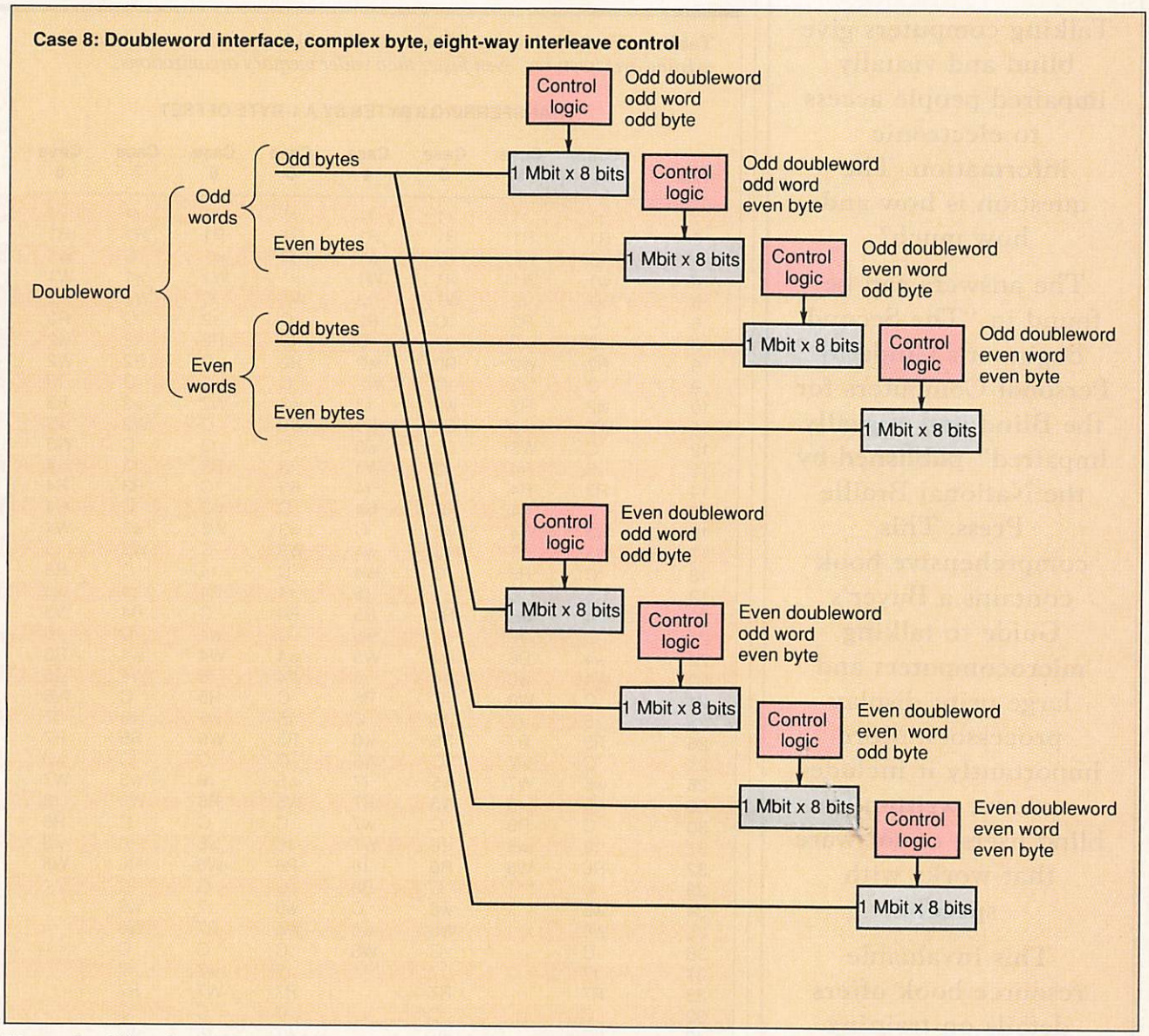


Figure 1c: (Case 8) *A 32-bit (doubleword/word/byte) eight-way interleaved memory, or pseudo 64.*

R*n* = second half of read cycle, byte *n*
w*n* = first half of write cycle, byte *n*
W*n* = second half of write cycle, byte *n*
*** = operation complete

In the first test, the 8-bit interleaved memory (case 2) would be the fastest among the existing architectures, quicker even than wider memory organizations (see table 1). But if you move each byte by an offset of 2 bytes (as shown in table 2), the 16-bit interleaved structure (case 4) is fastest, with 8- and 32-bit interleaved organizations (cases 2 and 6) tied for second place. Memory width and interleaving control yield benefits that are dependent on two things: the operand data width (8, 16, or 32 bits) and the offset and alignment that data traverses.

Although wider memories are slower, they produce benefits. Processors such as the 80386 and 80486 can use 32-bit operands; when they do, they outstrip systems with narrower memories. To demonstrate this, move two 32-bit words by an offset of one 32-bit word.

The scenario depicted in table 3 shows a fivefold improvement for the 32-bit interleaved memory over the 8-bit noninterleaved memory. This strongly suggests that if your processing requires 32-bit floating-point calculations, you should choose a machine that excels in 32-bit performance. Ignore the benchmarks that compare machines on byte operations; they may be misleading.

But if wider memories aren't necessarily better for handling small chunks of data, such as characters or byte operands, why use them? The answer points to a drawback in the simulation: The tests it runs are just a subset of what typically goes on within a system. If, in a real computer, every other CPU operation were a write to memory, then caching wouldn't do much good.

In reality, the ratio of memory-write operations to memory reads rarely exceeds 1-to-4, because the code portion of memory isn't written to except when

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Table 1: *The 8-bit interleaved memory (case 2) is the fastest among the existing architectures, even faster than wider memory organizations.*

TRANSFERRING 8 BYTES BY A 1-BYTE OFFSET

Tick	Case 1	Case 2	Case 3	Case 4	Case 5	Case 6	Case 7	Case 8
1	r1	r1	r1	r1	r1	r1	r1	r1
2	R1	R1	R1	R1	R1	R1	R1	R1
3	C	w1	C	w1	C	w1	C	w1
4	w1	W1	w1	W1	w1	W1	w1	W1
5	W1	r2	W1	r2	W1	C	W1	r2
6	C	R2	C	R2	C	r2	C	R2
7	r2	w2	r2	C	r2	R2	r2	w2
8	R2	W2	R2	w2	R2	C	R2	W2
9	C	r3	C	W2	C	w2	C	r3
10	w2	R3	w2	r3	w2	W2	w2	R3
11	W2	w3	W2	R3	W2	C	W2	w3
12	C	W3	C	w3	C	r3	C	W3
13	r3	r4	r3	W3	r3	R3	r3	r4
14	R3	R4	R3	r4	R3	C	R3	R4
15	C	w4	C	R4	C	w3	C	w4
16	w3	W4	w3	C	w3	W3	w3	W4
17	W3	r5	W3	w4	W3	C	W3	r5
18	C	R5	C	W4	C	r4	C	R5
19	r4	w5	r4	r5	r4	R4	r4	w5
20	R4	W5	R4	R5	R4	C	R4	W5
21	C	r6	C	w5	C	w4	C	r6
22	w4	R6	w4	W5	w4	W4	w4	R6
23	W4	w6	W4	r6	W4	r5	W4	w6
24	C	W6	C	R6	C	R5	C	W6
25	r5	r7	r5	C	r5	w5	r5	r7
26	R5	R7	R5	w6	R5	W5	R5	R7
27	C	w7	C	W6	C	C	C	w7
28	w5	W7	w5	r7	w5	r6	w5	W7
29	W5	r8	W5	R7	W5	R6	W5	r8
30	C	R8	C	w7	C	C	C	R8
31	r6	w8	r6	W7	r6	w6	r6	w8
32	R6	W8	R6	r8	R6	W6	R6	W8
33	C	***	C	R8	C	C	C	***
34	w6		w6	C	w6	r7	w6	
35	W6		W6	w8	W6	R7	W6	
36	C		C	W8	C	C	C	
37	r7		r7	***	r7	w7	r7	
38	R7		R7		R7	W7	R7	
39	C		C		C	C	C	
40	w7		w7		w7	r8	w7	
41	W7		W7		W7	R8	W7	
42	C		C		C	C	C	
43	r8		r8		r8	w8	r8	
44	R8		R8		R8	W8	R8	
45	C		C		C	***	C	
46	w8		w8		w8		w8	
47	W8		W8		W8		W8	
48	***		***		***		***	

loading, and even then it's treated as data. The model also assumed that you could move a known portion of data without regard to computational considerations, such as source/destination address generation or length of transfer.

Burst Mode: Feature of the Future?

Often, main memory isn't the direct interface to the processor. It has become customary for high-performance systems to incorporate an SRAM cache. The basic principle behind a main-memory cache is that when a given address for data or code is requested, it's very likely that the same or nearby addresses will be requested again. Since the cache controller maps precious SRAM in blocks or sets of words, main-memory operations become either block transfers to fill the

Table 2: *If you move each byte by an offset of 2 bytes, the 16-bit interleaved structure (case 4) is fastest, with the 8- and 32-bit interleaved organizations (cases 2 and 6) tied for second place.*

MOVING 8 BYTES BY A 2-BYTE OFFSET

Tick	Case 1	Case 2	Case 3	Case 4	Case 5	Case 6	Case 7	Case 8
1	r1	r1	r1	r1	r1	r1	r1	r1
2	R1	R1	R1	R1	R1	R1	R1	R1
3	C	C	C	w1	C	w1	C	w1
4	w1	w1	w1	W1	w1	W1	w1	W1
5	W1	W1	W1	r2	W1	r2	W1	r2
6	C	r2	C	R2	C	R2	C	R2
7	r2	R2	r2	w2	r2	w2	r2	w2
8	R2	C	R2	W2	R2	W2	R2	W2
9	C	w2	C	r3	C	r3	C	r3
10	w2	W2	w2	R3	w2	R3	w2	R3
11	W2	r3	W2	w3	W2	C	W2	w3
12	C	R3	C	W3	C	w3	C	W3
13	r3	C	r3	r4	r3	W3	r3	r4
14	R3	w3	R3	R4	R3	C	R3	R4
15	C	W3	C	w4	C	r4	C	w4
16	w3	r4	w3	W4	w3	R4	w3	W4
17	W3	R4	W3	r5	W3	C	W3	r5
18	C	C	C	R5	C	w4	C	R5
19	r4	w4	r4	w5	r4	W4	r4	w5
20	R4	W4	R4	W5	R4	r5	R4	W5
21	C	r5	C	r6	C	R5	C	r6
22	w4	R5	w4	R6	w4	w5	w4	R6
23	W4	C	W4	w6	W4	W5	W4	w6
24	C	w5	C	W6	C	r6	C	W6
25	r5	W5	r5	r7	r5	R6	r5	r7
26	R5	r6	R5	R7	R5	w6	R5	R7
27	C	R6	C	w7	C	W6	C	w7
28	w5	C	w5	W7	w5	C	w5	W7
29	W5	w6	W5	r8	W5	r7	W5	r8
30	C	W6	C	R8	C	R7	C	R8
31	r6	r7	r6	w8	r6	C	r6	w8
32	R6	R7	R6	W8	R6	w7	R6	W8
33	C	C	C	***	C	W7	C	***
34	w6	w7	w6		w6	C	w6	
35	W6	W7	W6		W6	r8	W6	
36	C	r8	C		C	R8	C	
37	r7	R8	r7		r7	C	r7	
38	R7	C	R7		R7	w8	R7	
39	C	w8	C		C	W8	C	
40	w7	W8	w7		w7	C	w7	
41	W7	***	W7		W7	***	W7	
42	C		C		C		C	
43	r8		r8		r8		r8	
44	R8		R8		R8		R8	
45	C		C		C		C	
46	w8		w8		w8		w8	
47	W8		W8		W8		W8	
48	***		***		***		***	

cache (read main memory—write to cache) or single-cycle write operations to update main storage. This is how Intel's 80486, with its built-in 8K-byte cache, interfaces to external memory. A line in the 80486's cache is 4 doublewords wide (128 bits); when the 80486 needs to fill that line, it can use burst-mode transfer.

The memory dialogue for this operation using the simulated memory architectures would look like this. First, you have to alter the conditions slightly. You fill the 80486's on-chip cache using DRAM page mode in 16-byte bursts. With the 80486's 25-MHz clock rate, and assuming that the memories are now implemented with 100-nanosecond

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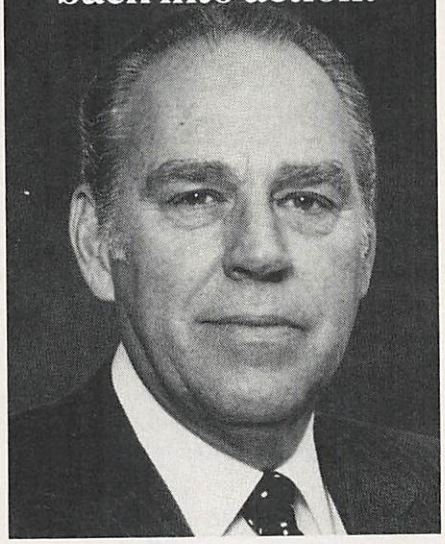


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Table 3: *This scenario shows a fivefold improvement for the 32-bit interleaved memory (case 6) over the 8-bit noninterleaved (case 1).*

MOVING TWO 32-BIT DOUBLEWORDS BY A 4-BYTE OFFSET

Tick	Case 1	Case 2	Case 3	Case 4	Case 5	Case 6	Case 7	Case 8
1	r1	r1	r1-2	r1-2	r1-4	r1-4	r1-4	r1-4
2	R1	R1	R1-2	R1-2	R1-4	R1-4	R1-4	R1-4
3	C	r2	C	r3-4	C	w1-4	C	w1-4
4	r2	R2	r3-4	R3-4	w1-4	W1-4	w1-4	W1-4
5	R2	r3	R3-4	w1-2	W1-4	r5-8	W1-4	r5-8
6	C	R3	C	W1-2	C	R5-8	C	R5-8
7	r3	r4	w1-2	w3-4	r5-8	w5-8	r5-8	w5-8
8	R3	R4	W1-2	W3-4	R5-8	W5-8	R5-8	W5-8
9	C	w1	C	r5-6	C	***	C	***
10	r4	W1	w3-4	R5-6	w5-8		w5-8	
11	R4	w2	W3-4	r7-8	W5-8		W5-8	
12	C	W2	C	R7-8	***		***	
13	w1	w3	r5-6	w5-6				
14	W1	W3	R5-6	W5-6				
15	C	w4	C	w7-8				
16	w2	W4	r7-8	W7-8				
17	W2	r5	R7-8	***				
18	C	R5	C					
19	w3	r6	w5-6					
20	W3	R6	W5-6					
21	C	r7	C					
22	w4	R7	w7-8					
23	W4	r8	W7-8					
24	C	R8	***					
25	r5	w5						
26	R5	W5						
27	C	w6						
28	r6	W6						
29	R6	w7						
30	C	W7						
31	r7	w8						
32	R7	W8						
33	C	***						
34	r8							
35	R8							
36	C							
37	w5							
38	W5							
39	C							
40	w6							
41	W6							
42	C							
43	w7							
44	W7							
45	C							
46	w8							
47	W8							
48	***							

DRAM chips, you'll need two ticks to read the next DRAM page for noninterleaved organizations, and one tick for interleaved. (The interleaved cases burst in one tick because they can initiate the access for subsequent data concurrently with an ongoing data transfer.)

The memory dialogues for the 80486 burst transfer in each of the cases are shown in table 4. The results show that the most efficient and practical memory architectures for supporting burst transfer are the 64-bit or 32-bit interleaved (pseudo 64) organizations.

How to Improve Performance

The examples above clearly illustrate that memory performance is too much a

function of application requirements and controller design to be easily improved with a quick fix, such as increasing word width. If you want a 32-bit memory interface on a 32-bit machine, then you must compromise subword access, such as byte moves, by creating a memory organization that hampers such operations. Or you have to create elaborate, sophisticated control structures, which are expensive and space-consuming. And even these have performance drawbacks: Case 8 in the simulation, for all its apparent advantages, would be crippled by a simple byte operation with an 8-byte offset.

The best solution may lie in changing the design of DRAM. If a small SRAM were integrated right into the DRAM chip and used as a high-speed cache, the result would be substantially better than separate DRAM/SRAM arrangements. Thousands of bytes of data could be burst from the DRAM to the on-chip cache in a single cycle, and write operations would be easier. The reason for this bears some explaining.

In every DRAM component, a few hundred to a few thousand bits are retrieved with every access. Most of the bits, of course, are ignored. At present, few systems take advantage of this very wide data word, and only the video RAM implementation of dynamic memory uses it to solve a specific problem. How does this wide data word work? Figure 2 shows a conceptual representation of a 1-megabit by 1-bit DRAM.

The number of bits actually accessed

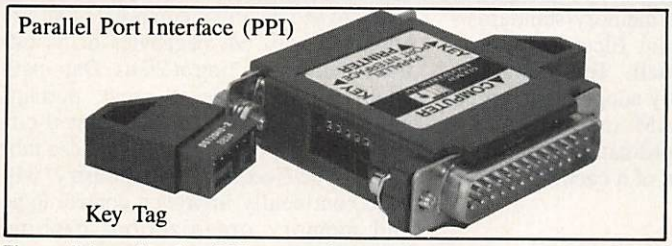
continued

Table 4: *These results show that the most efficient and practical memory architectures for supporting burst transfer are the 64-bit or 32-bit interleaved (pseudo 64) organizations (cases 6, 7, and 8).*

80486 BURST TRANSFER

Tick	Case 1	Case 2	Case 3	Case 4	Case 5	Case 6	Case 7	Case 8
1	r1	r1	r1-2	r1-2	r1-4	r1-4	r1-4	r1-4
2	R1	R1	R1-2	R1-2	R1-4	R1-4	R1-4	R1-4
3	r2	R2	r3-4	R3-4	r5-8	R5-8	R5-8	R5-8
4	R2	R3	R3-4	R5-6	R5-8	R9-12	R9-12	R9-12
5	r3	R4	r5-6	R7-8	r9-12	R13-16	R13-16	R13-16
6	R3	R5	R5-6	R9-10	R9-12	***	***	***
7	r4	R6	r7-8	R11-12	r13-16			
8	R4	R7	R7-8	R13-14	R13-16			
9	r5	R8	r9-10	R15-16	***			
10	R5	R9	R9-10	***				
11	r6	R10	r11-12					
12	R6	R11	R11-12					
13	r7	R12	r13-14					
14	R7	R13	R13-14					
15	r8	R14	r15-16					
16	R8	R15	R15-16					
17	r9	R16	***					
18	R9	***						
19	r10							
20	R10							
21	r11							
22	R11							
23	r12							
24	R12							
25	r13							
26	R13							
27	r14							
28	R14							
29	r15							
30	R15							
31	r16							
32	R16							
33	***							

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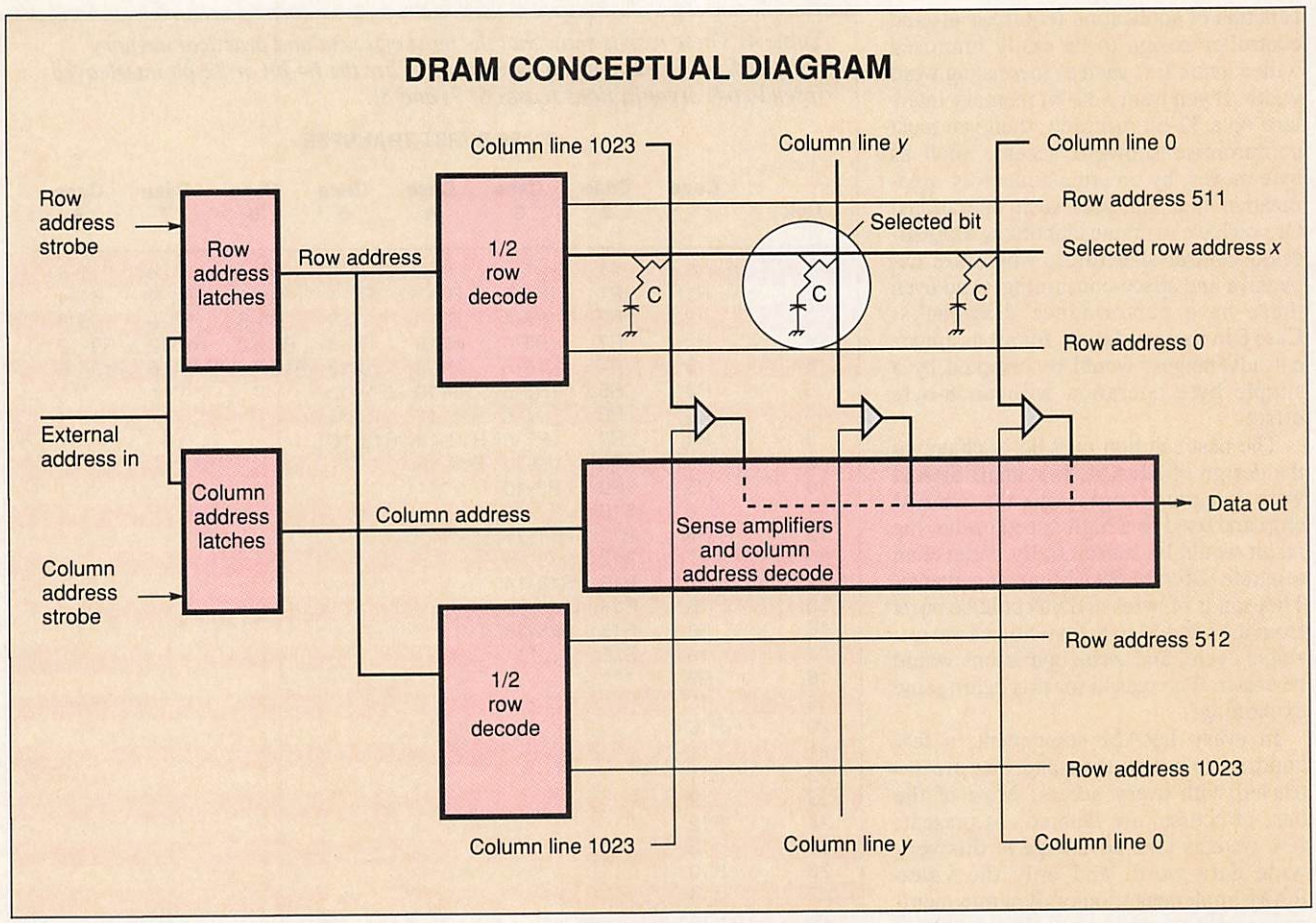


Figure 2: *A conceptual representation of a 1-megabit by 1-bit DRAM. A major access starts by presenting a row address on which a single row line is decoded. The active row then electrically connects 1024 capacitors to their respective column lines. Sense amplifiers ascertain the intended logic level for each of the 1024 columns and then latch the result. Because this process depletes the charge within each bit capacitor on reading, the row must then be rewritten.*

inside memory chips is even greater in wide memory organizations. A 32-bit memory system reads 32,768 bits, or 4096 bytes, at a time! If an SRAM were integrated at this stage, the interconnection between main memory and the cache would be extremely wide. A single cache line would be thousands of bytes long and could be loaded or swapped out in one DRAM cycle. Cache management for write operations, including avoiding stale data when multiple copies of an address exist within the system, would be easier and faster to perform.

The raw ingredients are now present within DRAMs to integrate a cache; all that would have to be added is 4K bits (4 rows) of high-speed SRAM and a few pins. This scheme is not impossible: One large DRAM supplier is considering it for a 4-megabit chip. In fact, the obstacles to achieving the caching DRAM are more political than technical. If each DRAM supplier should implement a different solution to the component, large manufacturers would shun the devices. Prices would be high, and each implementation would be a critical, sole-source component. Manufacturers avoid single-source components at all costs.

Fortunately, there is an industry committee that defines memory standards—JEDEC, or the Joint Electrical Device Engineering Council. Ten years ago, JEDEC successfully adopted and propagated the x4 DRAM standard; now it should work on coordinating suppliers in the standardization of a caching DRAM design.

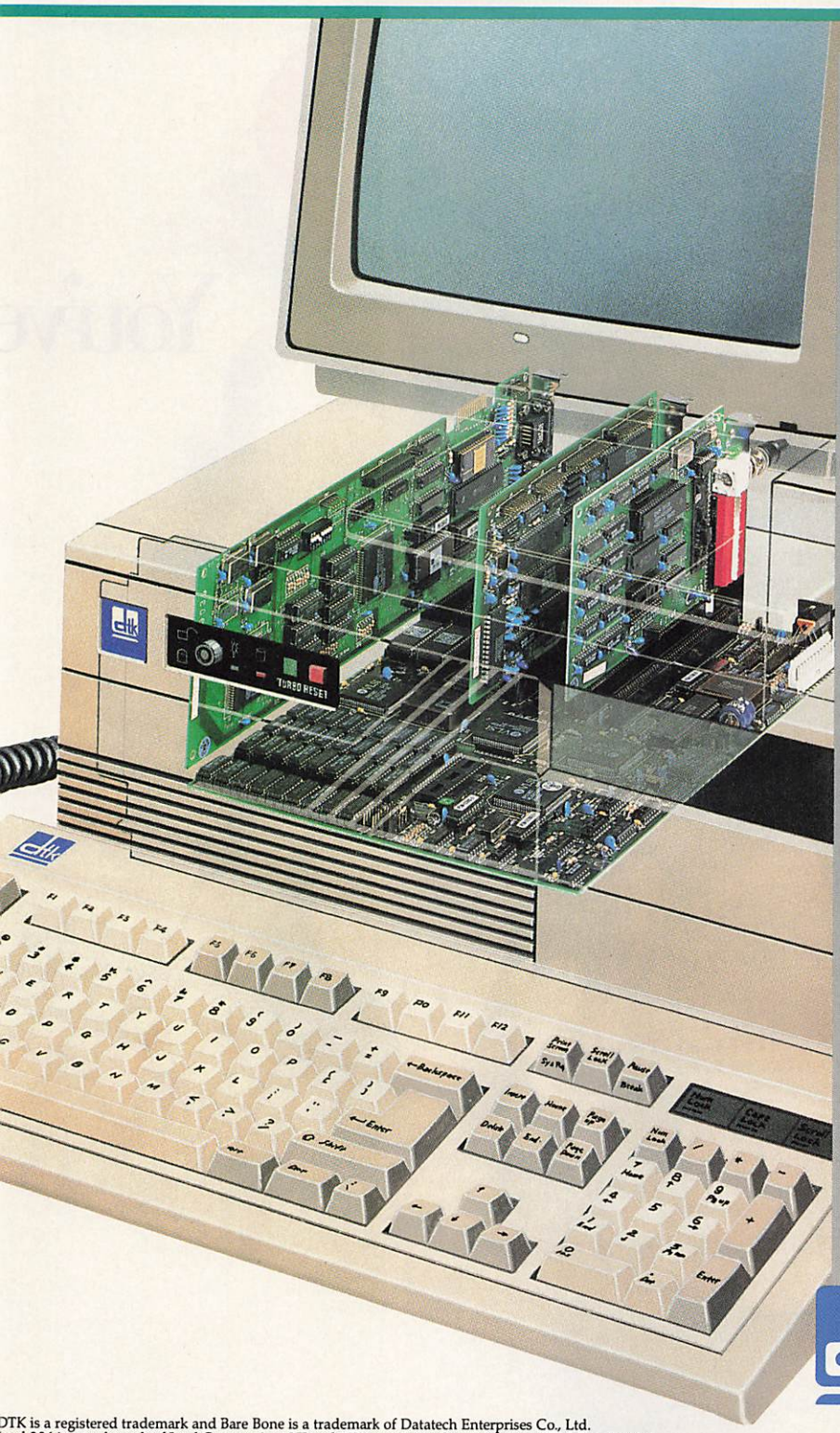
What the Future Holds

The pace of development in the computer industry makes predictions approximate, at best. After all, just a little more than 20 years ago, mainframes such as the IBM System/360 Model 50 (a medium- to large-scale member of the 360 product line) had a basic storage of 64K bytes (with a maximum of 512K bytes), a memory cycle time of 2000 ns, and a memory width of 32 bits (the same as the 80386 or 80486).

Processor speed improvements have placed greater and greater demands on main storage and will continue to in the future. Within the next 10 years, you're likely to see personal computers that are equipped with 64 megabytes of 64-bit-wide memory cycling at 20 ns. Data-path width will continue to grow, perhaps more so in silicon than on printed-circuit-board copper. To achieve these fabulous specifications, the industry will need continually improved control logic and memory organization, caching DRAM and multiple row accessing, and, most of all, coordination and standardization among suppliers. ■

Ron Sartore is the president of Cheetah International, a computer systems design and manufacturing company. He received his B.S.E.E. from Purdue University. You can contact him on BIX c/o "editors."

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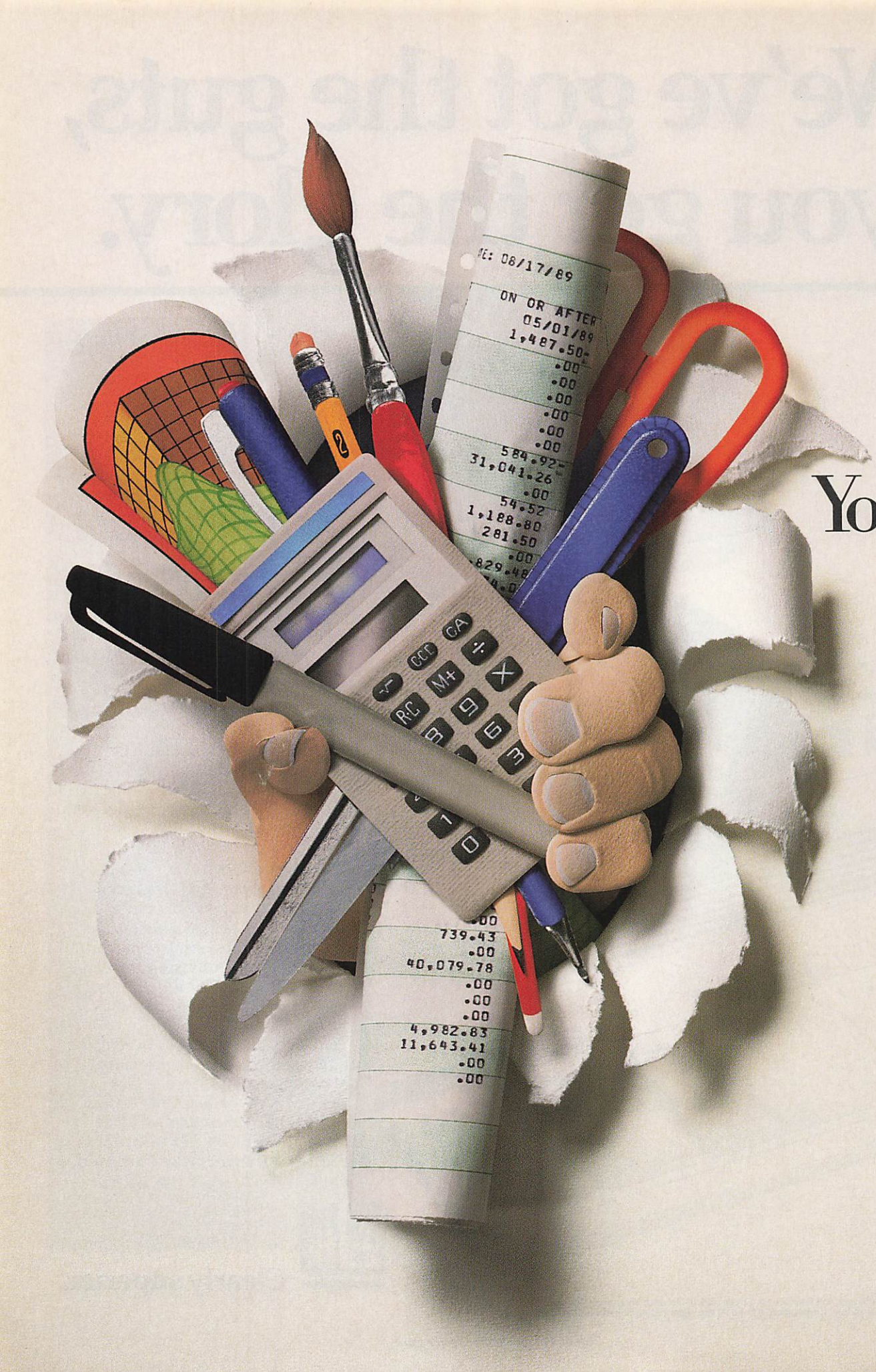
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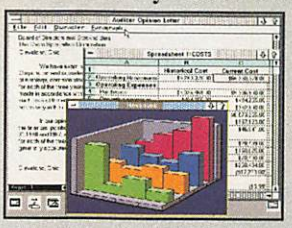
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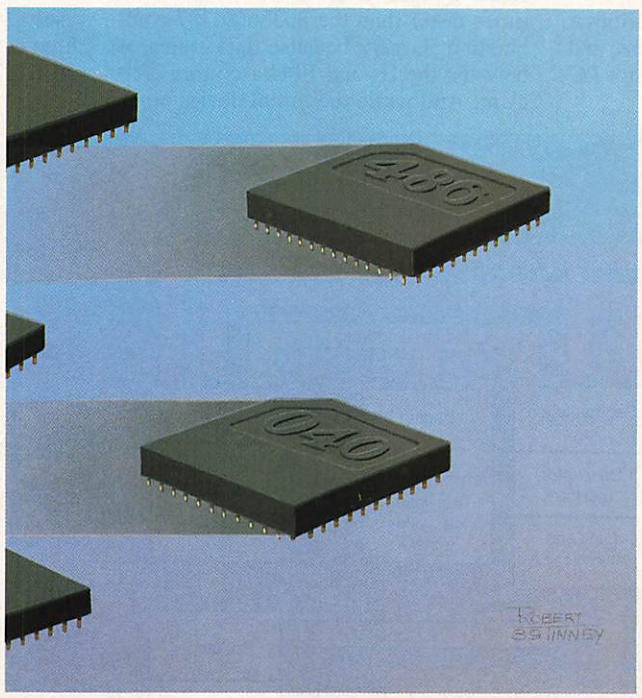
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Revenge of the CISCs

Will the 80486 and the 68040, heirs to the dynasties built by Intel and Motorola, slow the RISC bandwagon?

Michael Slater and John H. Wharton



The first commercial microprocessors contained thousands of transistors; the 8086 and the 68000, tens of thousands; and the 80386 and the 68030, hundreds of thousands. The logical next step is millions, and indeed the 80486 and the 68040 weigh in with over a million transistors each.

The increased complexity of each generation has allowed word widths to expand from 4 bits to 32 bits, and addressing ranges to jump from a few kilobytes to 4 gigabytes. Memory management units, included in more recent generations of microprocessors, have eased the implementation of multiuser, multitasking operating systems and virtual memory. For the most part, however, until the most recent generation of microprocessors, you needed external chips for cache memory and floating-point processing.

Now, for the first time, it's possible to build a complete, high-performance CPU with floating-point and memory management functions on a single chip. The first microprocessors of this latest generation are Intel's 80860 and 80486 and Motorola's 68040. The 80860 is Intel's first true RISC processor, and while it has an intriguing architecture, it's too new to have much of a software (or hardware) base.

This article will focus on the 80486 and 68040, the heirs to the dynasties built by Intel and Motorola. These chips are very similar in terms of general features (e.g., cache, memory management, pipelining, and burst-mode bus), although they execute different instruction sets and thus have different application software bases.

As of this writing, Intel had shipped some samples of the 80486, but Motorola was still awaiting the first 68040. Intel had released full details on the 80486, while Motorola had issued only general information about the 68040. Thus, this article covers the 80486 in much more detail simply because little information about the 68040 was available.

The Intel 80486

Contained in the 80486 are a highly optimized integer unit compatible with the 80386, an FPU compatible with the 80387, a complete virtual memory management and protection system, 8K bytes of unified program and data cache, bus snooping and other multiprocessing support hooks, and several minor additions to the family architecture and instruction set (see figure 1). The die measures 619 by 414 mils using 1-micron high-speed CMOS technology, and it contains 1.18 million transistors, edging out the short-lived record of 1 million in the 80860.

continued

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Intel claims that performance of the 80486 at 25 MHz will be about 37,000 Dhrystones, 6.1 million Whetstones (double-precision), or performance relative to the VAX 11/780 of about 15 to 20 VAX MIPS. This places the microprocessor squarely in competition with many RISC chips. Samples of 25-MHz chips have already been distributed, and Intel promises 33-MHz and 40-MHz versions to follow in 1990.

The 80486 implements essentially the same instruction set, memory organization, programming model, process-management facilities, and so forth as the original 80386, although the 80486 significantly outperforms its predecessors. Intel made no significant changes to the 80386 architecture except for six new instructions required for cache support and multiprocessing functions.

The 80486 appears to have been designed with four key objectives:

- Remain 100 percent software-compatible with existing 80x86 processors;
- Improve the performance of existing programs by 2 to 4 times;
- Add hardware and software facilities to support multiprocessing applications; and
- Increase the level of integration for PC-class systems.

Why didn't Intel reopen the architecture to add a slew of new instructions or to revise the programming model? Because the plan for the 80486 is to cement the 80386 family's domination of the personal computer industry. By retaining the same programming model for the 80386 and 80486 CPUs, Intel can promise third-party software developers a consistent programming environment on computation engines spanning a wide price/performance range. Intel hopes that the new product announcements will ensure that all future high-end PC software will be targeted to the 80386/80486 family, relegate the 80286 and its predecessors to lower status, and shut out the various "upstart" RISC builders.

Meeting Performance Goals

The 80486's claimed performance enhancement of 2 to 4 times that of the 80386 results from several factors. The fully redesigned integer unit (IU) and on-chip cache reduce the average number of clock cycles per instruction by a factor of about 2.5. The on-chip FPU executes floating-point instructions about three times faster than the 80386/80387 combination, largely because data transfers between the IU and FPU are more efficient. And while the initial device clock speed is 25 MHz, the 80486 is designed to scale to clock rates higher than those that the 80386 can achieve.

The instruction execution unit is designed to process loads, stores, and simple integer operations (i.e., those present in most RISC architectures) in as few clock cycles as practical. Less commonly encountered operations, such as multiplication, division, and process-context switches, received less design attention and require essentially the same number of clock cycles as—and occasionally more than—they do on an 80386.

If cache alignment and system timing conditions are propitious, data loads, stores, and simple register-to-register arithmetic operations do indeed complete in a single clock cycle (see table 1). There are no load-delay slots; the instruction immediately following a load can use the newly loaded data with no pipeline stall. No RISC machine has yet achieved this feat.

Arithmetic operations that implicitly reference memory-based variables need an extra clock cycle to retrieve data from the cache; operations that store computed results back in memory generally take three clock cycles total, as would a simple RISC load/operate/store instruction

continued

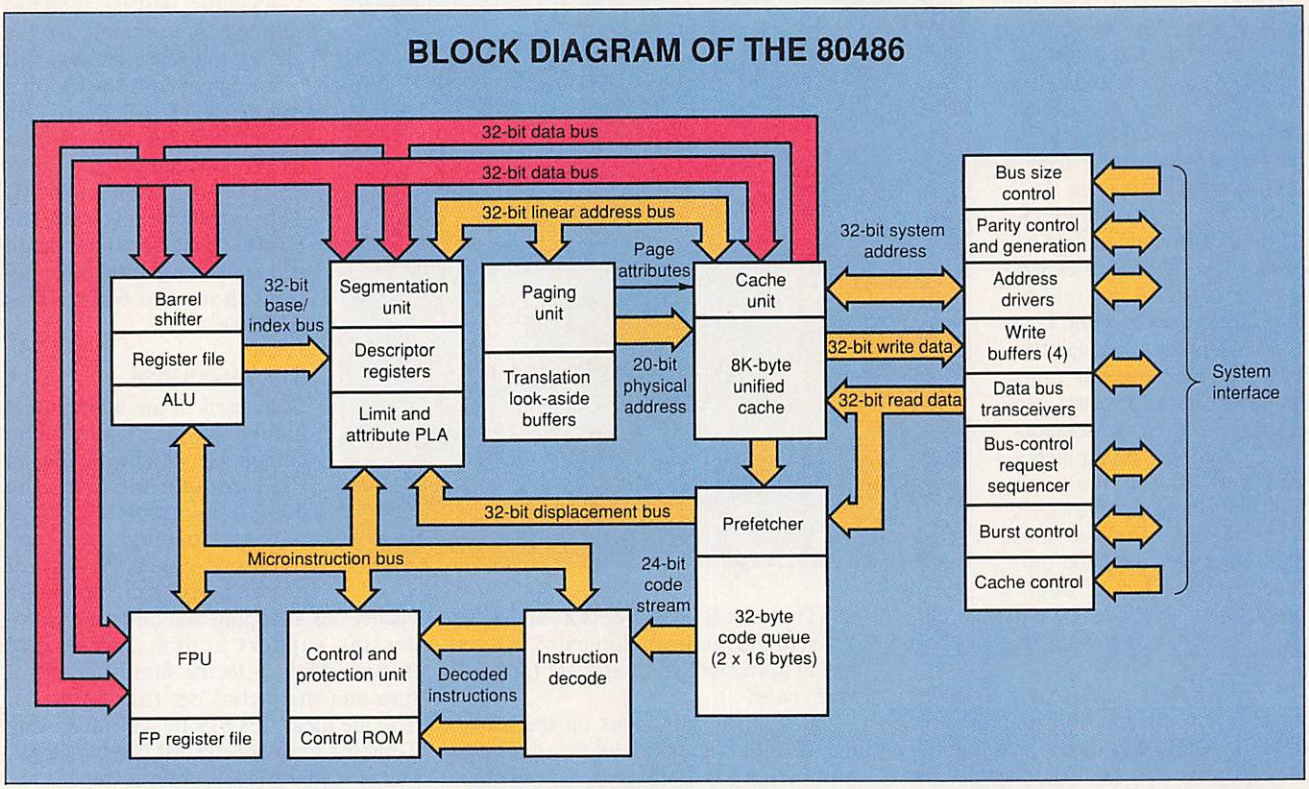


Figure 1: *The 80486 chip uses 1-micron high-speed CMOS technology and contains 1.18 million transistors. Its performance relative to a VAX 11/780 will lie between 15 and 20 VAX MIPS.*

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Table 1: *If cache alignment and system timing conditions are just right, data loads, stores, and simple register-to-register arithmetic operations really do complete in one clock cycle on the 80486. There are no load delays; the instruction immediately following a load can use the new data immediately. (N/A = not applicable.)*

INSTRUCTION EXECUTION TIME COMPARISON

Instruction	Optimum number of clock cycles 8088/8087	80386/80387	80486
Register-to-register add	3	2	1
Memory load (16-bit)	21	2	1
Memory store (16-bit)	22	4	1
Memory-to-register add (16-bit)	22	6	2
Register-to-memory add (16-bit)	33	7	3
Integer multiply (16-bit; min.-max.)	128-154	12-25	13-26
Unconditional jump	15	8	3
Branch (taken/not taken)	16/4	8/3	3/1
Call	23	8	3
Return	20	11	5
Enter level-1 procedure	N/A	12	17
Floating-point load (64-bit)	87	25	3
Floating-point add (80-bit)	70-100	23-31	8-20
Floating-point multiply (80-bit)	130-145	29-57	16
Floating-point divide (80-bit)	193-208	88	73

sequence. The penalty on cache misses is held to two clock cycles, assuming zero-wait-state external memory.

Instruction Pipelining

Achieving this level of performance required a complex five-stage instruction-execution pipeline. The instruction fetch and alignment stage is part of a semi-autonomous prefetch unit. Instructions in the cache are retrieved 16 bytes at a time into a 32-byte instruction-prefetch queue. Instruction fields can be extracted from the queue as needed, since instructions range from 1 to 11 bytes long, not counting override prefixes.

Decoding is performed in two stages. The first stage classifies the instruction, selects the microprogram ROM entry point, and determines whether a memory reference is needed. Operand address information (if relevant) is dispatched to a separate address-calculation unit.

The op-code bits are dispatched to a second-level decoder and microcode ROM, which expands the macroinstruction into one or more fully decoded microinstructions. The ALU executes the expanded microinstructions in the fourth pipeline stage, and the fifth stage stores the computed values back to the register file. If the instruction requires a memory update, it needs an extra clock cycle to transfer the destination address and data to the data cache or bus interface logic.

The first decode stage detects any branch instructions and initiates a speculative prefetch of the destination op code. The branch op code isn't interpreted until the execution stage, so a two-clock-cycle pipeline delay occurs when a branch is taken. If a conditional branch is not taken, instruction execution continues from the original prefetch point, incurring no additional delay.

To further enhance performance, the 80486 contains an intricate system of ALU and register-file bypass gates. Hard-wired comparators detect whether either of an instruction's source operands comes from a register that the preceding instruction has modified or loaded. If so, the ALU output bus or register-file input bus is routed directly to the appropriate ALU input. This eliminates the clock cycle that moving the data through the register file would otherwise have consumed. (Many RISC designs also use this same technique.)

Unlike RISC processors such as the 88000, the 80486 doesn't implement register scoreboarding. When conditions aren't right for immediate instruction completion, the entire ALU pipeline stalls. Existing 80x86 programs tend to use each memory operand immediately after it's loaded or retrieve it as part of the instruction it's used in. In such cases, register scoreboarding would simply stall the ensuing instruction anyway.

The 80486 also doesn't use branch delay slots or conditional-branch prediction clues. The existing 80x86 software base doesn't use these techniques either, since neither one had entered microprocessor-design methodology 12 years ago when the 8086 architecture was defined.

Cache Characteristics

The on-chip cache is fundamental to achieving the high performance level of the 80486. Although the cache is considerably smaller than the 32K-byte external caches built with the 82385 in many 80386-based PCs, it's considerably more sophisticated. Its line size is 16 bytes, rather than 4 bytes, and its organization is four-way set associative, not two-way. Wide buses from the cache let the instruction prefetcher grab blocks of code 16 bytes at a time. Cacheable memory reads always fill an entire cache line, using an optimized four-word burst transfer.

In contrast to most processors with on-chip caches, the 80486 cache is unified to hold both code and data. This generally provides more efficient cache utilization than would, for example, separate 4K-byte code and data caches. It also solves problems that might otherwise arise in executing application programs that include self-modifying code, a questionable programming technique that is used by some significant DOS software. Cache addresses are physically mapped.

The most-often cited disadvantage of a unified cache design is that code and data fetches can collide, stalling instruction execution. The 80486 prefetch system avoids this hazard in two ways. Prefetching instructions 16 bytes at a time reduces the frequency of collisions; and, when collisions do occur, the data request is serviced first. The execution unit can generally keep busy finishing instructions already in the prefetch queue. (For more details on the inner workings of the 80486's cache, see the text box "Caching In" on page 328.)

Cache Effects on Bus Operation

The 80486 is the first microprocessor to include an on-chip cache with complete bus-snooping logic. The inclusion of these functions causes a considerable change in the nature of the memory interface, and the 80486 bus structure is thus quite different from that of the 80386.

The inclusion of caches on any microprocessor leads to a curious reversal in the nature of the traffic on the external bus. In noncached systems, most of the activity on the external bus involves pro-

continued

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Caching In

Intel projects cache hit rates for the 80486 of 96 percent for DOS applications and 92 percent for Unix and OS/2 applications. (These estimates are from trace-driven simulations, not measurements, but are presumably close to what typical real values will be.) Thus, the number of read cycles that appear on the external bus is drastically reduced, and write cycles dominate bus activity.

When a cache miss occurs on a read cycle, the 80486 fills an entire four-word (16-byte) cache line. Thus, most memory-read cycles are four-word bursts. Single-word reads occur only for noncacheable areas and for input ports. (Accesses to the I/O address space are never cached.)

To support cache refills efficiently, the 80486 bus interface provides a special burst mode, but this is activated only when the system logic requests it. The processor indicates the start of the cache fill by asserting ADS# and providing the address of the first word. The system logic responds by asserting KEN# (cache enable) if the access is to a cacheable location. KEN# is then checked by the processor in the first cycle to determine whether or not to perform a four-word transfer.

The 80486 also provides cacheability control in the page table, but existing operating-system software doesn't support these bits. Systems designed with the 80386 and 80385 cache controller decode noncacheable regions in external hardware, and the KEN# input lets the 80486 use this same mechanism.

Figure A shows the timing for a maximum-speed burst transfer. This four-word transfer requires only five clock cycles, as compared to eight cycles for the fastest possible nonburst cache-line fill. The system logic indicates that it can perform a burst transfer by asserting BRDY# (burst ready). The processor then performs successive transfers as fast as one per clock cycle. Just as in regular transfers, wait states can be added to transfers within the burst by delaying the assertion of BRDY#.

The 80486 asserts (sets low) the BLAST# (burst last) signal during the last cycle of the burst and during nonburst (single-word) accesses to indicate to external logic that the processor isn't ready to begin a burst cycle. You can also think of BLAST# as "ready to burst." It is high whenever the processor is ready to perform a burst transfer.

Burst transfers aren't limited only to cache-line fills, and they don't have to consist of four transfers. The 80486 will offer to perform a burst transfer (by negating BLAST#) whenever it's reading 64 bits or more of data (e.g., a 64-bit floating-point read). If the addressed device asserts BS8# or BS16#, the processor performs the required number of transfers in a single burst. For example, a cache-line fill from a 16-bit device produces a burst of eight 16-bit words.

Burst-mode transfers take advantage of the fact that both page-mode and static-column DRAMs are much faster on successive accesses within a page than on the first access. However, even successive transfers aren't fast enough with common DRAMs to keep up with the 80486's maximum rate of one transfer per clock cycle (40 ns at 25 MHz, or 30 ns at 33 MHz). The solution is to provide two interleaved memory banks. Thus, each bank needs to provide only one word every two clock cycles to maintain the maximum transfer rate.

Snooping and Cache Coherency

Caches present a potential data-coherency problem in systems using direct memory access or multiple processors. If another processor or a DMA controller writes to a location whose contents are stored in the cache, the cache copy must be invalidated. The 80486 has logic to perform this function for the on-chip cache. To make this possible, 80486 address pins are bidirectional.

Snooping is required whenever a device other than the 80486 writes to a memory location that may be in the 80486's cache. When this occurs, the system logic must generate a cache-invalidation cycle (see figure B). System logic first asserts AHOLD (address hold) to the 80486, which disables its address outputs on the next clock cycle. This differs from a normal HOLD request in that only the address bus is disabled and the request is not delayed until completion of the current bus cycle. The system logic then drives the address on the 80486's address pins and asserts EADS# (external address). The 80486 compares the supplied address to the cache tags and, if there's a match, invalidates that cache line.

Normal data bus activity can continue while AHOLD is asserted. In figure B, RDY# is asserted and a word of data is read into the processor in the first cycle of the invalidate transaction.

BREQ (bus request) is an output from the 80486 that's asserted whenever the 80486 is ready to perform a bus transaction. BREQ can be used in multiprocessor systems to control access to the system bus.

Since cache-invalidate cycles require access to the cache tags, they can interfere with the processor's access to the cache. The 80486 reads code from the cache 16 bytes at a time, and these 16 bytes are fed into a 32-byte prefetch queue, so code fetches from the cache are relatively infrequent. But if the 80486 must perform a data access to the cache (or must fetch code because the prefetch queue is empty) in the same clock cycle as the invalidate request, the CPU stalls for one or more clock cycles.

In a multiprocessor system, this stalling can cause a significant degradation in performance. To minimize the degradation, you can use external logic to identify shared-memory areas and inhibit snooping on all but these areas. Second-level caches also reduce the degradation from snooping.

Second-Level Cache Support

A cache-hit rate of 92 percent may seem very good. But if the time to process a miss is very long, the misses can significantly reduce performance. For a given-speed main memory, the miss penalty (in clock cycles) increases as the processor's clock rate increases. Thus, the performance loss due to cache misses is lowest for 25-MHz systems.

Faster 80486 systems, operating at 33 MHz and eventually at 40 MHz and up, are likely to use external second-level caches, which are typically much larger than first-level (on-chip) caches. The majority of misses in the first-level cache will hit in the second-level cache, keeping the penalty for such misses to a minimum. Only when a miss occurs in the second-level cache will the 80486 need to access main memory.

The 80486 provides two signals to support a second-level cache: PWT (page write-through) and PCD (page-cache disable). These signals are copies of the corresponding bits in the page

table and allow the operating system to control cacheability on a page-by-page basis. If PCD is set, the internal cache is disabled, and a second-level cache must be disabled as well. The PWT bit has no effect on the internal cache because it's always write-through. It's provided to selectively force write-through operation on an external write-back cache.

Cache-Support Functions

Minor changes to the 80386 architecture were made to support the cache facilities. Two reserved bits of each memory-page-table entry were redefined to control cacheability characteristics on a per-page basis. When the PCD bit for a page is cleared, internal caching of data from that page is allowed. If the bit is set, internal caching is disabled. On each external memory access, the states of the PCD and PWT bits for the referenced page are copied to external pins. Off-chip logic can monitor these pins to control the write-back policy of an external second-level cache. The internal cache ignores PWT since all writes are write-through.

Two new input pins control internal cache operation. When a cache miss occurs, the 80486 tries to fetch the required data from external memory. As the data is returned, the chip tests the KEN# pin. If KEN# is negated on the first transfer cycle, the value fetched bypasses the on-chip cache and is processed directly, regardless of the state of the PCD bit. If KEN# is asserted, the memory cycle is transformed into a four-word burst transfer to fill the cache line. Asserting the FLUSH# input pin invalidates all internal cache tags.

The cache controller implements streaming and wraparound burst transfers for instructions and data. The first memory word returned contains the value needed by the unit that initiated the transfer; this value is passed to and digested by the requesting unit as soon as it arrives. The 80486 retrieves ensuing words in an order that ensures optimum use of 64-bit-wide interleaved memory systems, and it stores them temporarily into a four-word staging register. If external logic indicates that all four words fetched are cacheable, the cache is updated. Otherwise, the holding register is abandoned without affecting the cache.

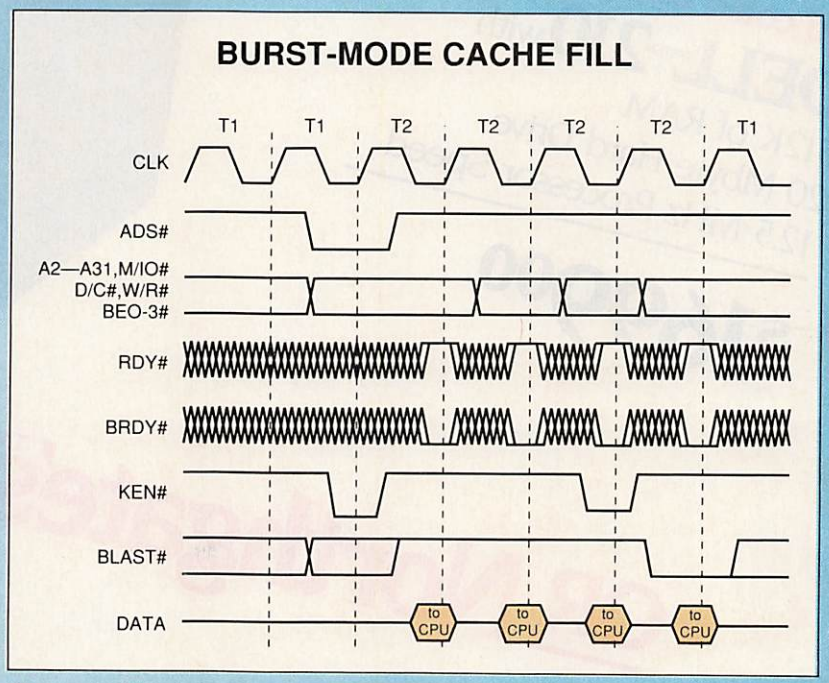


Figure A: *The timing for a maximum-speed burst transfer. This four-word transfer requires only five clock cycles; the fastest possible nonburst cache-line fill requires eight cycles.*

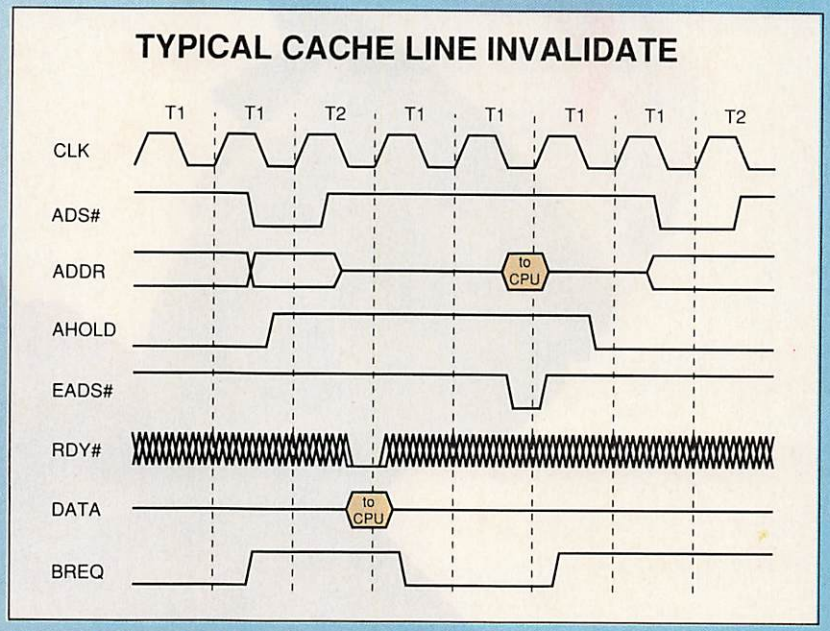


Figure B: *System logic first asserts AHOLD (address hold); then the 80486 disables its address outputs on the next clock cycle. System logic then drives the address on the 80486's address pins and asserts EADS# (external address). If the supplied address matches the cache tags, the 80486 invalidates that cache line.*

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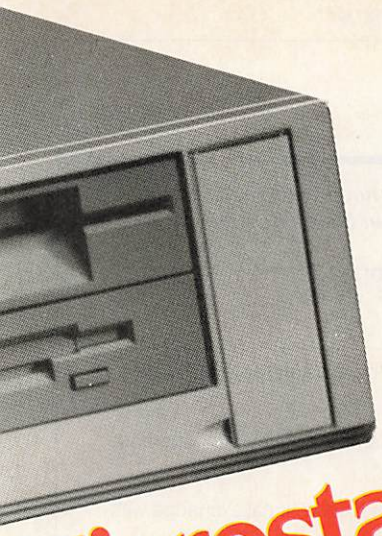
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Table 2: *The 80486 includes six new instructions not present in the 80386. The last three are new instructions to help maintain the cache state.*

80486 INSTRUCTION SET ADDITIONS

Instruction	Mode	Function
BSWAP	A/S	Swaps byte order within 32-bit register; simplifies sharing of big-endian databases.
XADD	A/S	Performs atomic exchange-and-add to memory operand; retains original value.
CMPXCHG	A/S	Performs atomic compare and conditional exchange with memory-based operand.
INVD	S	Invalidates full instruction/data cache.
WBINVD	S	Invalidates cache; signals secondary cache to write back dirty cache lines.
INVLPG	S	Invalidates matching TLB entry, if present.

A = application-level software; S = system-level software; TLB=translation look-aside buffer

gram fetches, and most of the remaining data transfers are reads. A cached system satisfies most fetch and read cycles internally, so they don't appear on the bus. All 80486 writes, on the other hand, pass through to the external bus, so the majority of the bus traffic is outbound.

To decouple write operations from the performance of external memory systems, the 80486 contains four internal write buffers. If the external bus is busy, data writes simply save their data and destination addresses in the write buffer and complete in a single clock cycle. If all four buffers are in use, the instruction stalls. (The MIPS Computer Systems R3000 family has a similar facility but requires external write-buffer chips.)

As a further performance enhancement, Intel recommends that memory systems latch the write data and address information externally and implement a delayed write-memory cycle to free up the address and data buses as quickly as possible.

New Instructions

The 80486 includes six new instructions that are not present in the 80386 (see table 2). Three new protected-mode instructions help maintain the cache state: INVLPG (invalidate the translation look-aside buffer [TLB] entry), INVD (invalidate data cache), and WBINVD (write back and invalidate data cache). The latter two are identical from the 80486's perspective, since the on-chip cache never contains dirty data to be written back. The only difference between them is that the second form asserts an output signal to control optional external write-back caches.

Two previously reserved bits in control register 0 have been defined to globally enable the cache replacement and write-through facilities. Three new 32-bit test registers have also been added, to let the operating system test operation of the cache tag and data memory blocks.

Two new instructions support multiprocessing systems. The CMPXCHG (compare and exchange) and XADD (exchange and add) instructions perform atomic memory read/modify/write cycles and simplify the implementation of software semaphores in multiprocessing applications.

The sixth new instruction, BSWAP (byte swap), reverses the byte order of a 32-bit operand. This lets the 80486 share data structures and on-line databases more easily with big-endian processors, such as the 680x0 and IBM mainframes, in coprocessing systems and networked installations. It will also be a boon to the execution of programs written in COBOL, still the most widely used of all computer programming languages. COBOL uses big-endian data structures and binary coded decimal (BCD) strings throughout. (You can use the original 8086 XCHG instruction to reverse the order of 2-byte operands.)

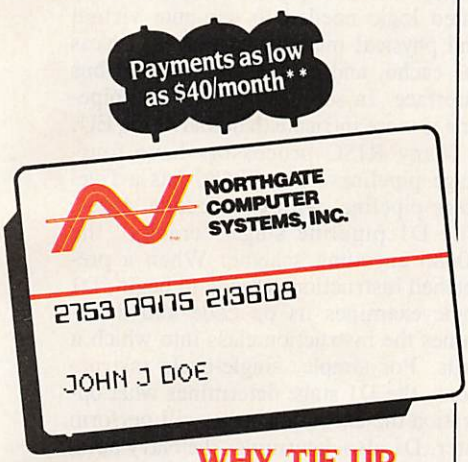
Pipeline Operations

In most RISC microprocessors, each pipeline stage is tightly coupled to its

continued

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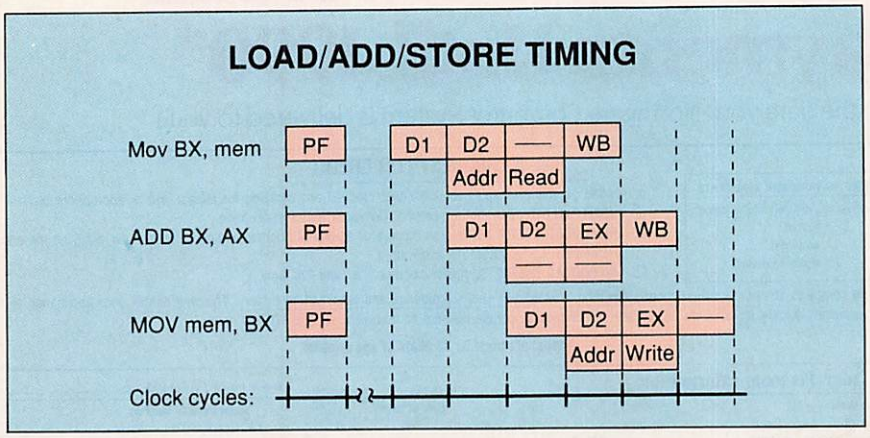


Figure 2: *The pipeline stages for a series of three single-cycle instructions. The first is a simple load from memory and assumes a cache hit; the boxes below the D2 and EX pipeline stages show the actions of the EU and cache logic during each clock cycle. The second instruction performs a register-to-register add, using the just-loaded data, and the third stores the result back to the same memory location. Note that all three instructions are prefetched together, and that each spends a single clock cycle in each of the other pipeline stages.*

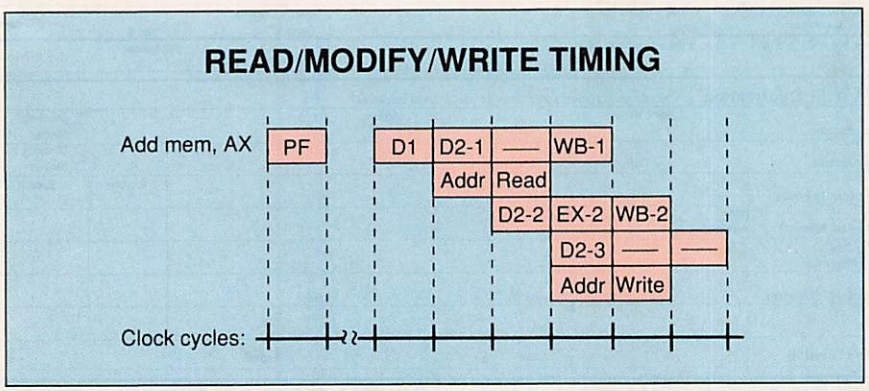


Figure 3: *A register-to-memory add instruction equivalent to the sequence in figure 2. While this form takes the same number of clock cycles to complete, it requires 4 instruction bytes instead of 10 and doesn't corrupt a temporary register.*

neighbors. With few exceptions, each instruction spends exactly one clock cycle in each stage. So in a system with a four-stage pipeline, most instructions complete in four clock cycles total. One instruction enters and another instruction exits the pipeline during each clock cycle.

Exceptional conditions cause the entire pipeline to stall until the condition is corrected. The simplified nature of a RISC instruction set and the uniform instruction encoding that this allows are what make it possible to overlap instruction execution so efficiently. The difficulty of fitting complex instructions into a highly regular pipeline has been a key justification for removing certain instructions from traditional RISC architectures.

The 80486 design extends the concept of pipelining in several ways. For one thing, the main execution unit (EU) pipeline expands to five stages: prefetch (PF), two decode stages (D1 and D2), execution (EX), and register-file write-back (WB). For another, the simple lock-step progression of instructions through a typical RISC pipeline has been made far less restrictive. "Slip-joints" between pipeline stages can in some cases let ensuing stages advance while blocking earlier stages.

The PF stage typically retrieves four or more instructions at a time, several clock cycles before any of them begin executing. While single-cycle instructions pass through the pipeline much as they would through conventional RISC designs, more complex instructions can consume a varying number of additional clock cycles in each stage. Interstage interlocks prevent each stage from advancing unless ensuing stages will be ready to absorb the resulting data when it arrives.

Furthermore, the 80486 operates a second, two-stage data retrieval pipeline in parallel with the decode and execution stages. The data pipeline contains dedicated logic needed to compute virtual and physical memory addresses, access the cache, and control the external bus interface. In some ways, the data pipeline is more intricate than that of the EU.

Many RISC processors have four-stage pipelines. The 80486 has a five-stage pipeline, with two decode stages. The D1 pipeline stage "cracks" the 80486 encoding scheme: When a prefetched instruction is ready to begin, D1 logic examines its op code and determines the instruction class into which it falls. For simple, single-cycle instructions, the D1 stage determines what operation the execution stage will perform later. D1 also determines the entry point within a microinstruction ROM that contains the control word for the first execution cycle. If the instruction requires a memory-address calculation, the D1 stage also retrieves the information needed to compute the address and passes it on to the segmentation unit.

The D2 stage expands each 80x86 macroinstruction into control signals for the ALU. For single-cycle macroinstructions, this is simply a function of the original op-code bits. The D2 stage also controls the computation of the more complex addressing modes.

During the EX stage of the 80486 pipeline, the ALU in the IU performs calculations appropriate to the instruction. Unlike a conventional RISC pipeline, the 80486 may take up to several dozen EX clock cycles to execute a complex macroinstruction or to manipulate complex data structures. In such cases, a conventional microcode engine controls the ALU. In other cases, such as memory loads and stores, the ALU remains idle.

Finally, the WB stage, if needed, disposes of the register data and status flags modified during the preceding EX stage. If the current instruction updates memory, the computed value is sent to the cache and to the bus-interface write buffers at the same time. If a hit occurs, the cache is updated immediately so as not to slow down the execution unit; bus-write cycles can safely be deferred until the bus becomes available later. Figure 2 shows the pipeline stages for a series of three single-cycle instructions: load, add, and store.

The 80486's nonreduced instruction set also supports a full range of opera-

tions that reference memory-based operands as their source or destination. Figure 3 shows a register-to-memory add instruction equivalent to the sequence shown in figure 2.

For optimum performance, 80486 programs should follow the same data alignment guidelines recommended for 80386 systems. Specifically, 32-bit (or smaller) data objects should reside within a single 32-bit word. If a data object isn't properly aligned, control logic immediately initiates two successive access cycles. This simplifies the cases in which the object is split between separate cache lines or when it combines cached and noncached data.

Unaligned references still work, but at the expense of three extra stall cycles as the second access is performed and mated with the first. (To optimize the execution of virtual-mode 8086 programs, unaligned 16-bit data objects that fit within a 4-byte address boundary don't incur this penalty.) If any part of a requested data object isn't present in the cache, control logic will initiate an external memory-read cycle and insert stall cycles as needed.

Refilling the Prefetch Buffers

As sequential instruction execution proceeds, each half of the prefetch queue periodically becomes empty. Prefetch logic attempts to refill empty buffers with the next sequential instruction block. If the required instructions are in the cache, the buffer will be refilled in one clock cycle.

If the cache misses, prefetch logic requests a burst of instruction fetch cycles from external memory. In the meantime, the EU can generally keep busy for a handful of clock cycles—Intel says about eight—processing instructions that remain in the alternate prefetch buffer. External prefetches are performed in ascending order, with each word copied both to the prefetch buffer and to the cache as it's received. Thus, performance is minimally impaired, even for external prefetches.

The instruction pipeline unit monitors its own copy of the code-segment limit register. Prefetch cycles that would exceed the limit are automatically suppressed, so as not to reference nonexistent memory. Attempted branches past the end of the code segment produce limit-check errors.

80486 Pin Functions

Figure 4 shows the 80486 pin functions. The 32-bit address bus is implemented as 30 address bits, plus four byte enables

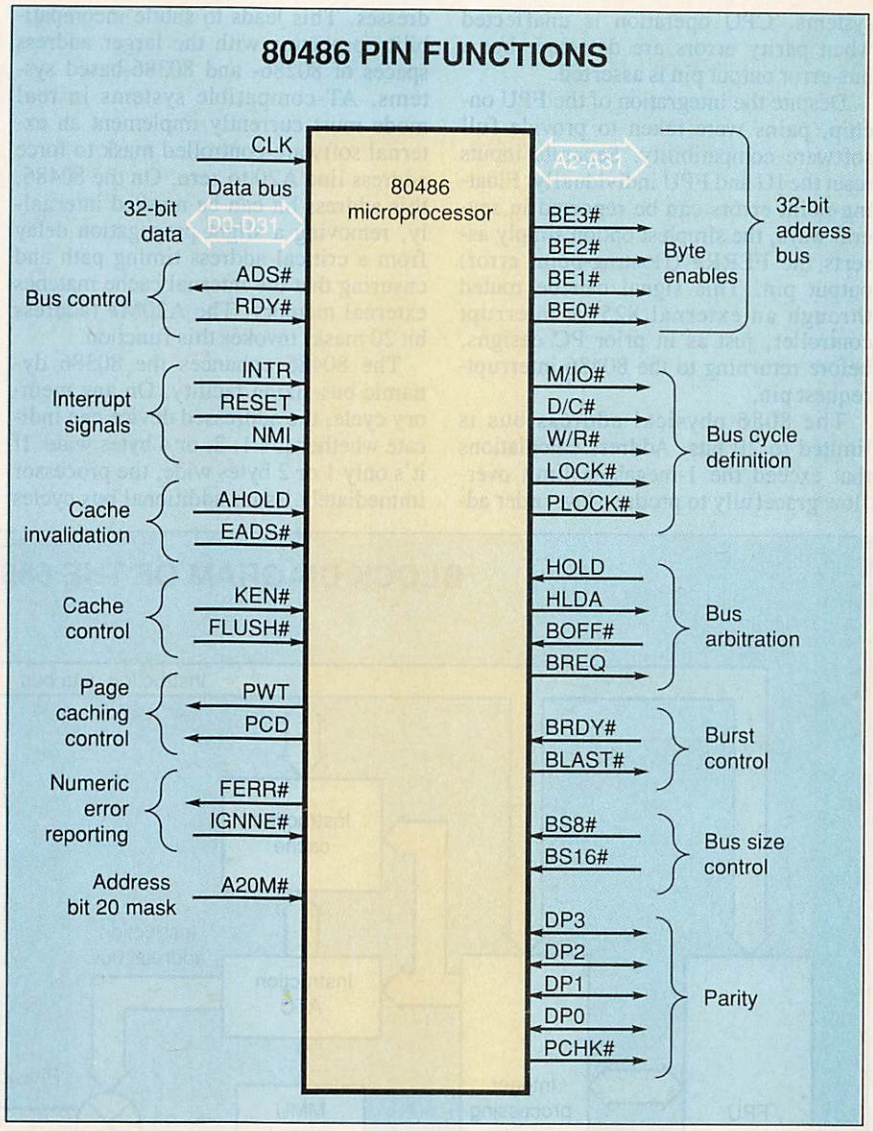


Figure 4: *The 32-bit address bus is implemented as 30 address bits, plus four byte enables that encode the two least-significant address bits and the transfer width. Many of the control signals and inputs are similar to their 80386 counterparts.*

that encode the two least-significant address bits and the transfer width. Many of the control signals, including M/IO# (memory/IO), D/C# (data/control), W/R# (write/read), RDY# (ready), LOCK#, HOLD, and HLDA (hold acknowledge) are similar to their 80386 counterparts, as are the RESET, NMI, and INTR inputs. The 80386 provides dynamic bus sizing for 16-bit devices via the BS16# (bus size 16 bits) signal; the 80486 adds a BS8# (bus size 8 bits) signal as well, to support byte-wide devices. The remainder of the signals represent new features in the 80486.

Intel processors have historically required an external clock that is two or more times faster than the processor's internal clock. The 80486 implements a single-phase clock, so the internal and external clocks have the same frequency. This technique, first tested by Intel with the 80860, should simplify system design and may make it easier to meet FCC emissions standards.

PC Integration Improvements

A number of 80486 bus-interface facilities simplify the design of IBM-style PCs and workstations. An extra pin for each byte of the data bus produces and verifies bus parity. This eliminates the need for off-chip parity logic, saving money and, more important, reducing delays in the critical timing path of external memory

continued

systems. CPU operation is unaffected when parity errors are detected, but a bus-error output pin is asserted.

Despite the integration of the FPU on-chip, pains were taken to provide full software compatibility. Separate inputs reset the IU and FPU individually. Floating-point errors can be reported in several ways; the simplest option simply asserts the FERR# (floating-point error) output pin. This signal can be routed through an external 8259A interrupt controller, just as in prior PC designs, before returning to the 80486 interrupt-request pin.

The 8086 physical address bus is limited to 20 bits. Address calculations that exceed the 1-megabyte limit overflow gracefully to produce low-order addresses. This leads to subtle incompatibility problems with the larger address spaces of 80286- and 80386-based systems. AT-compatible systems in real mode must currently implement an external software-controlled mask to force address line A20 to zero. On the 80486, this address bit can be masked internally, removing a slight propagation delay from a critical address timing path and ensuring that the internal cache matches external memory. The A20M# (address bit 20 mask) invokes this function.

The 80486 enhances the 80386 dynamic bus-sizing facility. On any memory cycle, the addressed device can indicate whether it's 1, 2, or 4 bytes wide. If it's only 1 or 2 bytes wide, the processor immediately issues additional bus cycles as needed to retrieve any required higher-order bytes. This lets the 80486 boot itself from a single byte-wide EPROM, simplifies peripheral interfacing, and eliminates the external state machine required to perform byte-wide transfers on the XT, AT, and Micro Channel buses.

The four parity bits, DP0 through DP3, serve as inputs on read cycles and as outputs on write cycles. If parity is incorrect on a read cycle, PCHK# (parity check) is asserted. This doesn't affect the operation of the processor in any way; systems that use parity will normally connect PCHK# to NMI. PCHK# isn't valid until the clock cycle that follows the end of the read cycle. Because of the cache operation and instruction prefetching, bus activity is quite decoupled from

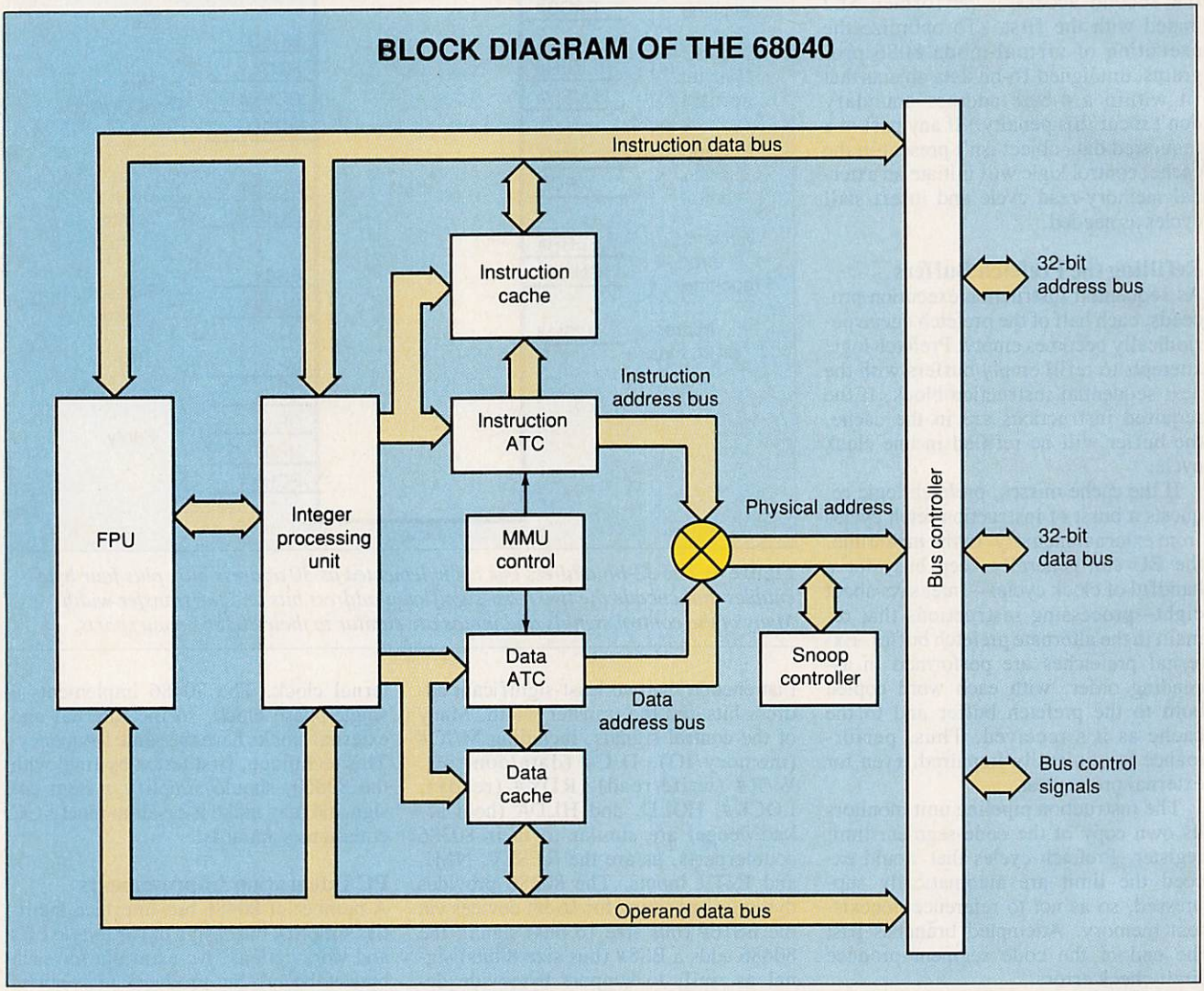


Figure 5: *The instruction unit of the 68040 executes the same instruction set as the 68030, with perhaps a few additions to support new hardware features. The implementation is completely new, however, with a redesigned ALU and pipeline to decrease the average number of clock cycles required per instruction. The design increases the size of on-chip caches from 256 bytes to 4K bytes each and integrates the FPU onto the chip.*

instruction execution, and it's difficult to correlate the parity error with the instruction that caused it. An external address latch can be added to capture the address for diagnostic purposes.

The Motorola 68040

The 68040 will contain over 1.2 million transistors, making it about the same size as the 80486. Motorola says that it will be 100 percent compatible with existing 68000-family processors. No specific performance figures have been released, but the chip is said to operate at roughly three times the rate of the 68030. Its floating-point performance is expected to be significantly faster than the 80486's.

Figure 5 shows the block diagram of the 68040. The IU must execute the same instruction set as the 68030, with perhaps a few minor additions to support new hardware features. The implementation, however, is entirely new, with a redesigned ALU and pipeline designed to significantly decrease the average number of clock cycles per instruction. Motorola's "Product Preview" states that the IU has been "optimized to significantly reduce the execution time of compiler-generated code." This presumably means that the simpler instructions, which most compilers tend to use, will be sped up the most.

The FPU is compatible with the 68882 coprocessor, but the trigonometric functions aren't directly supported. Instead, they are trapped and must be emulated in software. These functions were performed in microcode in the 68882, and since the 68040 will be able to execute simple macroinstructions in a single clock cycle, software emulation may be comparable in speed to a microcode implementation. The basic floating-point functions that the FPU implements in hardware will operate in fewer clock cycles than the 68882 required, providing very good floating-point performance.

The on-chip memory management unit is a superset of that found in the 68030. Separate address translation caches are provided for instructions and data, since there is a separate address path for each.

As in the 68030, the 68040 has separate instruction and data caches. Each cache contains 4K bytes, so the total cache size is the same as that of the 80486. Bus snooping provides cache coherency in multiprocessor systems. The 68030 doesn't provide snooping, and its data cache must be disabled in systems using shared data.

RISC Meets CISC

With the announcements of the 68040 and the 80486, CISC processors have taken a major step toward performance levels previously achieved only by RISC processors. This reopens the entire RISC/CISC debate and raises numerous questions about which processors are likely to be successful in various market segments.

Based on preliminary performance claims, it appears that the 68040 and the 80486 will both perform at roughly 15 VAX MIPS at 25 MHz. Each is projected to be about three times as fast as its predecessor, providing a significant speed increase while also reducing the system chip count by eliminating the floating-point coprocessor and, in many systems, the external cache.

The 68040 is said to operate at roughly three times the rate of the 68030.

Some observers question the need for this level of performance in single-user PCs, but among so-called "power users" there exists an insatiable desire for speed. More sophisticated windowing systems and user interfaces will require more processor performance just to keep the system's perceived speed at a constant level.

RISC processors have made possible a new class of workstations, including the R2000-based DECstation 3100, the 88000-based systems from Data General, and the SPARCStation 1 from Sun. These workstations cost roughly $10,000 for a basic configuration, which isn't much more than a similarly equipped 80386-based AT or Mac II, yet they provide two to three times the performance. If you're considering switching to Unix, these RISC systems provide a much better price-to-performance ratio than existing 80386- and 68030-based computers.

The drawback has been that RISC-based workstations couldn't directly use the existing DOS software base. DOS emulators are available, but their inefficiency reduces performance significant-

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ly. [Editor's note: *Some capability now exists to convert DOS software to run on RISC machines with the help of a "binary compiler." See "DOS at RISC" on page 361 for more on this subject.*]

Unix Meets DOS

The 80486 provides the best of both worlds. As a Unix engine, its performance should match that of low-end RISC-based systems. Furthermore, the 80486 will run both DOS and OS/2 software—within a Unix window if desired—and run it fast. This ability will be very valuable in convincing DOS users to move to a Unix system. If you can have top-of-the-line DOS performance and good Unix performance at the same time, it's not nearly so hard to decide to buy a Unix box.

The 68040 will also compete for the workstation market. Although it can't run DOS applications directly, it has the benefit of having the largest existing base of workstation applications software. While 80386 Xenix systems outnumber 68000-family Unix systems, most Xenix applications are business-oriented and not comparable to the technical workstation applications that are the 68000's strength. Nevertheless, the 68000 family's workstation application base is now being rapidly ported to RISC architectures.

The 68000 family's other key software assets, the Macintosh system software and applications, are an asset only to Apple. The future of the 68040 (and the future of the Macintosh itself) would be far brighter if Apple would license the Macintosh Toolbox. The 68040 will inherit Apple's high-end Macintosh business and a 68000-family compatibility-oriented segment of the workstation business, but these markets will not approach the size of the 80386 and 80486 systems market.

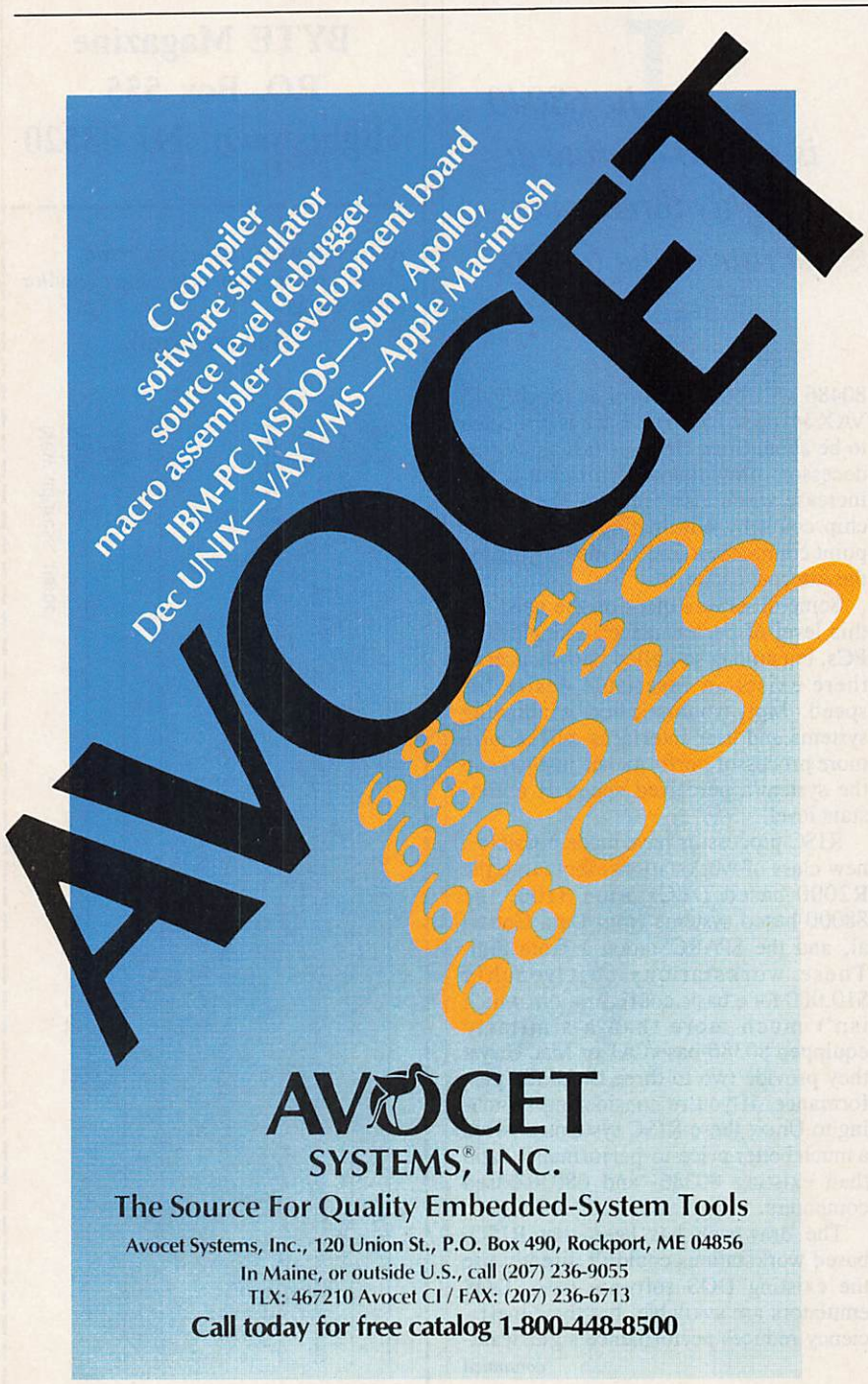
Playing Catch-Up

Some RISC advocates have claimed that CISC is doomed, since (they say) complex instructions have irregularities and external memory dependencies that inherently limit their performance. Nevertheless, by combining a finely tuned mix of brute force (multiple wide internal data buses and a huge transistor budget) and finesse (regularized instruction pipelining and an optimized bus interface), the architects of the 80486 and the 68040 have achieved near-RISC performance levels.

It now seems clear that CISC can catch up to RISC performance. However, it's important to note that this is indeed a game of catch-up. The 68040 and the 80486 will begin volume shipments in 1990; both SPARC and MIPS chips have been shipping with comparable performance levels for nearly two years. By 1991, a new generation of RISC chips will be doubling the performance of current implementations, and CISC will have to play catch-up again (probably in 1992) with the 68050 and the 80586. ■

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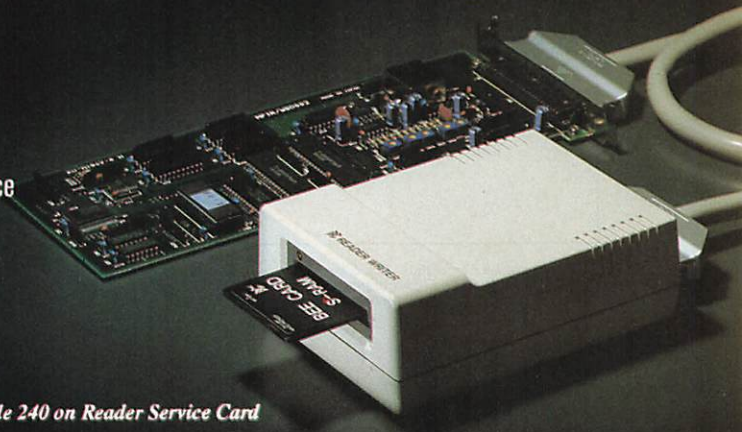
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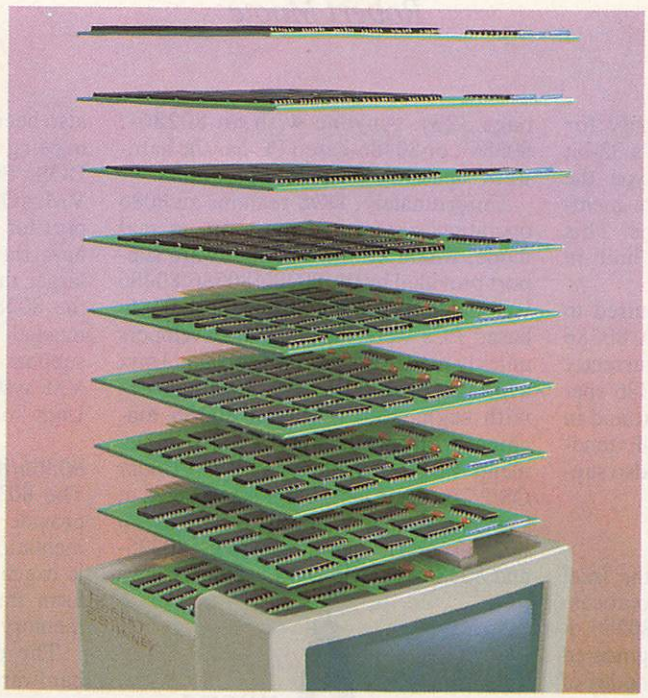
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A Virtual Crowd

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Virtual memory gives you the ability to run programs that are larger than the amount of physical memory installed on your computer. First used in the Atlas computer system at the University of Manchester, England, in 1960, VM today is almost universally available on mainframes, minicomputers, and workstations.

A distinguishing feature of VM is its low profile—you need not be concerned with the details of fitting your program into memory. Contrast this with, for example, program overlays. Overlays require you to indicate explicitly which parts of the program must be in memory simultaneously, and which parts are disjoint and need not coexist. Each time a new version of the application is released, these decisions must be revisited.

With a VM system, you simply build your multimegabyte application, oblivious to the amount of memory installed on the computer. If the computer has more memory, the application runs faster; less memory, and it runs slower—but it always runs, with no extra programming required.

How is this sleight of hand accomplished? At any given moment during the execution of a program, some portion of it is in physical memory, and the rest is swapped to disk. As the program executes, it continually references code and data in other parts of the program. If the referenced code or data is in memory, program execution continues uninterrupted. If the program references something that is not in memory, the operating system gets control. The referenced code or data is brought into physical memory (if necessary, causing some other part of the program to be swapped to disk); the application program continues executing, oblivious to all this activity.

To use VM, a program must be divided into pieces. Individual pieces of the program can be either in memory or swapped to disk at any given time, and the VM subsystem of the operating system must keep track of each piece. If the pieces are variable in size, they are called *segments*, and they usually relate in some way to the organization of the program (in the simplest case, the program has one code segment and one data segment). If the pieces are always the same size, they are called *pages*. In either case, hardware assistance is required to enable the VM system to bring referenced pieces into memory without the knowledge of the application program. It's generally accepted today that paging offers performance benefits over segmentation, and most commercially available VM systems offer some form of demand-paged VM. The term *demand*

continued

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paging means pages are brought into memory as they are referenced, as opposed to *anticipatory paging*, in which the VM system attempts to predict the pages that a program will need next.

A VM system is a clearly delineated subsystem of an operating system. The VM system allocates and frees memory, maintains the data structures necessary to perform the virtual-to-physical-address translation, and brings program pieces into memory as they are referenced. VM can, of course, be implemented for both single-tasking and multitasking operating systems, and it is essentially the same in either environment. The only additional consideration required for multitasking is separate tracking of the virtual address space for each process, to implement working set management at the process level.

The following two articles discuss the details of VM implementations on 80386 and 80486 systems and on the Macintosh. The first discusses how Intel's hardware has evolved to make demand-paged VM possible. The second describes how Macintosh System 7.0 implements VM while maintaining compatibility with applications written before VM was even considered for the Mac. The arrival of VM on the two most popular computing architectures signals another important advance in the capabilities of personal computers.

—Robert Moote

Virtual Memory: The Next Generation

Intel's 80386 and 80486 microprocessors bring demand-paged virtual memory to your desktop

Robert Moote

Although noted primarily for their raw power, Intel's 32-bit processors also give you the ability to address more memory than your computer contains. This capability is a result of their built-in hardware support for VM.

Software support is also required to provide demand-paged VM on 80386 and 80486 machines. You can currently find VM implementations in 80386-specific versions of Unix and Xenix, and in Phar Lap Software's 386|DOS-Extender. Future versions of OS/2 will also support demand-paged VM.

Hardware Roots

IBM based its original PC on the Intel 8088, a variant of the 8086 microprocessor. When Intel introduced the 80286, it built in hardware support for segmented VM. Thus, the 80286 has two modes of operation: real mode, in which it looks like a fast 8086 to ensure backward compatibility with DOS, and protected mode, which provides (among other things) the hardware support necessary to build a segmented VM system. With the 80386, Intel added hardware paging support and 32-bit operation. Recently, Intel introduced the 80486, which, from a software point of view, is largely a fast 80386 (see "Revenge of the CISCs" on page 323). Anyone with an 80286-, 80386-, or 80486-based PC has the hardware capability to run VM programs.

Unfortunately, DOS remains an 8086 operating system and must run in real mode, where all the VM hardware support provided by the 80286/80386/80486 is disabled. When 80286 and then 80386-based PCs were introduced, developers quickly made versions of Xenix and Unix available, providing 80286 machines with segmented VM and 80386 machines with paged VM. OS/2 also implements VM (see the text box "VM Under OS/2" on page 344), but it is restricted to segment swapping because OS/2 is an 80286-specific operating system. 80286- and 80386-specific DOS extenders have also been available for years. In addition to being able to run large programs under DOS, these extenders usually support VM. (OS/2 and Unix also provide support for large programs, but they do not have the ability to run DOS programs larger than 640K bytes.) As with Unix, the 80286 DOS extenders provide segmented VM, and 80386 DOS extenders support paged VM. (For more on Unix VM systems, see the text box "VM in Unix" on page 348.)

Anyone with an 80286, 80386, or 80486 PC has the hardware capability to run VM programs.

80386/80486 Memory Architecture

The 80386 and 80486 microprocessors provide hardware support for both segmentation and paging when the processor is executing in protected mode. As the term implies, this mode also provides memory-protection benefits.

The design outlined here uses the hardware segmentation facilities for program protection, and the paging facilities for VM. This division of labor is a common choice in a combined paged/segmented architecture.

Segmentation

80386 and 80486 programs are divided into segments; at a minimum, a program has one code segment and one data segment. Code segments can't be modified, and data segments can't be executed.

This allows easy detection of a common class of programming errors. Each segment has a limit, and any attempt to access code or data beyond the segment limit is prohibited.

A program segment on the 80386 or 80486 has its own base address, segment limit (its length), and protection information (whether it is a code or data segment, whether it is read only or read/write, and so on). This information is contained in either a global descriptor table or a local descriptor table maintained by the operating system. Each entry, or *segment descriptor*, in the GDT or the LDT identifies one segment.

When a program references a memory location, it's always a location within a segment. Usually the segment is implied; that is, it's a location within the current code or data segment for that program. The 80386 and 80486 processors contain segment registers that are loaded with values—called *segment selectors*—that select a specific entry in the GDT or the LDT. The program can then reference memory as an offset within the selected segments and need only reload the segment registers when it's necessary to address a different program segment. (For programs written in a high-level language, the program segmentation and the loading of segment registers is handled entirely by the compiler, so you need not even be aware of it.)

A segment selector, plus an offset within the segment, is referred to by Intel as a *logical address*. (The logical address is called a *virtual address* on most systems because it's the address that the application program sees.) This logical address is converted by the processor's segment-translation unit into a *linear address*. The linear address is equal to the base address of the segment (obtained from the segment descriptor) added to the segment offset (see figure 1).

Because it would be expensive to read the segment descriptor in the GDT or the LDT for each memory reference, the processor caches the descriptor in an internal register whenever a segment register is loaded with a segment selector. This allows the translation operation depicted in figure 1 to be performed efficiently.

Paging

The 80386 and 80486 processors have 32-bit internal and external address buses. The maximum size of both virtual and physical memory is therefore 4 gigabytes. The physical memory on the system is divided up into 4K-byte pages,

continued

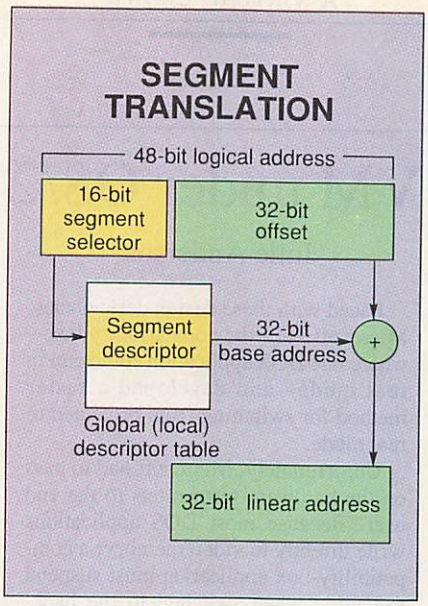


Figure 1: *The segment selector points to the entry in the descriptor table that contains the base address of the segment. When added to the offset, this produces the linear address.*

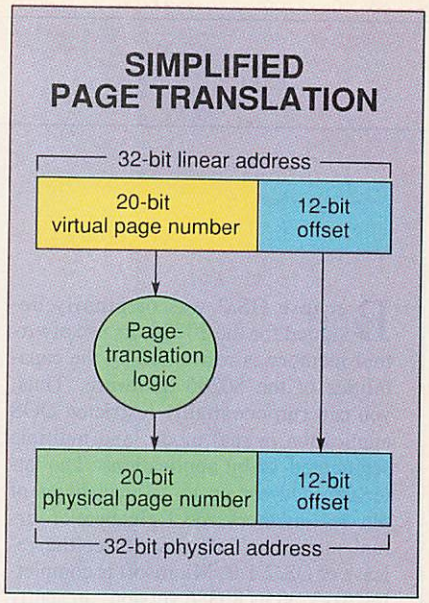


Figure 2: *The 12-bit offset provides the range needed to address any location in a 4K-byte page.*

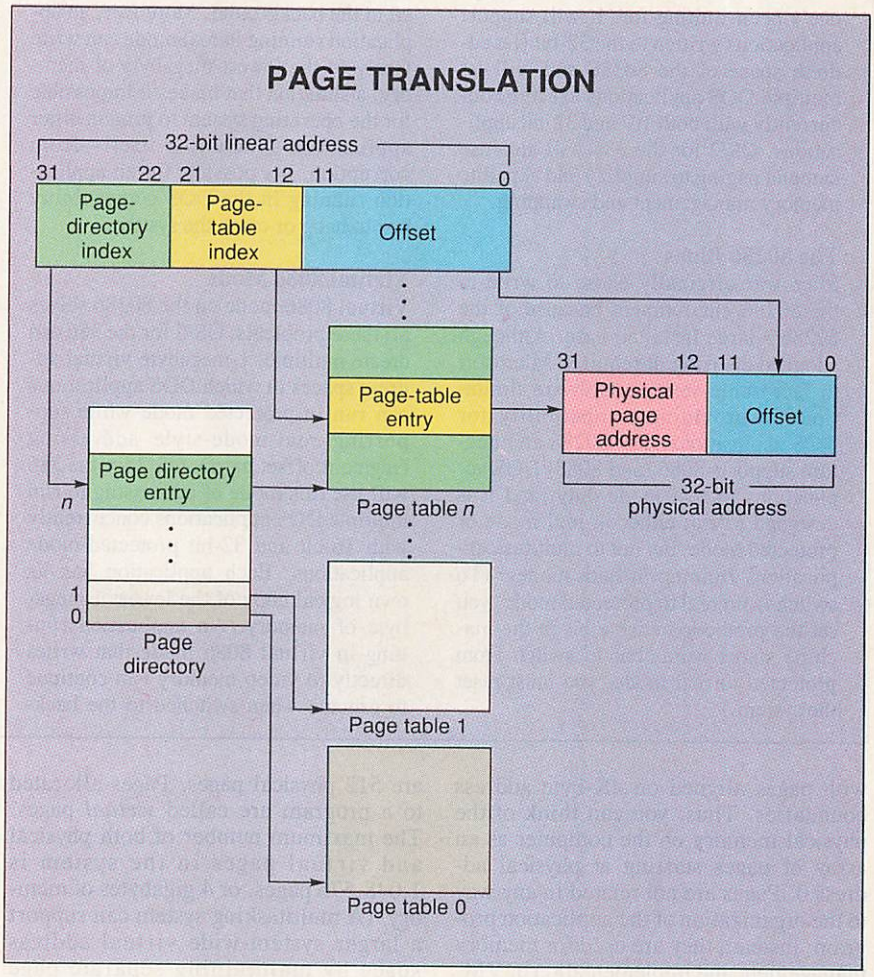


Figure 3: *The 20-bit virtual-page number actually consists of two 10-bit fields; the page-directory index and the page-table index. The most frequently accessed page-table entries are cached by the processor to optimize the translation process.*

VM under OS/2

Julie Anderson

Because OS/2 was originally designed for the 80286, its use of virtual memory is restrained by the capabilities of the 80286 hardware. Thus, you can run one highly restricted DOS application in real mode, and multiple segmented 16-bit applications. The latter can address up to 16 megabytes of physical memory and 1 gigabyte of virtual memory. Two years after the release of OS/2 1.0, Microsoft is completing work on its 80386 version, presently called OS/2 for the 386. Microsoft expects to release the Software Development Toolkit for this product at the end of this year, with the production release following in the first half of 1990.

OS/2 for the 386 is the OS/2 everyone's been waiting for. It will support applications written to the 32-bit flat address space of the 80386 and will let multiple DOS applications execute concurrently with both 16- and 32-bit applications. OS/2 for the 386 will also use demand paging to simplify and expedite memory management and swapping.

The 80286 Blues

Microsoft originally chose to write to the 80286 environment because of the 80286's large installed base. Although a logical decision, it required Microsoft to face some serious hardware limitations in providing compatibility for DOS applications. The 80286 architecture supports 8086 (and 8088) DOS applications in real mode only, and it is designed to run either in real mode or protected mode, but not to multitask applications running in both modes. (To switch from real to protected mode, you set the protection enable bit in the machine status word, but to switch from protected to real mode, you must reset the system.)

Faced with these design deficiencies, Microsoft built the compatibility box—where one DOS application could run in real mode—and developed a faster method for switching from protected to real mode.

Unfortunately, Microsoft had to pass on the hardware restrictions to the end user. Because most DOS applications write directly to video memory, a compatibility-box application must suspend execution when switched to the background so that its video output will not be mixed with the video output of the current foreground task. This means that communications programs cannot run in the compatibility box because they will lose interrupts when suspended in the background. Moreover, an application running in real mode can write freely to the lowest megabyte of memory, a situation that makes it impossible for the operating system to protect other applications—including itself—from corruption. It's possible for an application running in the DOS compatibility box to hang or crash the system.

Virtual 8086 Mode

Virtual 8086 mode on the 80386 solves all these problems. OS/2 for the 386 can create multiple, 1-megabyte virtual address spaces in which DOS applications can run in protected mode while supporting real-mode-style addressing (segment:offset pairs). OS/2 for the 386 will use this mode of addressing to run multiple DOS applications concurrently with 16-bit and 32-bit protected-mode applications. Each application has its own logical copy of the lowest 1 megabyte of memory. An application running in virtual 8086 mode that writes directly to video memory can continue to execute when switched to the background because it's writing to its logical copy of video memory. Changes made to an application's logical address space won't affect either the operating system or applications, which have their own versions of the same logical memory addresses.

In addition, the 80386 quickly switches into and out of virtual 8086 mode on a task-by-task basis, depending on the value of the TM86 flag in the Task State Segment. On an interrupt, the 80386 switches out of virtual 8086 mode, meaning that device drivers can exist outside the application's address space. OS/2 for the 386 uses this feature to map out device drivers—including network software—thus leaving as much as 600K bytes for the DOS application. In contrast, OS/2 1.1 gives the DOS application only 500K bytes. Although DOS applications that reprogram the hardware (e.g., some backup utilities) are still forbidden, any program that runs under an 80386 control program like DESQview or Windows/386 should run successfully under OS/2 for the 386.

Demand Paging

OS/2 for the 386 maps the application's logical addresses to physical memory addresses using the 80386's paging hardware, which divides the machine's physical memory into a series of 4K-byte page frames. The operating system assigns a page of virtual memory to each 4K bytes of an application's logical address space. Pages don't have to be contiguous in memory; OS/2 for the 386 keeps track of the location of an application's pages through entries in the page tables.

Demand paging, which the 80386 supports in protected mode as well as with pages aligned on 4K-byte address boundaries. Thus, you can think of the physical memory on the computer as an array of pages starting at physical address 0. Pages are not related in any way to the organization of the application program; instead, they are used for memory management and implementation of VM.

Actual memory pages in the computer are referred to as *physical* pages (often called *page frames*). For example, on a PC with 2 megabytes of memory, there are 512 physical pages. Pages allocated to a program are called *virtual* pages. The maximum number of both physical and virtual pages in the system is 1,048,576 pages, or 4 gigabytes of memory. (A multitasking system can support a larger system-wide virtual address space by maintaining separate page tables for each process in the system.) As a practical matter, the physical memory on a PC is much less than 4 gigabytes. While the virtual address space can be much larger than the available physical memory, it, too, is limited—in this case by the available disk space—because virtual pages must be kept either on disk or in physical pages.

The segment-translation logic yields a 32-bit linear address. The page-translation logic translates this linear address into the physical address that the processor places on the external memory bus (see figure 2 for a simplified view of this process). The linear address contains a

virtual 8086 mode, makes memory management on the 80386 faster and simpler than on the 80286. On the 80286, OS/2 allocates memory in variable-size segments, and then must track both the physical location and the size of an application's segments. As applications are loaded, grown, shrunk, and terminated, many variable-size segments are allocated and freed. Physical memory becomes fragmented, and OS/2 may need to move segments to free up enough contiguous memory to satisfy an allocation request. When physical memory is exhausted, OS/2 chooses a segment to swap to disk. It may need to rearrange segments in the swap file to free up enough space to write the segment. Later, when an application references the swapped segment, OS/2 must again find an appropriately sized area of physical memory into which it can read the segment from the disk.

On the 80386, the 4K-byte page frame removes much of the complexity. With this fixed-size memory-allocation unit, neither physical memory nor the swap file becomes fragmented, and moving pages is never necessary. Like segments on the 80286, developers can designate memory blocks in OS/2 for the 386 as "discardable." In this case, the page is not swapped; its space is merely reused.

Working hand-in-hand with the operating system, the 80386 hardware is optimal for demand paging. The 80386 speeds page lookups by caching on-chip, in the translation lookaside buffer, which contains the page-table entries for the 32 most recently accessed pages. When an application reads or writes to a page, the 80386 sets the accessed bit in the page-table entry. This helps the operating system determine which of the pages have been accessed recently.

On the 80386, attribute bits in page-table entries (similar to segment management on the 80286) indicate whether or not the page is present in memory and the types of accesses that are valid. To deny write access to a page, the operating system can reset the read/write attribute bit; application code is customarily marked read-only.

One additional attribute bit in the 80386 is the dirty bit. The 80386 sets this bit whenever the application writes to the page. The operating system can test this bit to determine whether or not a page should be written to disk. If the page already exists in the swap file and it hasn't changed, it can be discarded. In addition, for a page that isn't present, the operating system can use the other 31 bits of the page-table entry (all bits except the present bit) to store the disk address of the swapped page. Although it's fairly safe to assume that OS/2 for the 386 will exploit the 80386 hardware, Microsoft has not announced what use, if any, OS/2 for the 386 makes of these attribute bits.

Flat Address Space

OS/2 for the 386 supports the flat, or linear, address mode of the 80386, which allows an application to specify a segment selector and a 32-bit offset. In this mode, the 80386 supports 4 gigabytes of physical memory and 64 terabytes of virtual memory. Both 16-bit and 32-bit applications will run concurrently. To accomplish this, OS/2 for the 386 will add a dynamic link library (DLL) with a new set of application-programmer-interface calls. Those OS/2 API calls that reference 16-bit segment:offset addressing will be replaced with a 32-bit version. Because both APIs are provided in DLLs, an application simply loads the appropriate library to run.

Although a 16-bit application asks the operating system for memory in terms of segments, OS/2 for the 386 translates the request into the corresponding number of pages. Although their addressing schemes may be different, concurrent 16-bit and 32-bit applications can communicate with each other using the usual interprocess communications mechanisms, including shared memory; each application will simply use different API calls to reference them.

OS/2 for the 386

Although it's been a long wait (and it isn't over yet), OS/2 for the 386 will, by exploiting the capabilities of the 80386, address the current complaints against OS/2. More than one DOS application will run with true concurrency.

An efficient memory page-swapping technique will reduce the amount of physical memory you need to add to the system for acceptable performance. Most important, having access to the 80386's flat address space may entice developers to port applications from other unsegmented architectures, opening up the potential for a new class of OS/2 applications.

Julie Anderson, former editor of PC Tech Journal, *has an M.S. degree in computer science from Johns Hopkins University and 14 years' experience as a systems developer. She is manager of Standard Components and Tools at RoadNet Technologies (Baltimore, MD). She can be reached on BIX c/o "editors."*

12-bit offset (2^{12} equals 4096, the page size) and a 20-bit virtual-page number.

The processor looks up the virtual-page number in page tables maintained by the VM system. This process generates a 20-bit physical-page number. When concatenated with the offset, the result is the physical memory address. For example, if virtual page 8 (linear addresses from 32K to 36K) is mapped to physical page 1 (physical addresses from 4K to 8K) in the page tables, then the linear address 33K (00008400 hexadecimal) maps to physical address 5K (00001400 hexadecimal); the 20-bit virtual-page number 8 is mapped to the 20-bit physical-page number 1.

Figure 3 shows the page-translation process in more detail. The 20-bit virtual-page number is composed of two 10-bit fields: a page-directory index and a page-table index. The VM system maintains one page directory and multiple page tables. The page directory and page tables are 4K bytes in size, each containing 1024 32-bit entries. Each entry in the page directory contains the physical address of a page table. Each entry in a page table contains the address of a physical page. Thus, the page-translation logic uses the page-directory index to obtain the address of the appropriate page table, and it uses the page-table index to look up the address of the physical page.

The contents of a page-table entry for a

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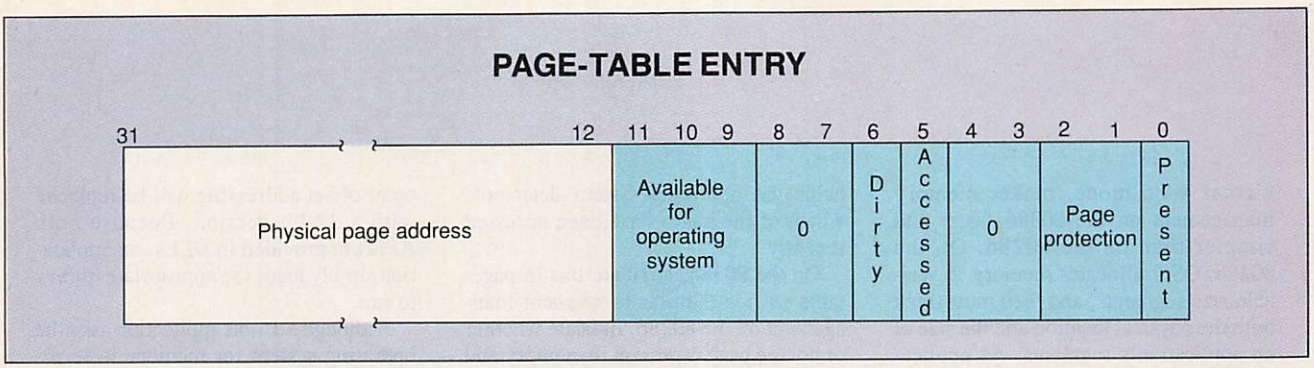


Figure 4: *Twelve bits in the page-table entry provide information about the page to the processor and to the VM subsystem of the operating system. Four bits on the 80386 (2 on the 80486) are unused and reserved.*

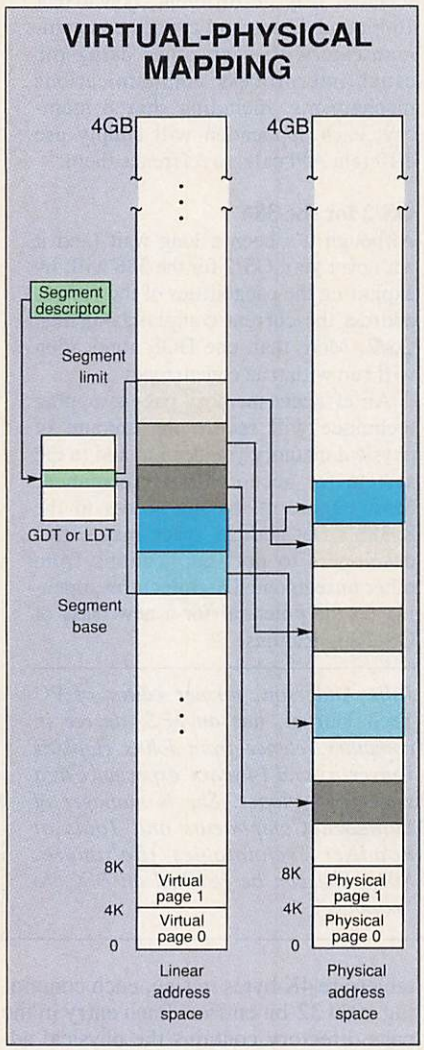


Figure 5: *When combined, segmentation and paging result in a system that provides protection without causing memory fragmentation. Segments are used for program protection, and paging is used to map programs into physical memory in fixed-size chunks.*

page present in physical memory are shown in figure 4. The 20-bit physical-page address leaves 12 bits available for additional information. Bit 0 is the present bit; it indicates whether the page is in memory or swapped to disk. For present pages, bits 1 and 2 are used for page protection; they mark a page either read only, read/write, or supervisor access only. Bit 5—the accessed bit—is set by the processor each time the page is accessed, and bit 6—the dirty bit—is set when the page is modified. The dirty bit and accessed bit are crucial for the implementation of VM. Bits 9 through 11 are available for use by the VM system, and the remaining 4 bits are reserved in the 80386 for use in future processors. Two of those 4 bits (bits 3 and 4) are used in the 80486 processor to control memory caching at the page level.

If a page is marked "not present" (the present bit is 0), the VM system can use all the other 31 bits in the page-table entry.

The page-translation process appears expensive, since it involves two memory accesses—one to the page directory and one to the appropriate page table—to obtain the address of the physical page. The 80386 or 80486 processor therefore keeps a four-way set-associative cache of recently referenced page-table entries. This cache is called the translation look-aside buffer. Since programs tend to exhibit localized referencing behavior, most page references result in a hit in the TLB. Thus, extra memory references are usually not required to obtain the needed page-table entry. Normally, software can ignore the operation of the TLB. However, VM system software must flush the TLB after making changes to the page tables to ensure no stale page-table entries remain.

The combined effects of segment translation and page translation are shown in figure 5, which demonstrates one possible mapping for a segment five pages (20K bytes) in size. In this example, the segment base address is aligned on a page boundary, and the segment spans exactly five virtual pages. Note that the segment is contiguous in the linear address space; this is mandatory. The five virtual pages are mapped by the page-translation logic to five noncontiguous physical pages.

VM Management

The job of a VM system is to allocate and free VM for use by programs, write virtual pages to a swap file on the disk if there are too many virtual pages to fit in physical memory, and bring pages back into memory as page faults occur, so the program can continue to execute. This is primarily a bookkeeping job. Part of this job requires the use of an algorithm that decides which page is to be replaced (swapped to disk) when a page fault occurs and a physical page is required to bring the referenced virtual page into memory. The choice of this algorithm can have considerable impact on the performance of an application program.

The VM system must maintain the data structures (the GDT, the LDT, and the page tables) so the processor can do address translation. It must also keep any additional information required to perform the rest of its tasks.

VM Data Structures

The VM system must keep track of free (unused) physical memory. Since pages are a fixed size and need not be contiguous (because contiguity is preserved in the linear address space, not the physical address space), this is a trivial task. A one-way linked list of free physical pages is all that is necessary.

When a segment is allocated or extended, it requires a contiguous region in the 4-gigabyte linear address space (see figure 5). The VM system must therefore

keep track of allocated and free regions in the linear address space. This is most efficiently done by means of a bit map, one bit for each page in the linear address space.

The VM system must also maintain certain information about pages in memory (see table 1) and pages not in memory (see table 2) in the page-table entry.

When a virtual page is marked "not present," there are 31 bits available for use by the VM system in the page-table entry. However, if the page is present, only 3 bits are available. It's possible to maintain all the information listed in table 1 in one 32-bit page-table entry if (a) just the accessed bit and the dirty bit are used for the page-replacement algorithm, (b) in-memory pages don't need an address in the swap file, (c) no process ID is needed, and (d) statistics are not kept on a per-page basis.

If more information is required (for more sophisticated swap-file management, a better page-replacement algorithm, or keeping paging statistics), the VM system must maintain an additional data structure in parallel with the page tables. For example, the parallel data structure could allocate an additional 32 bits of information for each virtual page, so that a total of 64 bits is available.

A virtual page marked "present" could then use the 3 VM system bits in the page-table entry for a page-locked flag, a system-page flag, and a mapped-page flag. The parallel data structure might contain a page-on-disk flag, a swap-file address, page-aging information, and statistics information.

A virtual page marked "not present" would use a present bit and a page-replaced flag in the page-table entry. The remaining 30 bits would be available for other information (such as a time stamp for when the page was replaced). A page marked "not present" would contain the same information as a present page in the parallel data structure.

Handling Page Faults

A page fault occurs when a reference is made to a virtual page that is marked "not present" in the page tables. It is the page-fault handler's responsibility to allocate a physical memory page, bring the virtual page into memory, and then restart the instruction that caused the page fault.

Usually, when a page fault occurs, all physical pages are in use. The page-fault handler must select a virtual page that is in physical memory and swap it out to disk, thereby freeing a physical page for

continued

Table 1: *Besides address information, the VM system needs to keep track of present-page characteristics and information for the page-replacement algorithm.*

INFORMATION REQUIRED FOR PRESENT PAGES

1. The address of the physical page to which it is mapped (bits 12-31 of the page-table entry).
2. Page-aging information, used to decide which virtual page to replace (swap to disk) when a page fault occurs. The not-recently used (NUR) strategy needs only the accessed and dirty bits in the page-table entry to make this choice; other replacement algorithms require more detailed aging information.
3. A flag marking the page as locked or unlocked. Locked pages cannot be paged to disk. This is required for operating-system pages, and sometimes for application program pages (e.g., for hardware interrupt handlers).
4. A flag identifying the page as owned by the operating system or by an application program. This is not always required (often it's sufficient merely to mark operating-system pages locked). On multitasking systems, a process ID may be needed.
5. A flag identifying the physical page as allocated (the usual case) or mapped. Programs sometimes need to map a region of the physical address space to access memory-mapped hardware devices. Mapped memory is not physical RAM memory, and the VM system must be able to make the distinction so it doesn't attempt to return mapped memory to the free physical-page list when it's deallocated.
6. A flag for whether the virtual page is also in the swap file, and if so, the address within the swap file where it is stored. This is used to enhance system performance when the page is replaced. If it is already in the swap file and has not been modified (the dirty bit is not set), then the expensive disk-write operation needed to put the page in the swap file can be avoided.
7. Optional paging-statistics information kept for performance analysis (and working set management, in a multitasking system). Typically kept information includes the number of times each page has been replaced, the paging rate (the number of page faults per second processed by the system), the page-reclaim rate (the number of page faults per second on previously replaced pages, as opposed to program pages being referenced for the first time), and a complete history of a program's paging activity.

Table 2: *Swapped pages keep track of their location on disk, indicate whether they are yet present on disk, and keep various statistics.*

INFORMATION REQUIRED FOR SWAPPED PAGES

1. The address of the virtual page in the swap file.
2. A flag indicating whether the virtual page is in the swap file. In a commonly used optimization, a virtual memory page newly allocated by a program is simply marked "not present" and "not in the swap file." It's not desirable to allocate a physical page immediately, because programs commonly allocate large amounts of virtual memory at a time. The first time the page is referenced, the VM system allocates a physical page and zeroes it. This avoids a disk write needed to put a zeroed page in the swap file when the virtual memory page is allocated, and it also avoids a disk read to bring the page in from the swap file the first time it's referenced. The page is only allocated and written to the swap file when (and if) it's finally swapped out to disk.
3. Additional statistics information. This typically includes a flag used to keep statistics on the page-reclaim rate that specifies whether the page is in the swap file because it's been replaced or because it hasn't yet been referenced by the program. More elaborate schemes might also time-stamp the page when it's replaced, so that the VM system can calculate the elapsed time between when the page is swapped out and the next time it's referenced.

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VM in Unix

Ben Smith

Programmers at the University of California at Berkeley first introduced virtual memory to Unix in 1978. The impetus was the VMS operating system on Digital Equipment Corp.'s VAX computer, which had the ability to address and use 1 gigabyte of memory when it had as little as 1 megabyte of physical memory. Earlier DEC machines required that all users have separate memory (limited to 64K bytes), private to their individual processes. The result of the Berkeley programming effort was 3BSD (and 4BSD in 1980). The spread of BSD Unix can be attributed, more than anything else, to this one feature. Now, all modern versions of the Unix kernel have either swapping or paging, which are two versions of virtual memory.

Swapping

Although in some contexts the terms *swapping* and *paging* refer to the same thing, in the Unix environment, swapping refers to moving entire processes in and out of physical memory. It's obvious that if each user process is going to be allowed to use a major part of memory, the only way to support multiprocessing is to swap these processes out of active memory to allow space for the next process. Each process is brought back into active memory when it's time for it to continue processing. A separate area of the disk (or a separate disk) is reserved just for swapping. This area does not require management by the file system, but instead is managed by the kernel, which is more tuned to the needs of swapping.

The limitation on swapping is that a single process must always use less than the system's physical memory capacity. (Some memory must be held for the kernel.) However, swapping is simple to implement and therefore requires little operating-system overhead.

Paging under Unix

The incorporation of memory management units into most modern computers has provided virtual addressing, a necessary element of paged virtual memory. The virtual address space is divided up into units called *pages*. If the operating system takes advantage of these facilities, it will properly handle page faults by moving virtual memory in and out of active memory as required. Since a page is smaller than the process or its data area, there is a finer control of memory. Only parts of a process need to be moved out to storage, not the whole process. There can be enough of it left in physical memory to continue the process while the data and nonactive sections of the program are moved back and forth between active memory and storage.

Because pages are a fixed size, the memory management at the page level doesn't relate to what the memory is being used for. The operating system can determine what a particular area of memory is being used for by looking at the structure of the executable file or process. Pages can be grouped into logical segments for each kind of use. Memory management at this level can relate to what the memory is being used for, as well as which memory is least-recently used. All processes and their data can be handled similarly, with the exception

the virtual page that is being brought into memory.

Page-replacement strategies have been the subject of considerable debate. Obviously, the best choice is the virtual page that the program will not reference for the longest time into the future. Since programs cannot predict the future, the page-replacement algorithm must be based on a heuristic about typical program behavior. Any such algorithm will occasionally make bad decisions; the objective is to select a strategy that makes reasonably good decisions most of the time and doesn't incur a lot of overhead.

Perhaps the most popular algorithm is least-recently used (LRU) replacement. This strategy selects for replacement the page that hasn't been referenced for the longest time. This is based on the heuristic that the recent past is a good indicator of the immediate future. Supporting this are common program constructs such as looping, subroutine calls, stacks, and repetitive array traversals.

Implementation of a full LRU algorithm requires time stamping a page each time it is referenced. This support is not provided by most hardware (including the 80386 and 80486). Thus, an approxi-

of the Unix kernel. The kernel serves all other processes and therefore must reside in physical memory at all times. So, even with virtual memory, the physical memory must exceed the size of the kernel. With some of today's kernels in excess of 2 megabytes, this is not a trivial requirement.

Mach to the Rescue

The Mach kernel (from Carnegie Mellon University) solves many of the memory problems that are inherent in standard Unix schemes. Mach doesn't require device drivers to be linked into the kernel, and therefore the kernel is much smaller.

Mach splits the concept of a process into two elements, *tasks* and *threads*. A task provides the physical environment to its threads. A thread can be created or destroyed, or started or stopped without adversely affecting its task. By having the operation of device drivers incorporated into threads of the kernel task, drivers are loaded into physical memory only when needed.

Mach's virtual memory implementation is significant. It's object-oriented, it has hooks for the implementation of virtual memory concepts at the user level rather than just at the kernel level, and it uses copy-on-write algorithms for efficiency. A task can allocate and deallocate arbitrary regions of virtual memory and change the protections and inheritance of allocated regions. Mach's virtual memory runs on both paged and unpaged memory management hardware. From the start, Mach was designed for undefined parallel-processor machines; it is building memory management for the computers of the future.

This hardware independence makes Mach an attractive design for developers. However, it has only been fully implemented on the NeXT Computer. (There are other implementations under development.) Mach is most significant as the guiding light for future Unix kernel design. It is influencing the designs of the OSF and AT&T Unixes (see "Mach: The Model for Future Unix" on page 411).

Designs of the Future

Virtual memory methods are particularly valuable to Unix developers. Because of the wide spectrum of Unix platforms, it's important that they appear identical to all the applications that run across them. Particularly now that Unix network nodes are so varied, standards need to be established to which all members of the network adhere.

The future designs of Unix systems will include vagrant processes or tasks moving around from server to server as the needs of the task change and the resource loads vary. Virtual memory in Unix will no longer pertain to physical memory and devices close at hand, but will extend to all resources in the network. The network will become one large virtual machine with aggregate resources beyond those of any single machine of today. The implementation and standardization of virtual memory methods is crucial to the designs of future Unix systems.

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mation of an LRU algorithm is usually selected.

LFU Page Replacement

One common approximation to LRU is least-frequently used (LFU) replacement. This scheme maintains a frequency count of references to each page. The page tables are scanned periodically, and the frequency count for each page that has been accessed is incremented (the scan also clears the accessed bit for each page, so the next scan will have fresh information available). The page with the lowest frequency count (the LFU page) is selected for replacement.

Two problems with this algorithm are that pages that are used heavily during the program initialization phase tend to remain in memory even after initialization is completed, and a page is vulnerable to replacement immediately after it is brought into memory (because its frequency count is 1, and all other in-memory pages may have been referenced more than once). A refinement of this algorithm increments the frequency count if the page is accessed, and decrements it if the page is not accessed, so that pages no longer being used gradually become more vulnerable to replacement. When a page is brought into memory, it's given an initial frequency count at the midpoint of the possible range of frequency-count values.

NUR Page Replacement

The not-used-recently (NUR) approximation to LRU is attractive because of its low overhead and its ability to make surprisingly good choices, considering the small amount of information on which its decisions are based. This algorithm uses the accessed and dirty bits maintained for each page to choose a page for replacement. When a program is first loaded, none of the pages has been accessed or modified. As program execution proceeds, code pages are accessed, and data pages are accessed or modified (marked dirty). Based on the values of the accessed and dirty bits, each page is placed in one of four categories, as shown in table 3.

The lower the category a page falls in, the more attractive the page is for replacement. The ordering of the categories is based on the heuristic that pages that haven't been accessed aren't likely to be needed in the near future. It is also based on the observation that unmodified pages are more attractive for replacement than dirty pages, because unmodified pages need not be written out to the swap file. Since there are typically many pages in each category, the algorithm performs a circular scan of the linear address space, starting with the page immediately following the last page swapped, and selects the earliest occurrence of the lowest category encountered.

As program execution proceeds, most pages tend to fall into categories 2 and 3, and the VM system loses the ability to make good choices. Therefore, the VM system periodically scans all the pages and clears the accessed bit for each page. This resetting of the accessed bits explains how pages fall into category 1 (modified but not accessed), which otherwise would describe an unrealistic situation. Immediately following the page-table scan, all pages are vulnerable to replacement; but not for long, as actively referenced pages quickly are marked as "accessed" again.

The Page-Swap File

Virtual pages that are not in physical memory are kept in a page-swap file on disk. Since pages are of fixed size, you can think of the swap file as an array of virtual pages. In the simplest case, the swap file is always as large as the virtual

continued

Table 3: *When a program references a physical page in a not-used recently (NUR) system, its accessed bit is set. If the program writes to the page, its dirty bit is set. Pages in category 0 are the ones first swapped to disk.*

NUR PAGE-REPLACEMENT CATEGORIES

Category	Accessed	Dirty
0	0	0
1	0	1
2	1	0
3	1	1

address space, and there is a one-to-one correspondence between virtual pages and their addresses in the swap file. The virtue of this design is its simplicity, along with the fact that a swap-file address need not be kept with each virtual page, reducing the overhead for data structures. The primary problem of the design is its consumption of disk space. Since programs often allocate huge amounts of VM, the disk space required may be prohibitive. For some operating systems, a swap-file region of fixed size is allocated on the disk when the system is configured. The decision of how large to make the swap file limits the maximum size of the virtual address space, thus determining the largest program that can be run.

Disk space is often a prime consideration on personal computers. Thus, it's often desirable to keep the swap file smaller than the virtual address space and to dynamically increase the size of the swap file as the program runs. This eliminates the one-to-one correspondence between virtual pages and swap-file addresses, however, so a swap-file address must be kept with each virtual page. In addition, when an application frees virtual pages, the space allocated to them in the swap file must be reclaimed. Because of this, the VM system must maintain a data structure for allocated and free pages in the swap file (usually a bit map, 1 bit per page in the swap file, is the best choice). So the decision to reduce the swap-file size comes at the expense of additional VM data structures and complexity.

Swap-file management can become complex, with many trade-offs involved.

The Bottom Line

The primary benefit of paged VM is the ability to run large programs regardless of the physical memory configuration of the computer system. Secondary benefits are the ability to place a program anywhere in physical memory without affecting how it executes, using fixed-size pages to eliminate the problem of physical memory fragmentation, and the ability to keep a program contiguous in virtual memory without requiring contiguous physical memory.

The main cost of VM is disk space—the portions of the program that are not in memory must be kept in a swap file on disk. A secondary cost is a slowdown in the program response time due to swapping; however, you must remember that a program large enough to require swapping couldn't run at all without VM.

With the hardware support for paged VM provided by the 80386 and 80486 processors, this capability is now possible on personal computers. Demand-paged VM is available today on 80386s running Unix or an extended DOS application program. With this development, the line between high-end personal computers and low-end workstations and minicomputers, already blurred, has all but disappeared.

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Mac VM Revealed

Virtual memory comes to the Mac: Small in scope, efficient, transparent, and, above all, compatible

Phil Goldman

As Macintosh applications grow larger and more complex, and as multitasking permits more than one application in memory at a time, RAM has become a scarce and precious commodity. One way to satisfy your Mac's ever-growing appetite for memory is to buy more. This is an expensive solution, however, and one that is still limited by the physical design of your computer. A less expensive and more elegant solution is to use your disk drive as RAM.

Mac-Flavored VM

The Macintosh virtual memory manager (which I will hereafter call Mac VM) is included as part of version 7.0 of the Mac System software. It allows the Mac to access up to 14 megabytes of memory using today's 24-bit ROMs. On newer 32-bit ROMs, it allows the Mac to address up to 1 gigabyte of memory. Practically speaking though, the VM size is constrained by how much disk space you have available; today, this is usually 300 megabytes or less, typically 40.

Mac VM runs on any Macintosh that contains a memory management unit (MMU). This unit is built into the Motorola 68030 CPU used in the Mac IIx, IIcx, and the Mac SE/30. It is an add-on

continued

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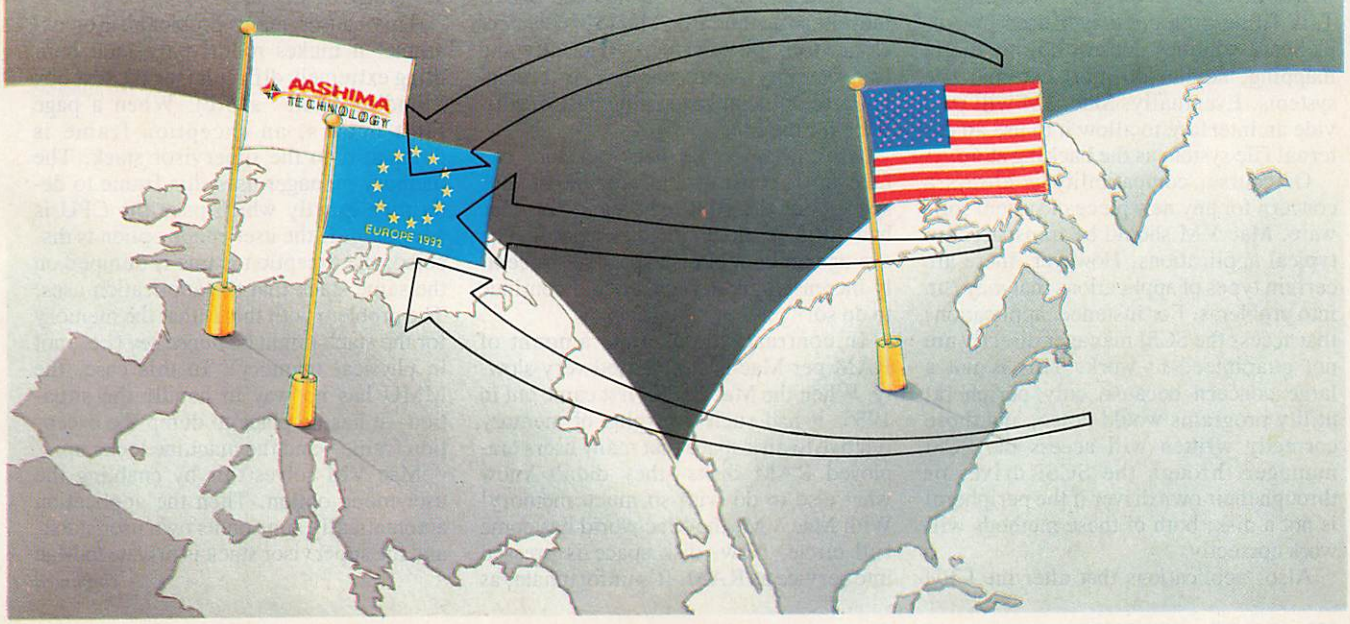
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Circle 11 on Reader Service Card

Finding Fault

In a virtual memory system, memory is divided into pieces called *pages*. At any time, some of an application's virtual pages will be in memory; others will be stored on disk. To make logical memory appear larger than physical memory, each virtual page must be distinguished by whether or not it is in physical memory. If it is, the page-table entry for the page contains the address of the physical page frame.

However, if the page referred to in the table entry is not in physical memory, a page fault occurs, and the memory management unit yields control to the memory manager. This is where your hard disk comes in. If the page accessed is not in physical memory, then it is contained on disk—specifically, in a portion of the disk (often a file) known as the *backing store*.

When a page fault occurs, the memory manager first frees up physical memory space by selecting a physical page frame and writing the virtual page that it contains onto the backing store. It then reads the page data for the desired virtual page into the frame and changes the new page's table entry to show that the page is in physical memory and located in the page frame stolen from the displaced page. Likewise, the entry for the page written to disk is updated; it is marked "not in physical memory." Finally, the memory manager returns control to the CPU, which retries the access that caused the page fault. The entire process is known as *page-fault handling*.

You can think of the backing store as an image of virtual memory; a particular page's data is found at the same offset in the backing store as it is in virtual memory. Pages are brought into physical memory as needed, but reside on disk. (In fact, they need to be written back to disk only if they have been changed since last being read from the disk). Because of this, the amount of virtual memory is limited to the disk space available for the backing store.

option for the Mac II, which uses the 68020 CPU.

Another requirement is a reasonable amount of disk space for the backing store—the disk file that stores pages not currently in memory. You must set aside an amount of backing store equal to the amount of memory desired. All this space must reside on the same disk volume, which must be a Hierarchical File System volume. You can't use an external file system, such as MS-DOS, nor a remote one, such as AppleShare, for the backing store.

This last restriction is necessary because Mac VM transfers to and from the disk mostly at the driver level. Thus, any driver that underlies a backing-store volume must support block-level reads and writes directly to the disk. The AppleTalk filing protocol driver used by AppleShare volumes doesn't do this direct mapping; neither do most external file systems. Eventually, Mac VM will provide an interface to allow it to use an external file system as the backing store.

Of course, compatibility is always a concern for any new piece of system software. Mac VM should be transparent to typical applications. However, there are certain types of applications that may run into problems. For instance, applications that access the SCSI manager directly are not guaranteed to work. This is not a large concern because only peripheral utility programs would do so, and those correctly written will access the SCSI manager through the SCSI driver or through their own driver if the peripheral is not a disk; both of these methods will work correctly.

Also, applications that alter the CPU interrupt vectors directly will crash under Mac VM. This, too, is a forbidden practice (as defined by Apple's guidelines for software developers), but it may be Mac VM that exposes the problem. Fortunately, this practice is ancient, and the applications that adopted it—mainly for copy-protection purposes—have long since ceased and desisted.

Note that both of these practices, while strictly "illegal," will still work for drivers. In general, the only type of code that could possibly break goes directly from the interrupt vectors to application memory (i.e., the application memory heap, the stack, or the A5 globals).

Pieces of the Puzzle

Up until the introduction of the Mac IIx last year, no Macintosh had the MMU built in as a standard. The MMU is necessary to implement VM efficiently and transparently. Transparency is crucial because of the huge existing base of software for the Mac.

Also, Mac VM's backing store can take up a considerable amount of disk space. For the first few years, the Mac had little or no extra disk space. The average amount of disk space has recently increased greatly and should continue to do so.

In contrast, the average amount of RAM per Mac has increased very slowly. When the Mac 512K first came out in 1985, it had such a surplus of memory relative to disk space that many users employed RAM disks—they didn't know what else to do with so much memory! With Mac VM, the Mac world has come full circle. Now, disk space is pressed into service as RAM. It's unfortunate, as the first situation is definitely preferable to the second.

Retrofitting the Mac OS

When the Mac OS was originally developed, VM was not a goal—not even a long-range one. Consequently, many shortcuts were taken in the architecture and implementation that have made the development of VM very difficult.

For instance, the Mac OS implicitly assumes that an application has complete control over the machine. The 68000 has an option that divides CPU processing between user mode (for applications) and supervisor mode (for the operating system). When disabled, all code is run in supervisor mode. The Mac OS never enables this option, and applications take advantage of this fact.

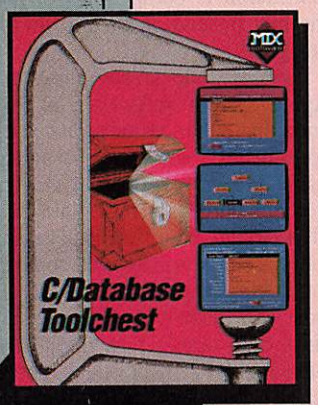
This causes many problems. For example, it makes robust page-fault handling extremely difficult (see the text box "Finding Fault" above). When a page fault occurs, an exception frame is dumped onto the supervisor stack. The memory manager uses this frame to determine exactly which page the CPU is accessing. If the user-mode option is disabled, the exception frame is dumped on the same stack that the application uses. The problem with this is that the memory for the stack might be *paged out* (i.e., not in physical memory). In this case, the MMU has no way to handle the situation—it has no place to dump the exception frame—and the machine locks up.

Mac VM solves this by enabling the user-mode option. Then the application automatically runs on its own user stack, and the supervisor stack is private to Mac

continued

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Table 1: *Mac VM's public interface consists of calls that let applications hold data in memory and calls used by NuBus peripherals.*

MAC VM PROGRAMMING INTERFACE

Command	Description
`DeferUserFn`	Allows a given user-code routine to be called as soon as it is OK to page fault (usually immediately).
`GetPhysical`	Given a range of held virtual memory, returns a table of physical memory extents to which they map. It returns an error if the entire range is not locked.
`HoldMemory`	Holds a given range of virtual memory in physical memory.
`LockMemory`	Holds a given range of memory in physical memory and makes sure it does not move within physical memory.
`LockMemoryContiguous`	Same as `LockMemory`, except that the physical pages chosen are one contiguous range. Memory may need to be moved to accommodate this request.
`UnholdMemory`	Releases a given range of virtual memory from being necessarily held in physical memory. It is now fair game for page replacement.
`UnlockMemory`	Undoes the effect of LockMemory.

VM and held in physical memory. Mac VM handles applications that wish to make use of supervisor-mode instructions by emulating the instructions in software.

Double Faults

The exception-frame dilemma is just one special case of a more general problem. Mac VM must ensure that in processing a page fault it doesn't generate a new one. This is the main reason that Mac VM doesn't use the file system to transfer pages between memory and the backing-store file.

The file system contains a large number of hooks—low-memory addresses that point to routines it calls. Sometimes, applications replace these hooks with ones that point to their own routines. The problem is that the memory occupied by these routines may be paged out to disk when Mac VM starts processing a page fault.

Thus, calling the file system in the midst of page-fault handling could conceivably cause additional, infinitely recursive page-faulting. Because of this, Mac VM uses the underlying driver and avoids the file system. Luckily, drivers don't have low-memory hooks, so Mac VM must only ensure that the memory it passes to the driver is kept in physical memory.

This last situation is trickier than it seems. Because current SCSI drivers are not reentrant (i.e., callable more than once concurrently), Mac VM must make sure that a backing driver (usually the SCSI driver) will never page-fault. If it does, you end up with the situation where Mac VM needs the driver during page-fault handling but can't get it because it is already being used. The solution is to trap all calls to the driver, made via the `_Control`, `_Status`, `_Read`, and `_Write` traps, and to hold a few things in physical memory—namely the parameter block, the application-supplied transfer buffer (for reads or writes), and the part of the stack that the driver might use (the few hundred bytes underneath the current stack pointer).

Deadly Interrupts

In addition to keeping the driver from page-faulting, Mac VM must ensure that no interrupt code page-faults while the backing driver is in use. This includes such code fragments as VBL (for vertical blank) tasks, time-manager tasks, I/O-completion routines, and raw interrupt code. All of these happen asynchronously with respect to the driver, so even careful monitoring of the driver won't catch them.

One simple solution is to turn off interrupts while using the driver. This isn't very satisfactory because it cripples the machine whenever the driver is used, which could be for many seconds at a time during file transfers. The cursor will be jerky (because the mouse won't be sampled often), AppleTalk will drop packets, and serial communications may fail. All in all, using the machine would be very frustrating.

A much nicer solution—the one that Mac VM adopts—is to be selective about which code will run at interrupt time when the driver is in use. Mac VM differentiates between user code and system code (which is somewhat ironic, as the distinction is being made 5 years after the fact instead of during the Mac OS's design).

System code is composed mostly of Apple system software, or third-party code that enhances or replaces it. System code usually exists in the system heap, which is always kept in physical memory. It keeps both its private data storage and all external data that it accesses within the system heap. System code that must touch application memory at interrupt time can make use of special Mac VM calls (see table 1) to temporarily hold such memory in physical memory. Examples of system code include the floppy disk driver, AppleTalk, the SCSI manager, the Apple desktop bus drivers (mouse and keyboard), and INITs.

User code typically comes from an application and resides mostly within an application's MultiFinder partition. It might run at interrupt time. User code includes application-spawned VBL and time manager tasks, AppleTalk link access protocol handlers, and completion routines, as well as application code. User code is allowed to cause page faults.

With a well-defined division of user and system code, Mac VM can simulate turning off interrupts by suspending all user code while the backing driver is in use. This avoids reentrancy problems without disabling system interrupts. Because system code remains resident, it cannot page-fault at interrupt time. Thus, the system response will remain smooth; the cursor code will always run, as will AppleTalk. The only difficulty lies in the fact that Mac VM must treat each type of user code as a separate case. The method for suspending VBL tasks is very different from the one that delays completion routines.

Of course, the best solution to the reentrancy problem is to use a reentrant backing-store driver. With this in mind, the SCSI manager for System 7.0 facilitates reentrancy in the drivers that use it, and the new Apple SCSI driver, also available with the system, will take advantage of it. Mac VM will check the backing driver to see if it's reentrant. If it is, Mac VM will not suspend user code at

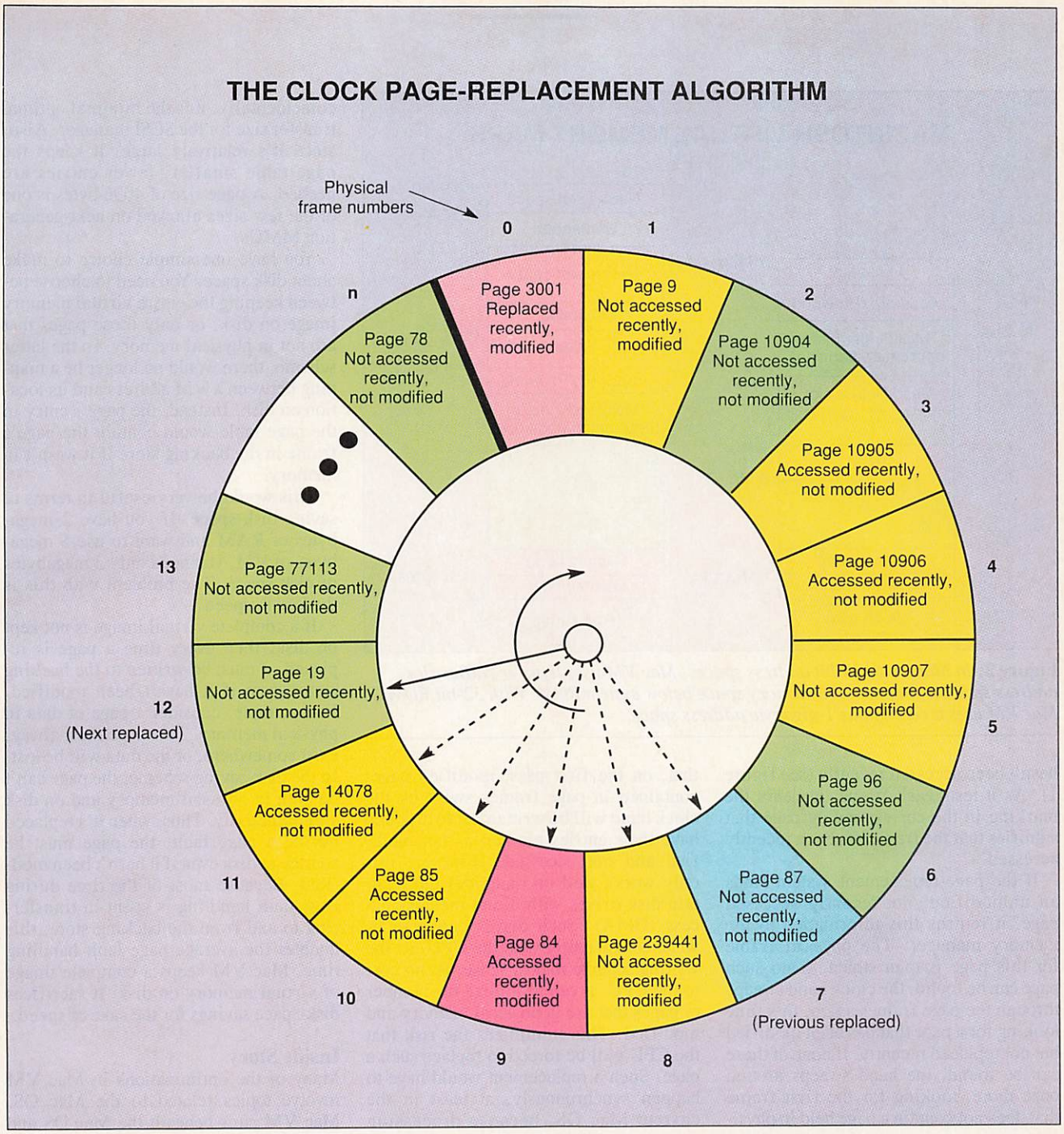


Figure 1: *The clock hand starts from the last frame replaced (blue) and examines each frame to find the first that has not been accessed recently and has not been modified (green). If no such frames exist, the hand does successive sweeps searching for frames (yellow and red) that meet successively less restrictive replacement criteria.*

all. Other types of drivers might be reentrant already; to work with Mac VM, all they would have to do is set the flag that Mac VM checks.

Design Decisions

Mac VM has been performance-tuned using a variety of techniques. It has been tested with different values of the classical VM parameters. For instance, a number of page-replacement algorithms have been tried. Page replacement is the process by which the memory manager decides which page to send to the backing store when it needs to bring a new one into physical memory.

The page-replacement algorithm currently used is a modified version of the Clock algorithm (see reference 1), so called because it simulates the movement of a clock. It involves keeping a circular queue of physical page frames. Implicitly linked and made circular by the algorithm rather than by a data structure, the frames in the queue are accessed sequentially by page-frame number.

Each page frame in memory is automatically marked by the MMU indicating whether it has been accessed recently by the CPU. Mac VM keeps a pointer (known as the clock hand) to the last page frame that it replaced. At a page fault, the pointer sweeps around the frames looking for a page frame that hasn't been modified since it was read from disk and

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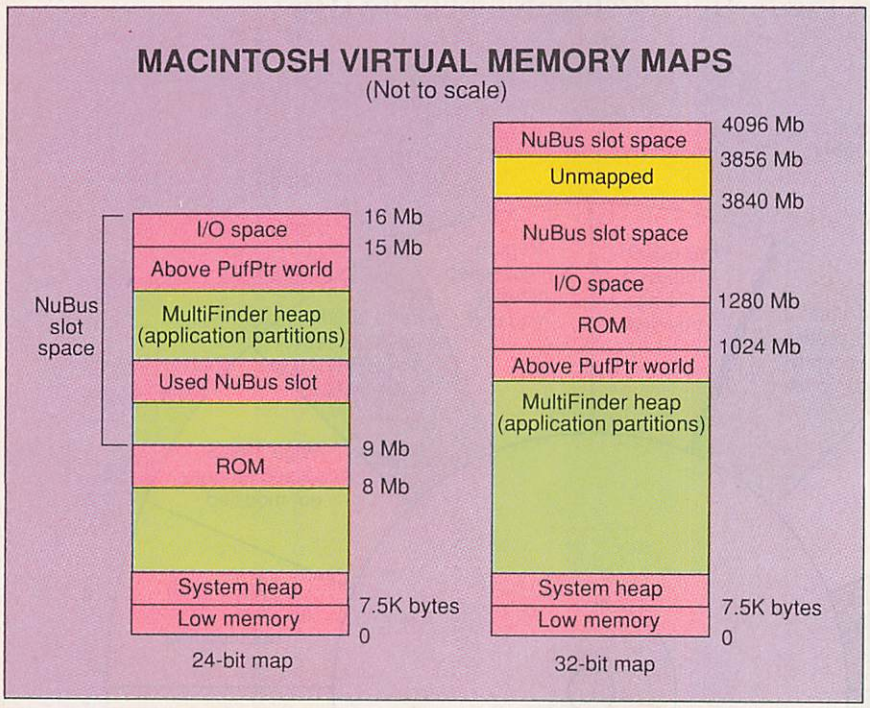


Figure 2: *In Macs with 24-bit address spaces, Mac VM uses leftover NuBus slot address space to augment the memory space below system ROM. With 32-bit ROMs, Mac VM uses a contiguous 1-gigabyte address space.*

hasn't been accessed recently (see figure 1). As it tests each frame, it clears the marking in the corresponding page that signifies that the frame has been recently accessed.

If the page-replacement system finds an unmodified, not-recently accessed page, it returns this information to the memory manager. The physical frame for this page is then stolen. If no such page can be found, the clock hand sweeps through the page frames again, this time looking for a page that has been modified but not replaced recently. If none of these can be found, the hand sweeps around once more, looking for the first frame that does not contain a page held in physical memory, as one in the system heap might be. The held pages are exempt from previous passes as well.

The Clock algorithm is well suited to Mac VM's needs. It is a global page-replacement algorithm; it doesn't require knowledge about different applications and their relative virtual and physical requirements and histories. Also, it's simple and efficient, yet still gives a good approximation to the more complex LRU algorithm. Finally, it is extremely space-efficient. The size of the circular queue is small and is proportional only to the amount of physical memory, not the virtual memory.

The generic Clock algorithm assumes that, on the first pass, modified pages contained in page frames swept by the clock hand will be written out to disk and have their entries marked as not modified and not accessed. However, this only works well on machines that contain disk drives with direct memory access (DMA). Such drives can read or write concurrently with the CPU, so the writing scheme makes sense: At no cost to the CPU, it can minimize the number of pages that are in physical memory and modified. This minimizes the risk that the CPU will be forced to replace such a page. Such a replacement would have to happen synchronously, at least in the current Mac OS, because processing cannot continue until the page fault has been handled.

Because of this, Mac VM's general strategy is to put off writing modified frames until it absolutely must. This is coupled with a variety of techniques that are used to convert modified pages into clean ones. Eventually, Mac VM will have replaceable algorithms, and it will know how to pick one based on the characteristics of the backing driver (the driver transfer speed, latency, and whether it has DMA).

Another parameter that has been tuned is page size. Mac VM currently uses a 4096-byte page size. This size has yielded the best empirical results. Not coincidentally, it is the minimal optimal transfer size for the SCSI manager. Also, since it's relatively large, it keeps the page table smaller; fewer entries are needed. A page size of 4096 bytes is one of the few sizes allowed on next-generation MMUs.

You have one simple choice to make about disk space: You need to choose between keeping the entire virtual memory image on disk, or only those pages that are not in physical memory. In the latter scheme, there would no longer be a mapping between a VM address and its location on disk. Instead, the page's entry in the page table would contain the page's frame in the backing store if it wasn't in memory.

This would be very useful in terms of saving disk space. If you have 2 megabytes of RAM and want to use 5 megabytes of VM, you need only 3 megabytes of disk space. The problem with this is the loss in speed.

If a complete virtual image is not kept on disk, then every time a page is replaced, it must be written to the backing store, even if it hasn't been modified. For example, consider a page of data in physical memory. This page must always exist somewhere, or the data will be lost. In the disk-saving scheme, the page can't be both in physical memory and on disk simultaneously. Thus, when it's replaced during a page fault, the page must be written to disk even if it hasn't been modified. Because most of the time during page-fault handling is spent in transferring to and from the backing store, this doubles the average page-fault handling time. Mac VM keeps a complete image of virtual memory on disk: It sacrifices disk-space savings for the sake of speed.

Inside Story

Many of the optimizations in Mac VM involve topics related to the Mac OS. Mac VM runs beneath the Mac OS and takes advantage of as many peculiarities of the Mac OS as it can. Most of the advantage comes from being able to determine whether the Mac is dependent on the data in a given page. If not, Mac VM can treat such a page as if it had uninitialized data and mark it "uninitialized."

These pages don't need to be written to disk when they are replaced, and they don't need to be read from the backing store when access to them causes a page fault. Therefore, page-fault handling for these pages is extremely fast. And page replacement in general is very fast, too; the modified Clock algorithm actually looks for uninitialized pages first. Ac-

continued

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cordingly, Mac VM is very concerned with finding these "born-again" pages.

Mac VM finds uninitialized pages by sitting in various traps and then analyzing the data passed to the trap routines, as well as the goal of the routine itself. For instance, when an application is launched, it is allocated a large MultiFinder partition. The partition memory may have been used for other purposes, but now that the application is launched into it, Mac VM knows to mark all the pages in the partition as uninitialized. This can also be done when the application quits.

In general, Mac VM will watch whenever a large piece of memory is allocated (`_NewHandle`, `_NewPtr`), resized (`_SetHandleSize`, `_SetPtrSize`), or deallocated (`_DisposHandle`, `_DisposPtr`) using the heap manager. (Note that the heap manager is commonly called the "memory manager" in Macintosh literature. The former term is used to differentiate it from Mac VM, which is a virtual memory manager.)

Mac VM pays very close attention to memory deallocation. Many applications dispose of the memory in which they are currently executing. Typically, they make the `_ReleaseResource` call and then immediately return to code that hasn't been disposed of. This saves a few bytes in resident-code size, since the instructions to dispose of the code segment no longer need to be in memory. Therefore, Mac VM must check to see if the program counter register is within the heap block being disposed of.

Mac VM's general strategy is to put off writing modified frames until it absolutely must.

Mac VM also watches the `_BlockMove` trap. When a large piece of memory is transferred, the previous contents of the destination are overwritten. Thus, the destination memory can be treated as if it were uninitialized, and Mac VM marks all pages completely contained in the destination range as such.

Finally, Mac VM takes advantage of the structure of the user stack. When the trap `_StackSpace` is called, Mac VM guesses that the application is about to use some portion of the rest of the stack (the space between the top of the heap and the bottom of the stack, which grows down). Therefore, it marks all the pages in this area as uninitialized. In addition, when Mac VM replaces a page, it checks to see if the page is completely in the no-man's-land between the heap and the stack. If so, Mac VM can mark the page uninitialized; it need not write the page to disk, even if it's modified.

One more optimization that Mac VM makes is to maximize the amount of VM available in Macs limited to a 24-bit address space (see figure 2). Although up to 16 megabytes is available (2^{24} bytes), the ROM is mapped in, starting at 8 megabytes. Thus, the Mac OS does not allow access to more than 8 megabytes (the motherboard has only enough sockets for 8 megabytes of memory using today's 1-megabit RAMs). The memory above the ROM is mapped to NuBus cards (1 megabyte per card) and to memory-mapped I/O. To increase VM space, Mac VM works around the ROM, literally. It wraps the ROM and used NuBus slots in nonrelocatable blocks in the MultiFinder heap. Then it can use the leftover NuBus slots for VM.

Start-up Action

Before Mac VM starts up, the Mac sees the physical memory as is. After Mac VM is installed, the Mac sees the virtual memory. Because VM addresses don't

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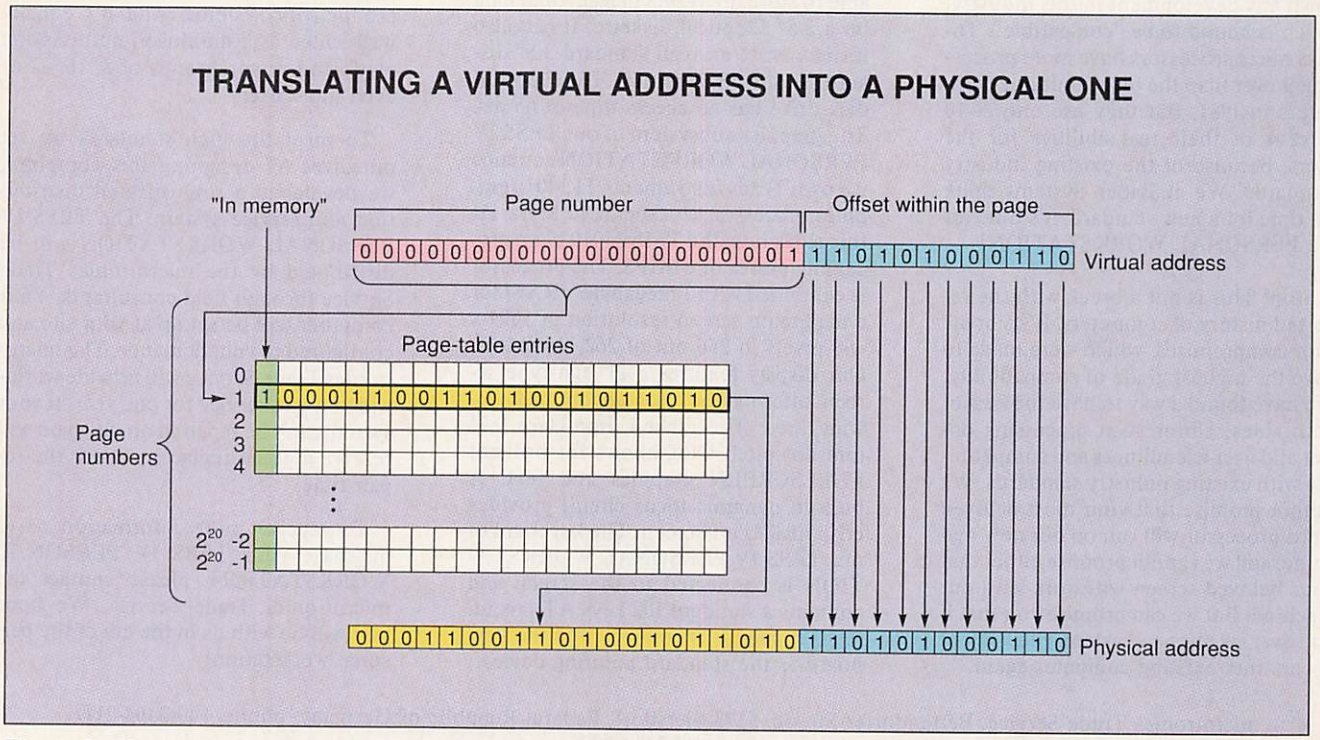


Figure 3: *The page table maps addresses within a virtual page to their corresponding physical addresses. (This example assumes a 4096-byte page size.)*



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necessarily map directly to physical addresses (see figure 3), and because some system and INIT software resides in a memory area bounded between addresses referenced by the low-memory globals `BufPtr` and `MemTop`, it's important that Mac VM be installed before such software. The Mac OS uses `BufPtr` as the upper bound on application memory.

The first piece of replaceable software that runs when the Mac starts up (not including the disk driver itself) is the debugger, if there is one installed. Developers frequently use the debugger MacsBug, but most users use none at all. When Mac VM is enabled (using the Mac VM interface in the Control Panel), it writes the name "Mac VM" to the debugger entry in the boot blocks of the system disk. It also writes the name of the debugger into the entry for the disassembler, which is the second piece of software executed. In this way, the debugger can still run, but only after Mac VM. This is very important, because MacsBug wants to install itself in the high memory above `BufPtr`.

However early the Mac VM installs, a system heap will already exist, since the driver for the system disk, as well as other structures already created by the ROM, must be located there. Therefore, Mac VM must guarantee that all addresses within the system heap are the same in virtual memory as they are in physical. It must ensure that the page-table entries for these pages have identical page-frame virtual-page numbers. This is a bit tricky to maintain, because under MultiFinder the system heap is resized dynamically.

When Mac VM starts up, it must also create the MMU page tables on the fly, since it doesn't know how much RAM is in the system or how large the system heap is.

Programmer Interface

Mac VM provides a limited number of routines available to applications programmers (see table 1). The first three calls are useful for system code that must access application code at interrupt time. The code can hold the memory, access it, and then release it. Since Mac VM keeps a reference count on each page, the unhold will not undo the effect of previous holds on other ranges of memory; the same is true for locking. The `DeferUserFn` call is useful when a routine is called whose size (including the routines it calls) is indeterminate; you can use this instead of holding the memory.

The last four calls are especially useful for smart NuBus cards. These cards can access physical memory, but they don't go through the MMU. Therefore, the card must get the page-table mapping so it can manually make the same translations that the MMU does. It uses the `LockMemory` call to ensure that the mapping doesn't change.

The Mac VM interface has purposefully been made as small as possible. Mac VM itself has been made as efficient and transparent as possible, negating the need for an extensive array of calls.

No Frills

The philosophy behind Mac VM is to keep it small in scope, extremely efficient, transparent, and, above all, compatible with existing software. It's important to limit the scope precisely because of the complexities that compatibility requires. Achieving compatibility with existing applications requires a little empirically derived code and a lot of testing. Compatibility with the Mac OS forces Mac VM to plug up the holes wherever a VM environment has been ignored. Another good reason to limit scope is time.

Future versions of Mac VM will include many more complex features. One such feature is memory protection. Protection ensures that one application running amuck cannot modify the memory of another.

Two problems are inherent in any protection scheme. First, it is difficult to implement a great deal of software without altering it. Second, Mac VM can't differentiate between applications. Therefore, MultiFinder would have to be changed to turn the protection to different applications on and off when switching between them, based on calls provided by Mac VM (`ProtectMemory` and `UnprotectMemory`, probably).

But this arrangement still has problems because system-wide linked lists exist that are threaded through multiple application heaps. For example, the port list keeps track of all open QuickDraw GrafPorts. The code that walks and maintains these lists will touch memory from multiple applications. Still, Mac VM might be able to allow for these types of lists since it catches the access violations and can recognize the offending piece of code. It can subsequently open up the desired protected area and restart the access. This will be very tricky, though, since third-party software unknown to Mac VM keeps such lists, too.

For all this trouble, the gain is not that great. The system heap is a huge area that is shared by all applications. Therefore, an illegal modification to the system heap can still crash the Mac. However, it might be possible to minimize the portion of the system heap that is shared and modifiable.

Another useful feature would be to have separate address spaces. In this scheme, each application has a separate page table and therefore separate mapping between virtual and physical memory. This automatically provides memory protection, but also carries with it all the problems associated with protection. In fact, these problems are now more severe than ever. The linked lists are now impossible to deal with, since some of the addresses (those not referring to objects in the current space) aren't valid, although they might map to valid addresses in the current address space. The type of bug this aliasing causes is very difficult to track down.

The one especially nice characteristic of maintaining separate address spaces is that it would allow for a much larger total amount of VM. Instead of 14 megabytes of VM total, Mac VM could allow perhaps 13 megabytes of VM per application, plus about 1 megabyte of shared memory. For a system running 6 applications, this would amount to as much as 79 megabytes of VM.

However, in the time it would take to implement separate address spaces, 32-bit ROMs will be plentiful, most applications will (hopefully) run with the 32-bit ROMs, and there will be unlimited amounts of VM for all. If this is not the case in the future, then perhaps Mac VM will indeed implement separate address spaces.

Beyond 7.0

Future versions of Mac VM will implement many of the features I've mentioned. The most exciting feature, however, is a tighter integration of MultiFinder and Mac VM. Intrinsically, these two belong together; they represent the key components of a mature operating system: task handling, task communication, and memory management. Integration will allow for a more efficient, elegant, and robust interplay among these components. ■

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Phil Goldman is a member of the Macintosh OS Group at Apple Computer and coauthor of Mac VM. He can be reached on BIX c/o "editors."

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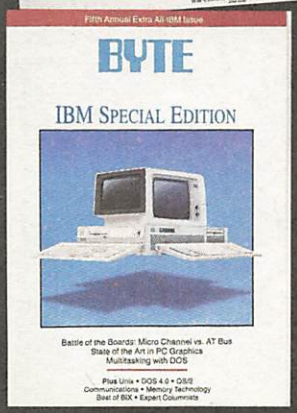
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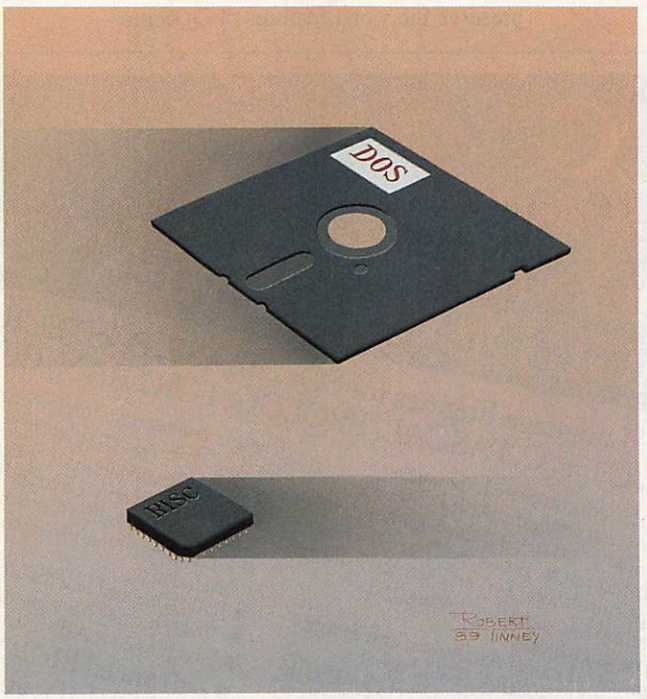
DOS at RISC

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Colin Hunter and John Banning

The advent of 32-bit microprocessors—the 80386, the 68030, and RISC chips—has led to a performance revolution in computer design, affecting workstations, midrange systems, and large multiuser systems. But, ironically, the impact of that revolution has barely been felt on the desktop, where the 16-bit 8088 and 80286—continue to dominate.

RISC-based systems are the performance champs among desktop computers. But their acceptance has been slow—largely because of a lack of applications software. Millions of business users have grown accustomed to the wide range of DOS spreadsheets, word processors, department-level database management systems, and other personal productivity tools. With a multibillion-dollar training and data investment in these programs, DOS users aren't about to switch to RISC if they can't take their software with them. The solution is to let them run their DOS software on RISC machines.



Making DOS software run on RISC machines isn't easy, and several traditional strategies have failed to overcome the portability problem. But a new technology called *binary porting*, which converts the binary 8086 instructions of a DOS program into high-performance RISC code, means hundreds of DOS programs—and millions of DOS users—could soon make the leap to RISC.

RISC Side Story

The first RISC CPUs were developed in the late 1970s and early 1980s by computer researchers at IBM, the University of California at Berkeley, and Stanford University. Instead of following traditional computer designs, which packed as much processing power as possible into each CPU instruction, these computer architects built machines with much simpler instructions that executed more quickly.

The resulting performance gain was so striking that RISC ideas quickly found their way into commercial CPU designs, including the Motorola 88000, the MIPS R2000 and R3000, and the Sun SPARC. These RISC processors use instructions that execute in as few clock cycles as possible, generally only one.

RISC processors also rely on optimizing compilers to generate the fewest possible instructions for each program and to organize the instructions to minimize pipeline delays. The marriage of optimizing compilers and RISC architectures means that a RISC program can often execute much faster than its conventional equivalent, even though the RISC program may be longer.

RISC has the speed—but it doesn't

continued

ILLUSTRATION: ROBERT TINNEY © 1989

have the business software. And duplicating familiar DOS business software on RISC workstations is no simple task. This is not only because RISC processors are incompatible with old-fashioned CISC (complex-instruction-set computer) CPUs such as the 8086, but also because all RISC computers introduced to date are based on the Unix operating system, which is incompatible with DOS.

Meanwhile, millions of PC users have reached the performance limits of their DOS-based IBM PCs, XTs, and ATs, and need more power. RISC workstations would be a logical upgrade path but for the lack of compatibility. How can we bridge this compatibility gap?

Movable Software

For the last 25 years, two main strategies have allowed software written for one computer to run on a second, incompatible machine. *Emulation* means that a program running on the second computer mimics the first computer's hardware and operating system. *Porting* requires rewriting or otherwise modifying the first computer's software to run on the second machine.

The problems with these two approaches have remained the same for 25 years, too: Emulators are too slow, and porting takes too long.

An emulator is essentially an instruction set interpreter. It fetches, decodes, and executes the instructions of the DOS program, one instruction at a time. This process consumes a great many RISC instructions for each 8086 instruction performed, and a great many clock cycles. Thus, an emulator runs DOS software relatively slowly. Emulating DOS code on a RISC is more of a problem because of the mismatch between the 8086 CISC instructions and the RISC instructions. Since each 8086 instruction must be decoded on the fly, there is no opportunity to use the compiler optimization techniques that give RISC its performance advantages.

Emulators have other disadvantages for DOS programs running on RISC Unix systems. They produce a single-user environment on the target system and thus fail to take advantage of the multiuser features of Unix (a real problem for database programs). They also preserve the worst features of DOS programs on the Unix system—for example, keyboard polling loops, which are a real performance drain in multiprocess systems, since idle programs consume CPU cycles by polling the keyboard. And they tend to make very inefficient use of cache memory.

Porting, by contrast, has traditionally required the software vendor to rewrite the source-language version of the program. Porting is great for the user—if it happens. Unfortunately, it almost never does. A port of the program you're interested in is almost never available for the RISC Unix computer you're using. The reasons are partly technical and partly economic.

For performance reasons, most DOS programs contain relatively large sections written in assembly language. Porting a program requires that these sections be rewritten in another language. From that point on, the software vendor must support, maintain, upgrade, and keep in sync at least two versions of the program—or three versions if there's a second port, four if there's a third, and on and on. This rewriting takes a long

continued

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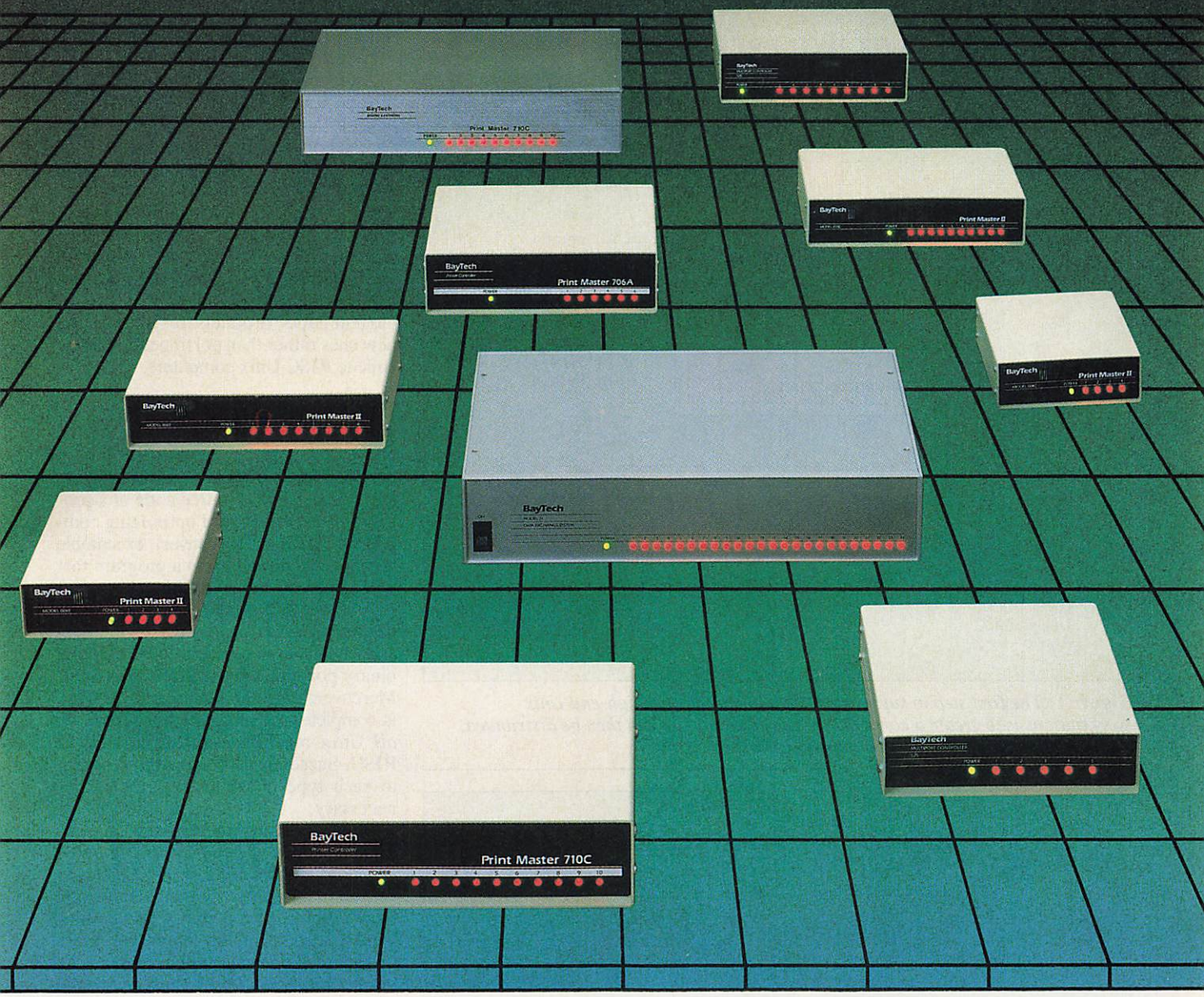
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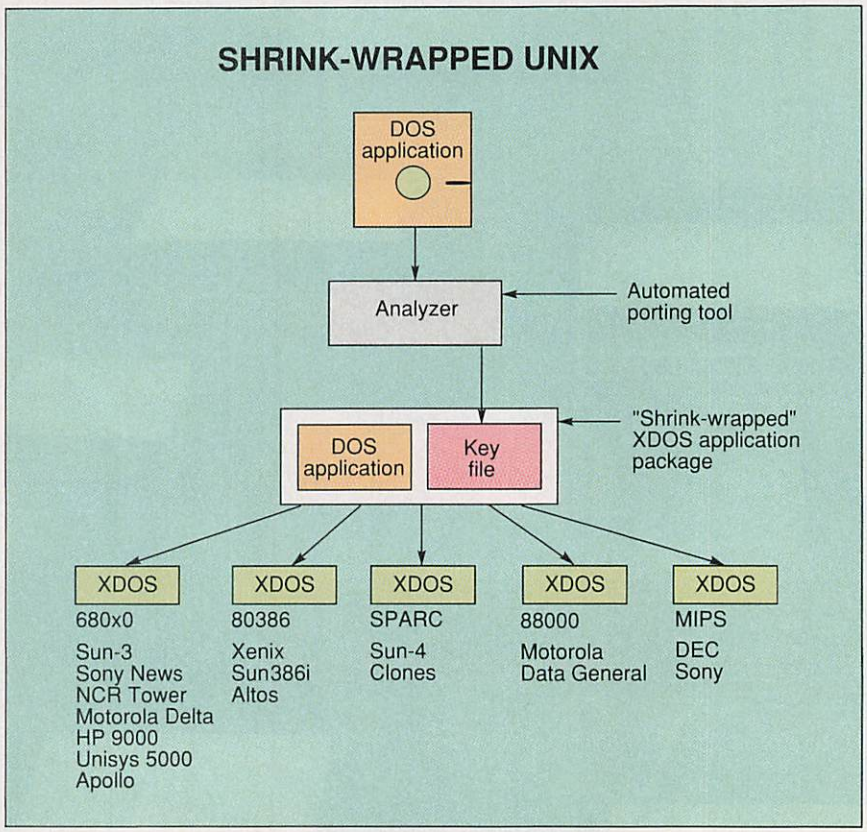


Figure 1: *The first step in supplying DOS applications for high-end Unix workstations is to create a common key file. The key file can then be distributed, with the application, to XDOS-equipped Unix systems.*

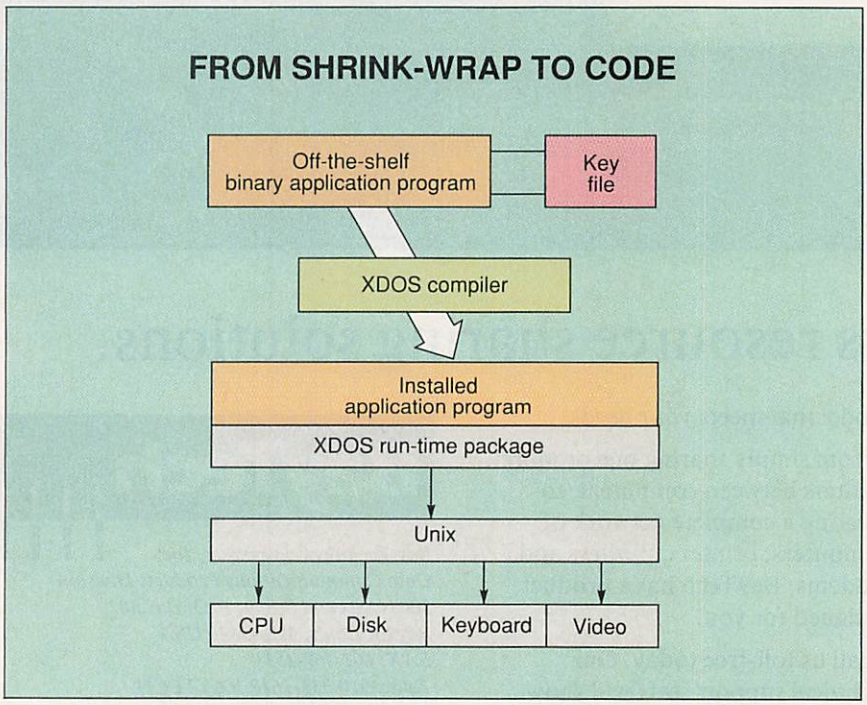


Figure 2: *Step 2 in the binary porting process is to install the application on the target system.*

time—often several years—and maintaining multiple versions of a program is very costly.

And for what? The DOS market has 25 million users. The entire Unix market has 4 to 5 million. But the Unix market consists of dozens of incompatible machines, each requiring a separate port. And of the fewer than 5 million Unix users, only about 30,000 use RISC workstations. Given these market realities, it's no surprise that most DOS software vendors choose to invest their precious engineering resources on upgrading their current DOS products or introducing new ones rather than porting their source code to RISC Unix computers.

The Binary Porting Strategy

Hunter Systems has recently developed a new porting technology called *binary porting*, which does not require making any changes to the source code of a program. It uses advanced optimizing compiler technology to convert executable binary code directly into a program that will run on the target machine.

A binary port produces a program that has the same performance and functionality as a source port, but performing a binary port takes considerably less time. Moreover, once the binary port to Unix is complete, the program is available on *all* Unix machines—CISC as well as RISC. Successively porting the program to each type of computer is no longer necessary.

Binary porting is a two-step process. The first step is *binary analysis*. This step is time-consuming; it corresponds to conventional source porting. However, binary analysis takes only a few days or weeks, instead of the months or years that source porting usually requires. The binary analyzer reads the executable code of the DOS program and performs a sophisticated global data-flow analysis on the program. The analyzer then produces a *key file* containing the results of the data-flow analysis.

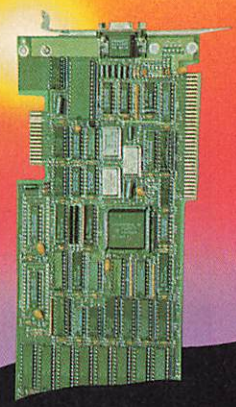
The key file can then be combined in a "shrink-wrapped" package with the original DOS program. This package can be distributed to any Unix user, with almost any type of computer: RISC or CISC, System V or Berkeley Unix. For all practical purposes, the package is a "universal binary" that all Unix machines can run (see figure 1).

The second step is called *binary compilation*. This is essentially an automatic installation process. The end user needs to do it only once, and it takes only a few minutes using a program called a *binary*

continued

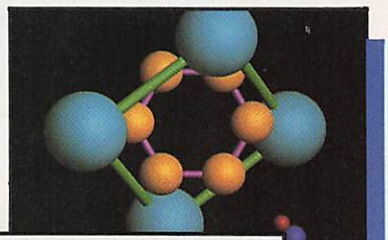
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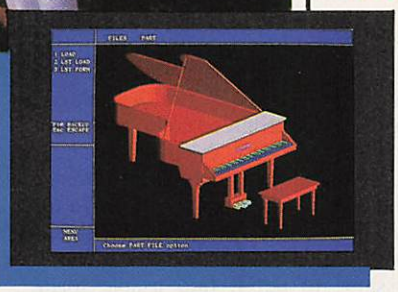


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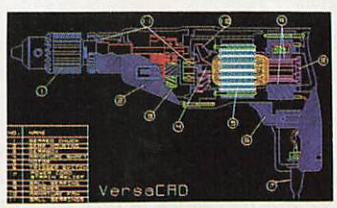




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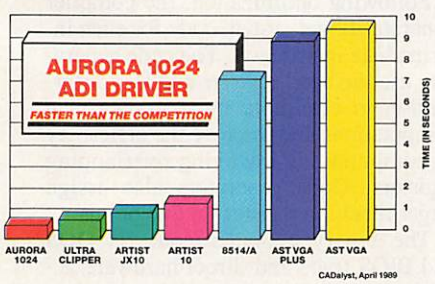


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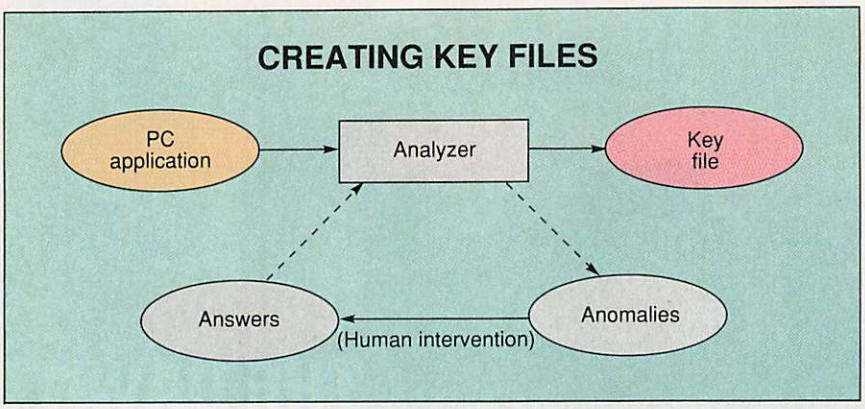


Figure 3: *Creating the key file requires human intervention when execution paths are blocked by anomalies created by self-modifying code and computed jumps.*

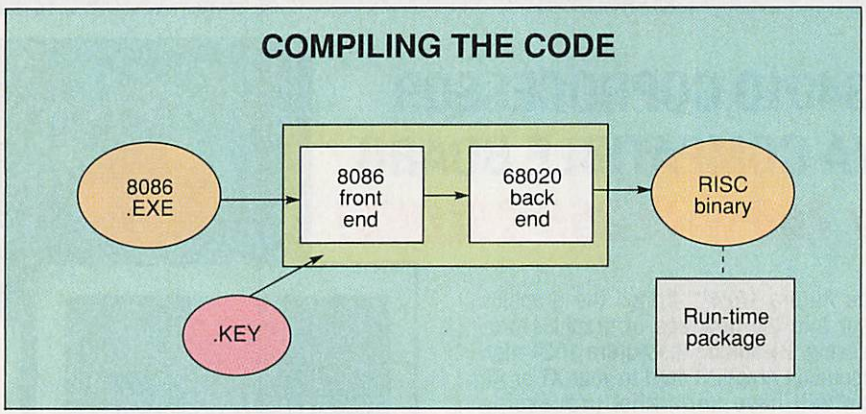


Figure 4: *An XDOS binary compiler is specific to each target machine. Traps and hardware calls in the original application are converted into calls to the Unix run-time library, which in turn calls the appropriate Unix resource to handle these situations.*

compiler. The binary compiler reads the DOS program and key file and converts them into a RISC Unix program, using the key file's flow data for code optimization. The installed program is a real Unix program, with the performance and functionality of a source port (see figure 2).

All architectural and operating-system dependencies of a particular RISC Unix system are incorporated in its version of the binary compiler. The binary compiler can be ported to many different Unix platforms, and each new port inherits all the currently available DOS programs with key files.

Binary Analysis

The basic problem for the binary analyzer is finding all the executable code of the application that it's analyzing and then creating a complete flow graph for the code. Once this is done, the analyzer uses a series of relatively mechanical steps (e.g., global flow analysis) to create the information for the key file.

To find the code and create a flow graph, the analyzer traces execution paths and decodes instructions, starting with the application's entry point. This process will easily find all the executable code in the program, as long as the program doesn't use either self-modifying code or computed jump or call destinations. Unfortunately, real programs use both of these techniques. The binary analyzer handles them by a combination of automatic procedures and human intervention (see figure 3).

When the analyzer encounters these constructs, it generates an anomaly report and proceeds until all execution paths are blocked by anomalies. Then a human analyst must figure out the construction that caused the anomaly and provide the answer to the analyzer. To aid the analyst, the analyzer has an interactive mode in which it prints out the instructions, propagated values, and flow graphs of partially analyzed programs and indicates the parts that cannot be analyzed.

Once the binary analyzer has constructed a complete flow graph for a program, it performs a number of analysis and optimization steps, including live/dead analysis of registers and condition codes. The analyzer uses this information in subsequent optimization steps. The binary compiler will also use it to help generate good code.

Once all this analysis is complete, the analyzer produces the key file. The key file consists mainly of directions to the binary compiler indicating where to decode instructions. The analyzer outputs this information in an order that will allow the binary compiler to process all the application-program files in a linear way. In general, a key file is about 20 percent the size of the corresponding executable application file.

Binary Compilation

The binary compiler uses the information in the key file to convert the code in the original binary image into the machine code of a target system. Each binary compiler is designed for a particular target architecture. The binary compiler contains a front end that reads the DOS program and key file, a back end that generates optimized code, and a run-time library that provides the interface to the Unix operating system (see figure 4).

The compiler starts by reading in the binary application program, using the transformation routines in the key file, if necessary, to put it into usable form. Under the direction of the key file, the compiler then converts the binary code into an intermediate representation, one block of instructions at a time. The compiler first decodes each block of code and then applies any modifications that are called for in the key file. The dead register and flag information from the key file is propagated from the end of the block back through to the beginning. Then the compiler performs a number of optimizations on the intermediate code.

Following optimization, the compiler generates target-system code for each intermediate instruction. The code generators use the dead register and flag information to eliminate unnecessary flag computations and improve the efficiency of computations involving overlapping registers. Code generators also assign target-machine registers at this point.

The binary compiler converts DOS and BIOS traps and direct hardware accesses into calls to the Unix run-time library. This library's functions then

continued

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Our research shows that knowledgeable MIS managers, PC coordinators, and end users simply don't want to think of modems at all.

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By then, you've lost data, time, money, and perhaps an opportunity. Both senders and receivers are dismayed and disarrayed.

Fortunately, there are simple ways to limit this aggravation. Our research suggests a few points to keep in mind.

The cost of the modem is not the modem's cost.

The fixed price of the modem is relatively insignificant. Ongoing costs matter far more.

In the long run, for example, a high-speed modem can save you a small fortune on phone bills. More data sent in less time means less money to the phone company.

You can also save with more reliable and robust modems that communicate over a wide range of telephone line conditions.

Resending data costs both time and money. The less time you spend transmitting data, the more time you have to spend on your business.

Downtime and adaptation time can also cost you dearly.

Be sure to ask if the modems are compatible with their earlier generations. You don't want to start with suppliers who regularly obsolete their own products, or who don't offer you an upgrade path.

Modem support can be a real hassle with the wrong vendor.

Setting up and installing your modem can affect both your budget and your sanity. Many manufacturers forget to make their modems easy to use!

This becomes expensive when you want to start up fast or need to support a large number of users.

Dip switches, on-line help screens, and easy-to-use manuals should be demanded. It also helps to have a quick-reference guide printed on the bottom of the case.

In sticky situations, it's vital to have toll-free support and applications engineering.

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From there, it is exposed to the vagaries of phone lines, various transmission media, and weather patterns.

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All modems are not created equal; some are less sensitive to noise and have better error-correcting protocols.

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Not everyone needs the same modem.

The best way to keep modems from wasting your time and money is to buy them from a reliable supplier with a broad product line. Those with limited lines sometimes try to cram square pegs into round holes.

People with differing applications have differing requirements. Dealing with a broad-line supplier simplifies ordering, reduces training/support time and cost, and limits hassle and coordination.

In the end, if you give enough consideration to choosing the right supplier, you'll hardly have to give modems any thought at all.

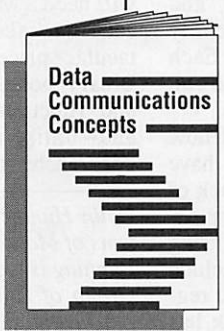
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Listing 1: *The binary compiler converts 8086 code into an intermediate representation, which is then converted into the native code of the target machine.*

```
8086 code:

INC.w  ss:0x8e[bp]
MOV    al, ds:0[si]
XOR    ah, ah
PUSH   ax
CALL   L929

Optimized and scheduled intermediate
code:

[0] VR240 :- op_load.h.algn( VRbp
    0x8e )
[1] VRsp  :- op_sub( VRsp 2 )
[2] VR242 :- op_ext16( VRsi )
[3] VR243 :- op_load.b( VRds VR242 )
[4] VR241 :- op_add( VR240 1 )
[5] :- op_store.h.algn( VR241 VRbp
    0x8e )
[6] VR245 :- op_ext8( VR243 )
[7] VRretaddr :- op_bsr( L929 )
[8] :- op_store.h.algn( VR245 VRsp
    0x0 )

Motorola 88000 code:

ld.hu  r2,r18,0x8e
subu   r19,r19,2
extu   r3,r20,16<0>
ld.bu  r3,r25,r3
addu   r2,r2,1
st.h   r2,r18,0x8e
extu   r2,r3,8<0>
bsr.n  L929
st.h   r2,r19,0

MIPS R3000 code:

lhu    $2,0x8e($18)
addiu  $19,$19,-2
andi   $3,$20,0xffff
addu   $1,$25,$3
lbu    $3,0($1)
addiu  $2,$2,1
sh     $2,0x8e($18)
andi   $2,$3,0xff
jal    L929
sh     $2,0($19)
```

call the appropriate Unix resource to execute the operation.

Optimized RISC Code Generation

RISC CPUs derive most of their performance advantage over CISC processors through code optimization. This is why emulated code cannot realize the same performance as compiled code. The binary compiler, however, is a true compiler; it uses the same optimization and code-generation techniques that other RISC compilers employ. As a result, binary-compiled programs compare favorably with compiled source ports.

Among the optimizations the binary compiler performs are simple peephole optimizations, such as eliminating instructions whose combined result is dead and combining multiple instructions into one. In addition, the compiler performs dynamic register allocation based on a virtual register model. The compiler assigns both 8086 registers and temporary registers (used, for example, in address calculations) to target-machine registers.

The binary compiler also performs code-motion optimizations. The most common of these involves eliminating common subexpression computations. For example, two 8086 instructions in a given block may have the same memory-addressing mode with the same parameters. This is too trivial to eliminate at the 8086 level, but it becomes significant when the addressing-mode computation must be done by several target-machine instructions.

Finally (and perhaps most critically for RISC CPUs), the binary compiler performs instruction scheduling to take advantage of pipeline delays. The compiler moves arithmetic and logical instructions immediately behind jumps and loads to fill the "delay slot" that is available right after a jump or load instruction is executed.

The Analyzer and XDOS

Binary porting may be a promising idea in theory, but how does it compare in practice to the conventional techniques of emulation and porting? We at Hunter Systems have developed not only the binary-porting idea, but also a real binary analyzer (called the Analyzer) and a series of real binary compilers (each called XDOS). We have also created key files for more than a dozen DOS software packages, all of which can now be used on multiuser Unix systems.

With the Analyzer, a human analyst can produce a key file from the binary code of a DOS program in a fraction of the time that a conventional port would require. Since the key file contains no dependencies on the target computer, the same key file can be distributed to any XDOS-equipped system.

XDOS uses the key file to convert the DOS program to its target format. Hunter Systems has ported XDOS to many different Unix platforms based on the 68000 and 80386 CPUs. XDOS for the 88000, MIPS R2000 and R3000, and Sun SPARC will become commercially available over the next few months. Each of these XDOS ports will be able to run all DOS programs with key files.

Listing 1 shows one example of how successful the RISC XDOS ports have been. The listing shows a basic block of 8086 code that has been binary-compiled into 88000 code and R3000 code using XDOS, with optimizations that include instruction scheduling and dynamic register allocation. The original block has five instructions and takes 23 cycles to execute on an 80386. The compiled version takes 9 cycles to run on the 88000 and 10 cycles on the R3000. At the same clock rate, the RISC versions run more than twice as fast.

Making Port

Key files are available for some of the most widely used DOS programs: Lotus 1-2-3, DataEase, dBASE III Plus, Microsoft Word, Multimate Advantage II, Quattro, R:base, BRIEF, Sprint, WordPerfect 4.2 and 5.0, WordStar Professional, and XyWrite III Plus. Hunter Systems is also marketing the Analyzer as a porting tool for software vendors so that key files can be developed for the incredible variety of DOS programs.

In addition, Hunter Systems has submitted the Analyzer and XDOS to the Open Software Foundation as an Architecturally Neutral Distribution Format, or ANDF. The OSF is currently searching for a system by which software vendors can distribute their programs to users of many different kinds of Unix computers without sending source code. (Sending source code to users has two disadvantages: The user must recompile the source code before running it, and the source code may contain proprietary information or techniques that the software vendor wishes to keep secret.) An XDOS key file, along with the original executable version of the program, forms an ANDF package that any XDOS-equipped computer could use.

True 32-bit processors, including RISC CPUs, are just beginning to penetrate the desktop market. Recent announcements by Digital Equipment (DECstation 2100), Data General (Aviion), and Sun Microsystems (SPARCStation 1) represent a milestone in the progress of RISC-based Unix computers into the low-end desktop market, in direct competition with high-end DOS systems.

The new RISC Unix computers will need the wide range of DOS applications software to succeed in the business market, and both users and software vendors will need a way to move their DOS applications to take advantage of RISC's spectacular price-to-performance features. Binary porting offers the performance and functionality that emulators lack, and—unlike a source port—one binary port reaches the entire Unix market. ■

Colin Hunter is president of Hunter Systems of Mountain View, California. John Banning is technical lead of the Compiler Group of Hunter Systems. They can be reached on BIX c/o "editors."

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Clearing the Air

What are the issues to consider with 32-bit software? Will 32 bits solve all your problems?

Bill Blagdan

Choosing all your hardware by how well it can run the software you need is much easier said than done. Many 80386-based computers are currently being used as fast 80286-based machines because the vast majority of popular software applications on the market are compiled for 16-bit execution. 80386-based microcomputers don't have a price/performance advantage over 80286-based PCs unless they are running 32-bit software.

It's true that 32-bit software can move more data in fewer clock cycles and has access to more memory than 16-bit software. These are the factors that provide increased performance for 32-bit applications. However, there are not yet many 32-bit applications available that can take advantage of these capabilities. Understanding the issues as well as the technology surrounding 32-bit software will provide you with the insight you need to make educated microcomputer-buying decisions. Some of the issues include 80386-specific software versus 32-bit software, DOS extenders, various aspects of OS/2, and the 80386SX microprocessor.

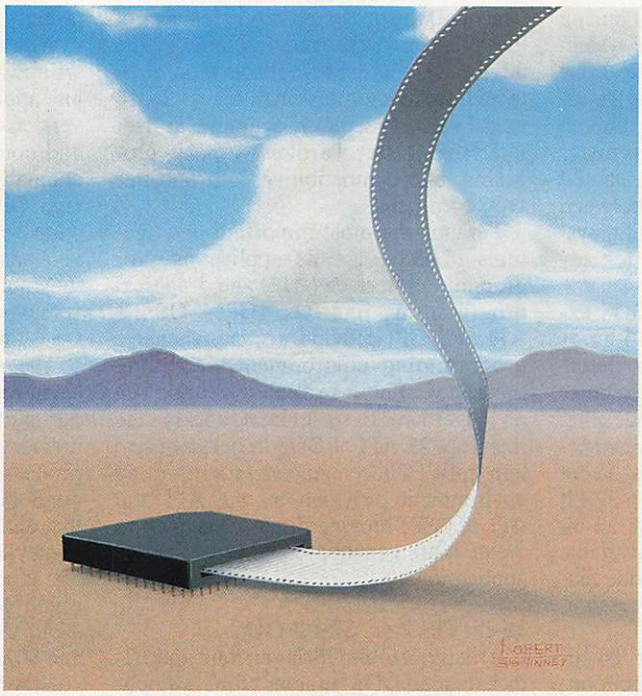


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80386-Specific vs. 32-bit Software

80386-specific software uses features of the 80386 CPU not available on the 8086, 8088, and 80286. But to be truly classified as 32-bit software, applications must execute 32-bit instructions. Thirty-two-bit instructions can manipulate data and memory in 32-bit chunks and provide 32-bit addressing of up to 4 gigabytes of memory.

The 80386's *real*, *protected*, and *virtual 86* operating modes also complicate things. When executing in real mode, the 80386 is operating as a fast 8086 processor executing 16-bit instructions. None of the advanced features of the 80386, including 32-bit instructions, are employed in real mode, and memory access is limited to 1 megabyte. On the other hand, virtual 86 mode enables simultaneous multiple 8086 sessions, each in its own protected memory partition, or *virtual machine*. However, this multitasking of 16-bit sessions occurs only with the proper operating environment to function as an arbitrator.

Windows/386 is specific to the 80386, but it is *not* a 32-bit application. It is a 16-bit application that enables semi-protected multitasking of other 16-bit applications through its windowing graphical interface. It offers only partial protection because it doesn't provide true crash-isolation of its multitasking programs. When one of its multitasking applications crashes, Windows/386 lets you save the data in the other multitasking sessions before rebooting. It's also important to note that Windows/386

continued

doesn't run concurrently with, or allow multitasking of, 32-bit DOS applications. This is because they run in the protected mode of the 80386, which conflicts with the Windows/386 memory management structure.

The 80386 microprocessor's protected mode provides the means to access the advanced features of the 80386, such as 32-bit instruction execution, 32-bit addressing, and multitasking of 32-bit applications. However, to take advantage of all the features of the 80386's protected mode, operating systems and software applications must be written for it. Currently, DOS is a real-mode operating system that doesn't permit protected-mode execution. So, how do you create 32-bit DOS software that runs in protected mode and takes advantage of the advanced features of the 80386?

DOS Extenders

DOS extenders are software tools used to create applications that run partially in protected mode under DOS. An *extended application* is only partially protected because it switches back and forth between real and protected modes during execution and can crash the whole system when it is in real mode. Applications created with DOS extenders look like ordinary DOS programs. However, hidden from the user is a kernel that starts under DOS, switches the processor to protected mode, and provides an interface between the application and DOS operating-system services, via a keyboard, for example.

To produce software with a DOS extender, you need a compatible 16-bit or 32-bit compiler. The compiler determines whether the application executes 16-bit or 32-bit instructions. To develop software that exploits the 32-bit instructions of the 80386, you need a 32-bit compiler that is compatible with a 32-bit DOS extender. Both 16-bit and 32-bit versions of DOS extenders are available to take advantage of protected-mode features of the 80286 and 80386 processors, respectively.

If you can compile familiar 16-bit DOS applications for 32-bit execution, why are there so few 32-bit versions of 16-bit software packages? First of all, DOS extenders have some very important limitations. When executing an extended DOS application, all DOS system services, including I/O, must run in real mode. Therefore, every time an extended application performs an I/O instruction, such as reading the keyboard, it switches to real mode, performs the I/O function, and returns to protected mode. This switching between modes costs valuable clock cycles and decreases application performance.

Second, you may have to significantly rewrite 16-bit source code to run in protected mode. You can port well-behaved software from the 16-bit DOS environment to a 32-bit, protected-mode, extended-DOS environment.

Third, the market for an 80386-only product is much smaller than for an 80286/80386 product due to the massive installed base of 80286 machines. Many of the 32-bit DOS applications available today are mainframe or minicomputer software ported to the 80386 and recompiled with a DOS extender. And many of them address small, vertical markets and don't offer any solutions to the broad base of IBM-compatible personal computer users.

The OS/2 Challenge

Another factor contributing to the small number of 32-bit DOS applications is the challenge to create OS/2 versions of popular programs. OS/2 is a 16-bit operating system that was designed to take advantage of all the protected-mode features of the 80286 microprocessor. Some of the advanced features include true protected-mode multitasking, access to 16 megabytes of memory, a graphical user interface, better harmony among programs, and compatibility with familiar DOS commands.

Perhaps the most important new features of OS/2 are its application programming interface (API) and graphical programming interface (GPI). OS/2's API and GPI provide a comprehensive programming environment, including thousands of built-in function calls. You no longer have to set up interrupts via the interrupt 21 API of DOS to perform system calls. The enhanced programming environment provided by the API and GPI of OS/2 provide the tools needed to create more functional and easier-to-use applications.

16-bit OS/2 vs. 32-bit DOS

Currently, 16-bit OS/2 versions and 32-bit extended DOS versions of many popular software packages are under development. For those packages with *both* versions under way, you might expect the 32-bit version to be faster. Tests have shown, however, that 16-bit Paradox OS/2 outperforms 32-bit Paradox/386. Unlike DOS, which is a real-mode operating system, OS/2 runs exclusively in protected mode. Thus, OS/2 applications don't waste time switching between real and protected modes. So, if you compare different program incarnations, you must do it carefully.

A 16-bit OS/2 application also may outperform a 32-bit DOS version because of OS/2's ability to use *threads*. A thread is the smallest unit of execution within an OS/2 application. Every OS/2 application has at least one thread, but several threads can run at the same time.

OS/2 programmers can use these threads to create applications that employ multitasking within themselves by overlapping program functions with user input. For example, an OS/2 spreadsheet program could perform recalculation as a separate thread when you hit the Recalculate key, freeing up the keyboard so you can go on working with the spreadsheet.

OS/2 vs. OS/2 for the 386

The production release of a new 80386-specific, 32-bit version of OS/2, tentatively called OS/2 for the 386, is scheduled for the first half of 1990. Two important issues must be addressed when comparing this version with the original: 32-bit instruction execution and segmentation.

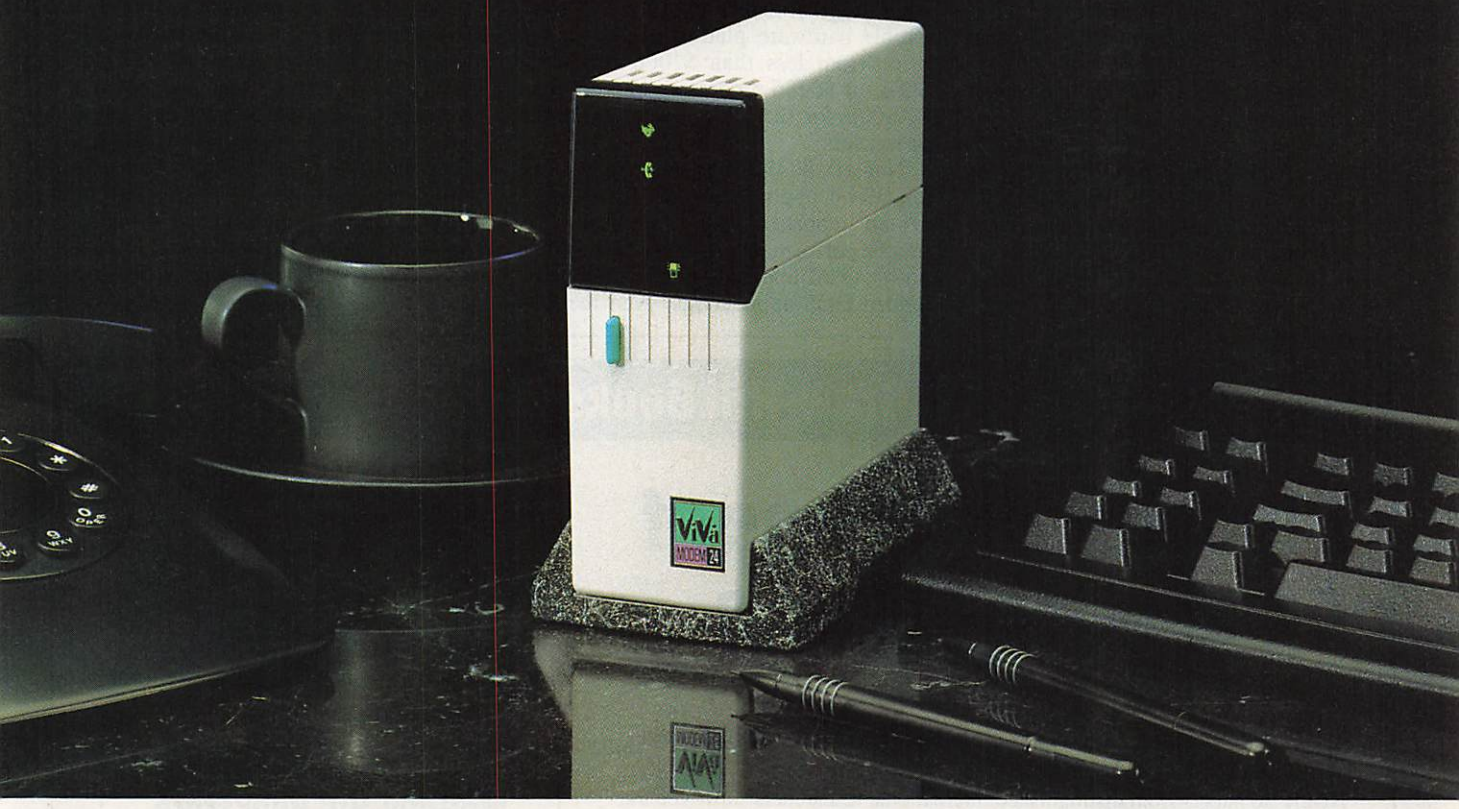
Although 32-bit instruction execution will be available under OS/2 for the 386, any applications released for the current version of OS/2 will have to be rewritten and compiled with a new 32-bit OS/2-compatible compiler to gain this advantage. Given this complication, many software vendors may never release 32-bit versions of OS/2 applications. Instead, they may simply package them as 16-bit versions to run under both OS/2 and OS/2 for the 386.

The second important issue to consider regarding OS/2 and OS/2 for the 386 surrounds segmented versus linear memory addressing. The 80386 microprocessor's memory architecture supports a linear, or "flat," memory model that enables direct addressing of up to 4 gigabytes of memory. With a flat memory model, you can set up one huge 4-gigabyte code-and-data segment and avoid the extra work required by 8086 and 80286 segmented architectures.

However, memory segmentation is required with a protected-mode, multitasking operating system such as OS/2 or OS/2 for the 386. Multiple code and data segments are kept for each application running concurrently in a multitasking environment to enable hardware-assisted protection by the microprocessor. Therefore, while OS/2 for the 386 won't do away with segmentation, it will enable you to use data and code segments that

continued

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The 80386SX Microprocessor

The 80386SX is a low-end version of the 80386 that can run 32-bit software but is hindered by a 16-bit data bus. In most cases, the 80386SX operates in the same 16-bit environment as the 80286.

However, tests show that the 80386SX is slower than the 80286 when running 16-bit applications, and slower than the 80386 when running 32-bit applications. Compared to the 80286, the 80386SX is also slow at multitasking 16-bit applications under OS/2.

Easier Said Than Done

Software continues to be one of the most important factors to consider when purchasing personal computers. You have a wide range of choices of IBM PC–compatible hardware platforms, ranging in price from less than $1000 for 8088, 8086, or 80286 processors to more than $10,000 for the latest 80386 or 80486 processors.

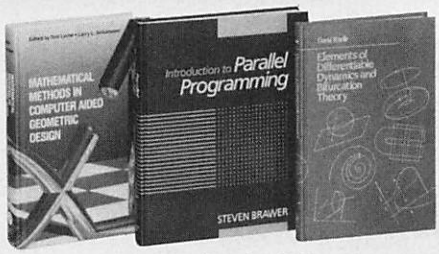
Not all 80386-specific applications are 32-bit applications. DOS extenders are an important option to consider, as are the performance differences between 16-bit OS/2 applications and 32-bit extended DOS applications. And the new 32-bit version of OS/2 has its advantages as well.

Which IBM PC–compatible personal computer platform you choose should be determined by two primary factors: the software you need, and the hardware's ability to run that software effectively. Just because a program claims to be "32-bit software" doesn't mean that it is the best program to run your particular application. ■

Bill Blagdan is a product marketing engineer at Advanced Micro Devices in Austin, Texas. He can be reached on BIX c/o "editors."

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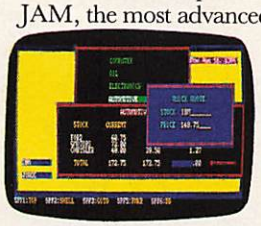


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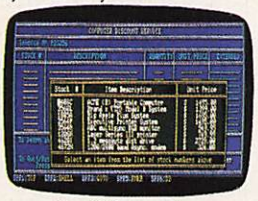
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Suite 203
San Jose, CA 95131
(408) 433-9208
Abacus 386/25..... $1200
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Inquiry 1182.

AST Research
2121 Alton Ave.
Irvine, CA 92714
(714) 863-1333
Premium FASTboard/386 ... $1095
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Flowerbranch, GA 30542
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(404) 967-2077
Daystar 33/030..... $2995
33-MHz 68030 processor for the Mac SE. Optional 68882 math coprocessor for $900.
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Dove Computer
1200 North 23rd St.
Wilmington, NC 28405
(800) 622-7627
(919) 763-7918
FastNet LAN 020..... $1499
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Peabody, MA 01960
(508) 535-7510
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(617) 890-0880
HyperCharger 020..... $999
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(503) 681-8080
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Ann Arbor, MI 48105
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(313) 930-9000
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XL 20..... $995
XL 25..... $1695
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Levco Sales
6181 Corner Stone Court E,
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San Diego, CA 92121
(619) 457-2011
Prodigy SE..... $1499
16-MHz 68020 processor board for the Mac SE with 1 to 4 megabytes of memory.
Prodigy 4..... $2995
16-MHz 68020 processor board for the Mac Plus with 4 megabytes of memory and a SCSI port.
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Novy Systems
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Edgewater, FL 32032
(904) 427-2358
MAC20MX Series
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68020 accelerators for the Mac Plus and Mac SE; available with 1 to 4 megabytes of RAM.
Inquiry 1191.

Orchid Technology
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Fremont, CA 94538
(415) 683-0300
Jet 386..... $1299
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Inquiry 1192.

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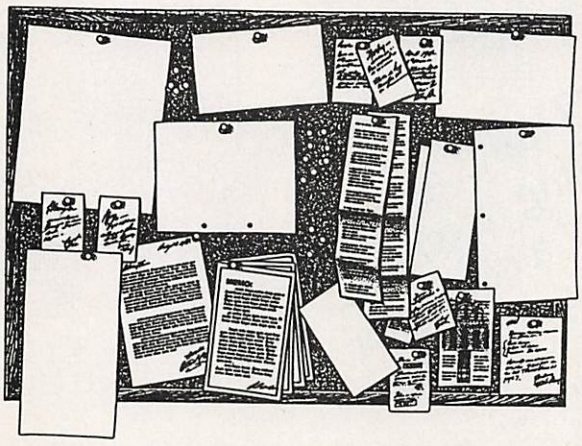
Norcross, GA 30093
(404) 923-6666
Quad 386XT
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20 MHz..... $2295
80386 processor board for the IBM PC, XT, and compatibles; available with 1 to 3 megabytes of memory.
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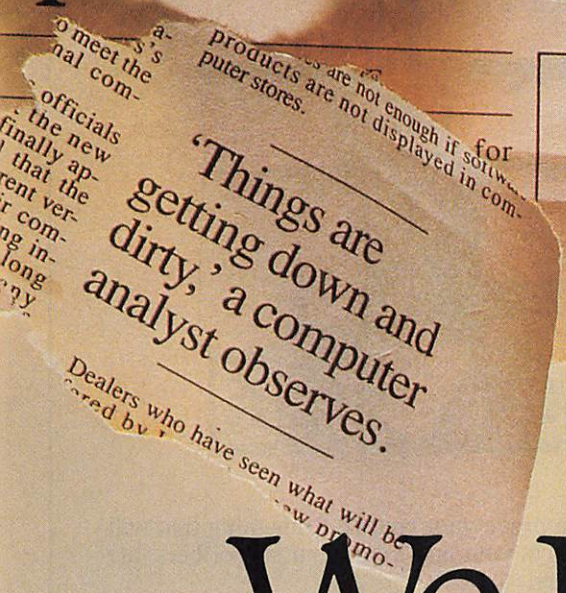
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Spreadsheet Rivalry Heats Up







We Interrupt T War For This Im

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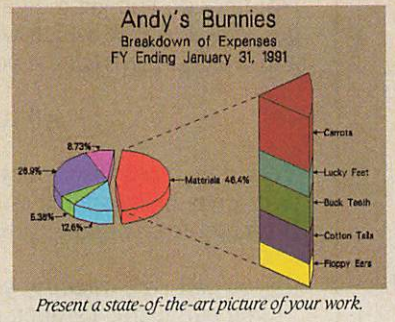
There is, at last, a viable alternative to war: revolution.

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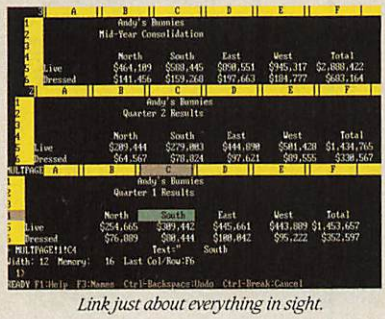
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Catch bugs before they come back to bite you.

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to be precise. Linking either in memory or on disk, either pages of the same spreadsheet or independent, either SuperCalc5's files or Lotus® 1-2-3®'s.

Which brings us to the "L" word. SuperCalc5 not only reads and writes Lotus® 1-2-3® files, it totally coexists with Lotus.

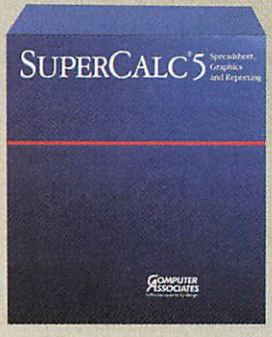
Letting you easily move 1-2-3 macros into SuperCalc5 and back again. Even toggling between menus is a snap for SuperCalc5.

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Which now brings us to the "E" word. Unlike Excel, SuperCalc5 runs on all IBM® and compatible computers but also takes full advantage of 286 and 386 machines when *you* decide to make that transition.

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Which finally brings us to our admittedly biased outlook for the much touted spreadsheet war.

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FY Ending January 31, 1991
Unaudited

	This Year	Last Year
Revenue:		
Sales		
Live	$5,778,453	$4,099,672
Dressed	$1,444,775	$675,333
Sales Discounts	($434,990)	($475,124)
Rent-a-Rabbit Fees	$679,991	$274,357
	$7,468,229	$4,612,218
Cost of Sales:		
Opening Inventory	$9,662,351	$5,676,712
Purchases	$109,814	$4,229,164
Freight in	$56,727	$43,345
	$9,828,892	$9,949,218
Ending Inventory	$7,334,310	$8,662,767
Cost of materials	$2,494,582	$1,286,451
Direct labor	$1,447,951	$1,677,243
Employee benefits	$289,590	$335,449
Ranch supplies	$679,444	$610,142
Total Cost of Sales	$4,911,767	$3,909,901
Gross Profit	$2,556,462	$1,702,317
Less selling, general and admin expenses	$469,887	$490,774
Earnings (loss) from operations	$2,086,575	$1,211,543
Other income and expense:		
Interest income	$11,309	$9,765
Other income	$17,899	$15,666
Gain (loss) on sale of fixed assets	($379)	$0
	$28,829	$25,431
Provision for income taxes:		
Current income taxes	$1,043,287	$605,772
Deferred income taxes	$0	$0
	$1,043,287	$605,772
Net earnings (loss) for period	$1,043,287	$605,772

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A New Twist on an Old Technology

Helical-scan technologies—including DAT—provide tape storage systems with gigabytes of data storage

Jay Bretzmann

Because today's personal computers are powerful enough to run large and complicated applications, users need enormous storage capacity. Helical-scan tape storage offers multi-gigabyte capacities that most other personal computer storage systems can't achieve. Helical-scan techniques also provide higher transfer rates and cost-efficient, removable data storage. Currently, users can't obtain these benefits from tapes recorded by traditional techniques.

By Any Other Name

Helical-scan recording isn't really new. What is new is the name and the fact that, until about 16 years ago, this technology wasn't used for computer applications.

Otherwise known as *slant-track* or *diagonal* (versus *longitudinal*) recording, helical-scan technology has been used in video recording applications since 1956, when Ampex introduced the first commercial videotape recorder. Adaptations of the technique for computer data storage began about 18 years ago. Once again, Ampex was the pioneer when it introduced its Terabit Data Recorder in 1972, but IBM drew significant attention to the format.

In 1973, IBM purchased the rights to the technology from Ampex for $13 million, and in 1974, it introduced the IBM 3850 as the ultimate solution to data-storage problems. The aim was to eliminate the manual handling (and resultant human error) associated with tape reels and disk packs. The 3850 could essentially put all your data on-line by storing between 35 and 472 gigabytes. The 3850 was able to record this much data by using helical-scan technology and a large-width tape.

For various reasons, including the move from batch to transaction processing, in 1985, IBM discontinued support of the 3850. Generally, there was a move to smaller machinery and increasing electronic (versus mechanical) complexity. As video recording technology evolved, tape widths shrank, recording heads started to slant, and, by and large, companies began developing a helical tape format known as VHS, which was adopted first for commercial and then for consumer video recording.

As engineers experimented with this technology for data-storage applications, the form factor changed (from 8-inch to 5-inch), limiting the acceptance of this format and causing most serious tape suppliers to shy away from its use.

Mostly Good News

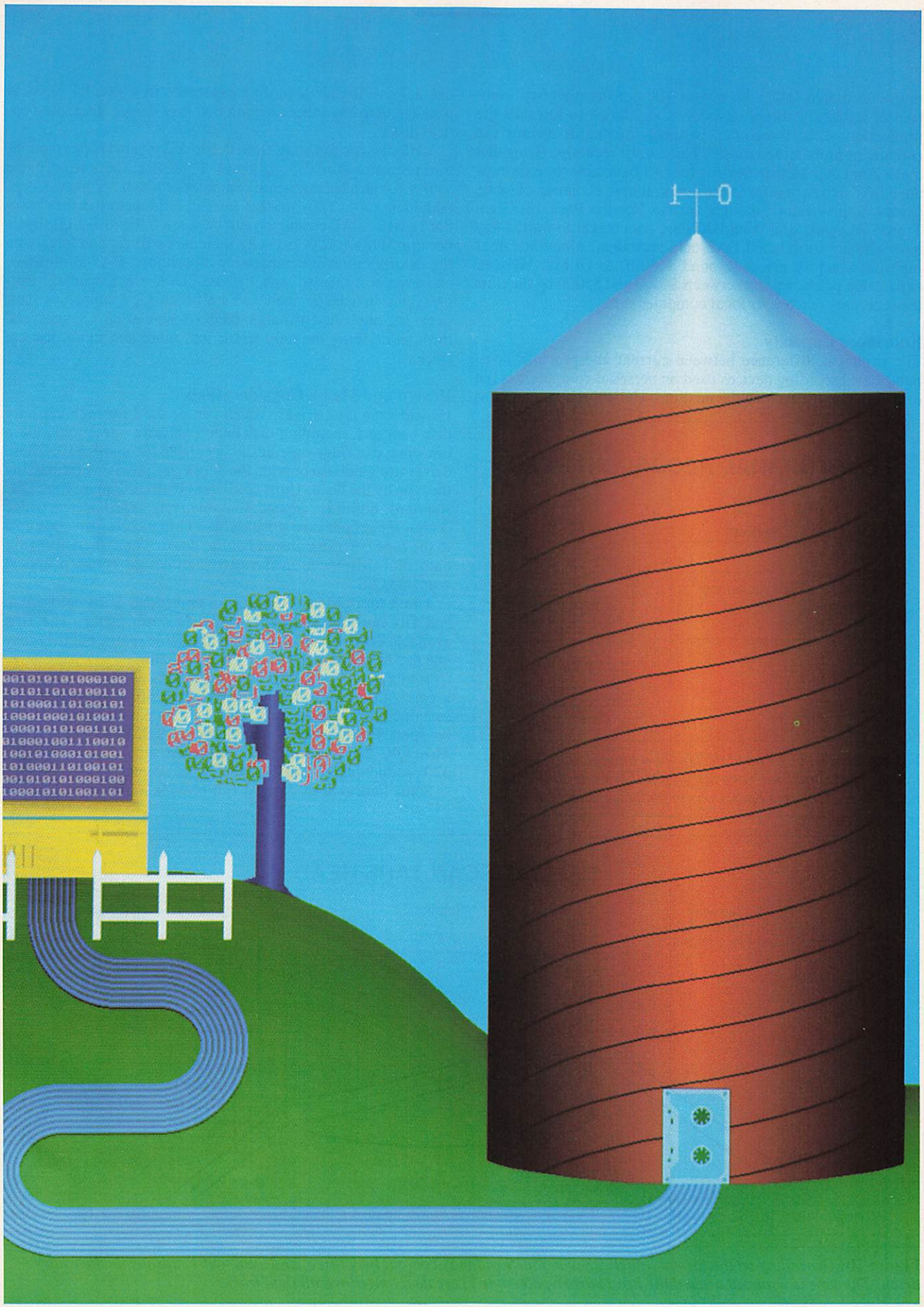
"Conventional" tape devices write data longitudinally in a pattern parallel to the edge of the tape. In helical-scan recorders, the recording head tilts at a slight angle, causing the tape to wrap around it in a barber-pole fashion. The spinning head writes data tracks as portions of a continuing spiral or segments of a helix—thus the name. Figures 1a and 1b show the differences in track layout and head design for typical recording devices, such as the quarter-inch drive and the helical-scan product.

The first helical-scan tape machines used 2-inch-wide tape, but now helical-scan products are produced in several widths, including 4-mm digital audio tape (DAT), 8-mm, quarter-inch, half-inch, and a few nonstandard widths. The 4-mm DAT, which is potentially one of the best tape-storage formats, has been plagued with ongoing controversy that has held back its implementation. (See the text box "The DAT Controversy" on page 384.) DAT technology involves the ability to put well over 1 gigabyte of almost totally pure data on a cassette the size of a credit card (see "DAT Drive Eases Mac Backups" on page 225).

Of course, as with any beneficial technology, along with the advantages come some trade-offs. For instance, as yet, not all the helical-scan standards are in place. Some are here and others are on their way, though, via organizations such as QIC (Quarter-Inch Cartridge) and DDS (Digital Data Storage), which make recommendations and decisions concerning standard tape drive features and formats.

An additional problem has been that because sound can be

continued


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reproduced onto DAT with almost 100 percent integrity, compact disk manufacturers introduced legislation to forestall the production of DAT recorders without safeguards against the copying of prerecorded music. Thus, until recently, firms that make computer storage devices haven't been able to mass-produce DAT drives to offer to the public at low, economy-of-scale prices. Some vendors, though, such as Hewlett-Packard, GigaTrend, Wangtek, and WangDAT, are not content to wait. They have already introduced DAT data recorders, albeit at rather high introductory prices (around $1500), to OEMs. You can expect that prices will be between $4000 and $5000 by the time the recorders reach your local computer store.

Enormous Capacity

The principal difference between current and previous computer tape recording devices used on personal computers is the orientation of the data on the medium. Helical-scan techniques can achieve higher recording capacities in a smaller physical package than any other computer storage device, including optical disks.

VHS devices can store from 2.5 to 5.2 gigabytes per tape; 8-mm products store 2.3 gigabytes. Presently, there is only one source for purchasing 8-mm computer products: Exabyte Corp. (Boulder, CO). Thus, in this format, a de facto industry standard exists. DAT products yield between 0.9 and 1.3 gigabytes per unit. Future DAT capacity increases will depend largely on the incorporation of compression algorithms. DAT minimizes, and even eliminates, capacity loss due to track spacing. Progressions in quarter-inch and half-inch tape capacities have been accomplished through media formulation changes and through dividing the tape width into more and more discrete tracks.

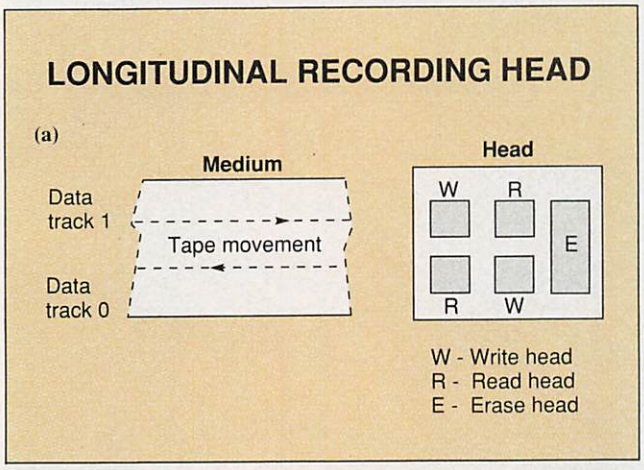


Figure 1a: *The basic head design for a longitudinal, single-track tape recorder uses two sets of parallel write-and-read heads to enable drive operations in both tape directions.*

Design and Media Considerations

Helical-scan tape drives, which can be used for high-capacity disk backups, including distributed network operations, use a low-cost, cartridge-tape design available for under $10. These drives use guides to provide the necessary precision for passing the tape by the head. Units consistent with the longitudinal QIC standard, however, depend on a relatively expensive cartridge design for proper tape positioning. This mechanism adds cost to the tape cartridge instead of the drive. Thus, there is a fundamental difference in the cartridge design between helical scan and QIC.

The 8-mm product features an embedded SCSI connection and fits into the 5¼-inch full-height form factor. The first available DAT drives will occupy the same space, but they may one day be made in the 3½-inch form factor.

While moving the tape at a rate of almost one-half inch per second, the 8-mm product achieves a 246K-byte-per-second sustained data transfer rate. DAT designs pass the tape at similar speeds and feature a maximum of 192K bytes per second. Most QIC drives achieve 90K bytes per second, with the QIC 320 products achieving 240K bytes per second.

Some helical-scan designs can provide a high-speed search

continued

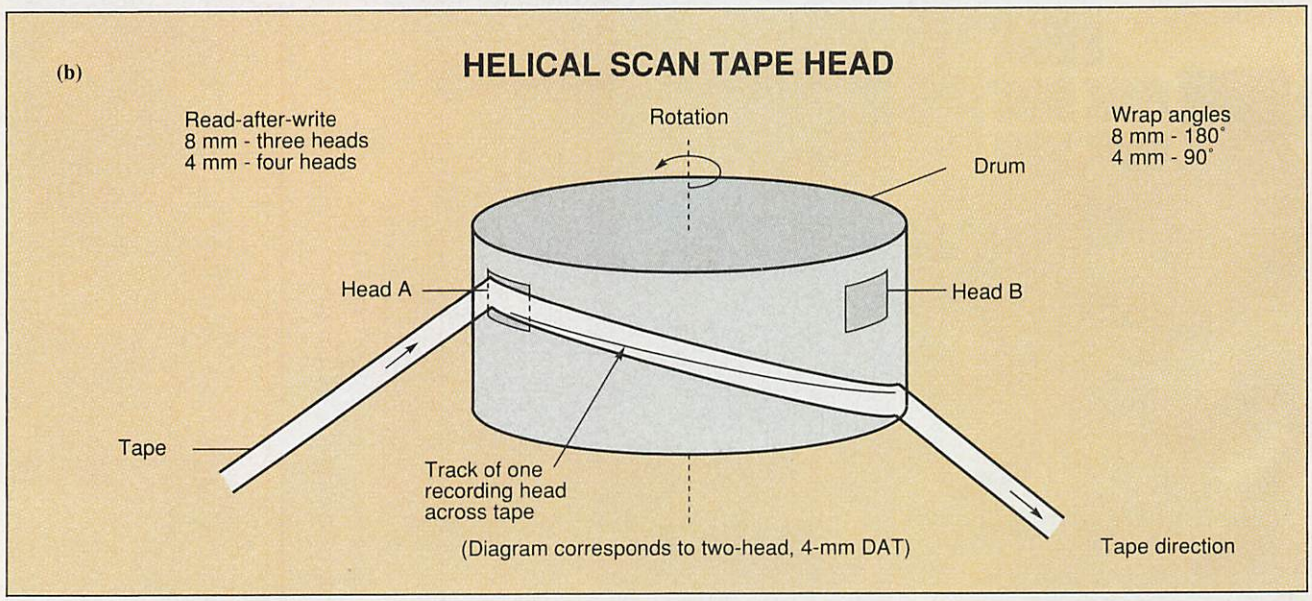
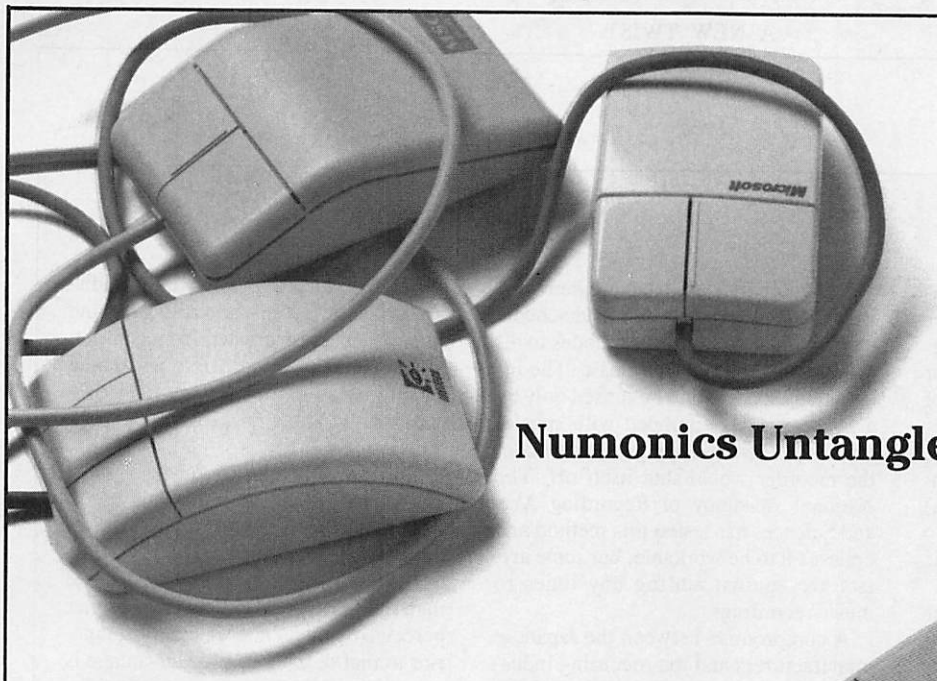
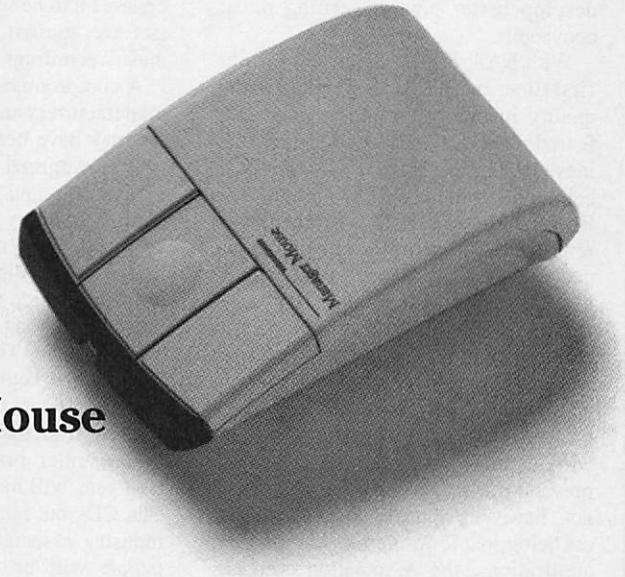


Figure 1b: *Depending on the format, a helical-scan tape head may contain two, three, and even four heads inside the rotary drum. The tape is wrapped around the head barber-pole-style to create a longer overall data track.*



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The DAT Controversy

Until recently, the recording industry associations have blocked Japanese companies' attempts to import digital audio tape (DAT) recorders for consumer use. The issue has been one of mechanically preventing the reproduction of compact disk (CD) recordings. Organizations such as the Recording Industry Association of America (RIAA) are lobbying for more time in order to develop better laws governing music copyrights.

With DAT, consumers would, for the first time, be able to reproduce digital-quality music and sounds. Thus, it is feared that a new rash of illegal recordings would be triggered, with the focus being on the lucrative CD market. The RIAA is also against the introduction of rewritable CDs or any other device capable of reproducing professional-quality recordings.

Citing fears of lost revenues from bootleg music reproductions, the RIAA is threatening to take legal action against any company selling a DAT product in the U.S. consumer market without including circuitry that would prevent mass copying. The RIAA is not, however, opposed to DAT recorders being sold for professional recording applications; the Association even has one of its own.

A CBS attempt to thwart would-be pirates has been quashed by the National Bureau of Standards (NBS). This technique blanked out the audio signal around 3840 Hz. If special decoding circuitry detected this "notch" for 15 seconds, the recording would be halted for the next 25 seconds. The NBS found that the scheme didn't work between 40 percent and 90 percent of the time, and that certain harmonics associated with violins, synthesizers, and organ music tended to activate the copy protection.

R. Miller & Associates of Glenview, Illinois, is developing a second scheme involving the addition of subcodes to all commercially produced music. The inaudible subcode could be sensed only by a DAT recorder equipped with special circuitry. Having detected the subcode, the recorder would shut itself off. The National Academy of Recording Arts and Sciences has tested this method and believes it to be workable, but some artists are against adding any tones to music recordings.

A compromise between the Japanese manufacturers and the recording industry may have been reached. The Japanese have agreed to add extra circuits to defeat unlimited copying, while the recording industry has eased restrictions against copying original recordings. In this scheme, a digital subcode identifies the input source of the information and prevents copying except from the original DAT tape. The category code is located at the beginning of the tape and therefore does not interfere, add, or subtract from the music.

Consumer products arriving early next year will have the ability to duplicate CDs but not DAT recordings. The industry associations believe that few people will be interested in creating multiple copies of the same source material for distribution.

Significantly less turmoil was raised over the introduction of the analog cassette recorder years earlier. Many of these units were unable to fully reproduce an LP's range of sound. In addition, their recordings contained "tape hiss," and each playback added to the degradation of the signal quality. Consequently, the effect on record sales was relatively slight.

No such undesirable characteristics are associated with digitally recorded music. The recording is virtually indistinguishable from the original, and since the music is created from converting a digital bit stream into an analog signal instead of amplifying previously recorded modulations, each playback remains crisp.

Until now, the music industry has had a monopoly on digital recording methods. It has been able to charge a premium for the CD format, which is less expensive to produce and distribute than the vinyl LP. The CD has a higher perceived value since its signal is superior to that of the LP. This advantage is certain to diminish in the years to come, however, as digital circuits continue to replace earlier analog designs.

In some ways, the RIAA's struggle resembles the efforts of software developers to devise effective copy-protection schemes. Over time, most major developers abandoned these programs in favor of an honor system.

Right now, unless you operate a professional recording studio, the only place you can buy a DAT recorder for home use is in Europe and Japan. To date, some 25,000 units have been sold worldwide, mostly to professional recording studios. Prices are high, around $3500, because of the small volumes that manufacturers are currently producing. The economies of scale necessary to reduce unit prices to an affordable level are only possible with the product's acceptance in the U.S. market.

Computer storage versions of DAT are already becoming available from a wide group of manufacturers. This device holds much promise for users seeking to achieve unattended backup operations on desktop computers. But until the products are qualified by system OEMs, volumes will remain low and prices high.

capability. DAT technology provides two subfields per track containing information that can be indexed and read many times faster than the actual tape speed. Any spot on the tape can be accessed in 20 seconds or less. Because of this feature, DAT technology is particularly appealing for value-added system development requiring low-cost mass storage.

Both the 4-mm and the 8-mm units depend on a digital recording format; the QIC designs are analog devices. Digital recording is regarded as the more accurate and is required for voice and image representations.

Most camera stores already sell 8-mm tape, and DATs seem destined for widespread consumer distribution. If you purchase from uncertified sources for use in backup operations, be careful not to obtain poor-quality tape. If you plan to use a helical-scan device, you need the best tape available, because as bit densities increase, tape defects become magnified. Head clogs are another source of error and will occur more often in a tape containing surface variations.

Error Correction

Defects of the medium are a common source of error in tape-based recording, and there's a big difference in the way helical-scan and longitudinal recorders deal with the problem. By using the read-after-write verification process, both drives are capable of sensing bad blocks—those containing more errors

continued

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Development of a standard file format would facilitate software distribution on tape.

than can be corrected by the error-correction coding (ECC).

But the longitudinal designs simply rewrite the data farther down the tape, up to 16 times. This rewrite usually takes place on the same track, a process that may not circumvent the problem if the errors were caused by a longitudinal scratch. The design of the 8-mm drive causes it to rewrite bad blocks 11 blocks farther down the tape, a procedure that serves to position the data away from the same horizontal path. The device can rewrite a block up to 12 times. If, after 12 tries, its efforts are still unsuccessful, you should throw out the tape.

Helical-scan recorders possess better error-correction capabilities than just about any other mass storage device, partly because the higher bit densities mandate more sophisticated error-correction algorithms to account for dropouts, or flaws, in the recording area of the tape.

Helical-scan tracks are recorded at an angle of about 5 degrees to the edge of the tape in order to create a longer overall track length. In DAT, the incoming signal is split between two adjacent tracks, referred to as a *frame*; for error-correction purposes, frames are arranged into groups. The 8-mm drive, however, doesn't use the frame or the group concept. Instead, it writes data as a set of continuous blocks, and detects and corrects all errors within the data block structure.

One factor further compounding errors is that with helical-scan techniques, the spinning head can create helical scratches (on top of the longitudinal scratches already caused by the tape guides regardless of head design). With helical technology, tape defects are magnified over those found with longitudinal recorders with lower surface or overall recording densities.

Tracking, however, is generally more precise with helical-scan devices, which incorporate an additional head for reading a servo (positional reference) track. It is not yet necessary for most quarter-inch designs to include these capabilities in the drive design; however, future capacity increases will create the need. Since its inception, many improvements have been made to the data cartridge medium that address earlier problems that users encountered with these longitudinal recorders.

An 8-mm format track contains a servo zone (positional reference bits) and eight data blocks, each capable of storing 1024 bytes. The drive's read-after-write design can handle burst errors of up to 246 bytes within each block, and up to 80 additional single-byte errors—an extremely high level of ECC that results in a nonrecoverable error rate of less than one in 10^{-13} bits read.

Products based on 4-mm DAT technology achieve an even higher level of data integrity using various correction techniques in addition to read-after-write. The first two levels of ECC, called C1 and C2, are based on industry-standard Reed-Solomon algorithms. They are a holdover from the audio format. C1 and C2 are designed to handle horizontal error patterns up to 0.3 mm wide.

Data-storage formats include a third algorithm, called C3, for correcting diagonal errors affecting any two frames within the same group. Finally, *n*-group writing (i.e., rewriting the same block *n* times) can be used to further enhance data reliability, but the trade-off is a decrease in tape capacity. DAT products achieve an uncorrectable error rate of 1 in 10^{-15} bits read.

Products based on the DAT technology also incorporate a scheme known as *alternate azimuth recording*, which maximizes capacity by allowing the overlapping of adjacent tracks. The magnetic cores are mounted in the drum at different angles: The first head is aligned at +20 degrees to horizontal center, the second at −20 degrees. This design permits *interleaving*, a technique in which incoming data is divided between two tracks so that no major sections of the signal are lost. Alternate azimuth recording also minimizes crosstalk.

Benefits of a New Technology

Increasingly, new personal computers are being marketed with tape drives designed into their peripheral storage systems. Manufacturers developing 4-mm products may decide to adhere to a standard low-end file-interchange format. The result will be that, besides being able to use tape devices as backup storage, you will be able to use them to share large data sets among fellow users without regard to the drive's manufacturer.

Vendors of 4-mm products are in the process of addressing this key data-cartridge problem involving file-recording formats. QIC developers have long recognized this deficiency, but they have only recently taken significant corrective actions—possibly due to the pressure from DAT.

Development of a standard file format would also facilitate software distribution on tape, a process that heretofore has been limited to floppy disks. Once again, helical-scan technology may have a leg up on existing longitudinal machines.

Because these products use tape formulations with the ability to hold a stronger magnetic signal, software vendors may soon be able to implement a replicating process referred to as *contact printing*—the process of transferring a signal through the contact of a master tape against a clone tape. By using contact printing for updates rather than sending multiple disks, vendors could achieve significant savings and, hopefully, pass them along to users.

A new technology often adds some more desirable product attributes missing from current systems. On some of the DAT format designs, you will find a feature known as "update-in-place." With this provision, you can insert new information on a tape as long as the storage requirements for the new data do not exceed the requirements for the data being replaced.

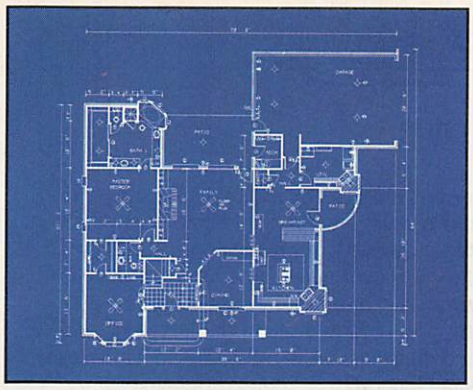
DAT formats also provide an area on the tape called the *system log*. Information stored in the log, including C3 error activity, is used to indicate the level of data integrity found within the volume. If the log contains a high level of C3 activity, then the tape is bad.

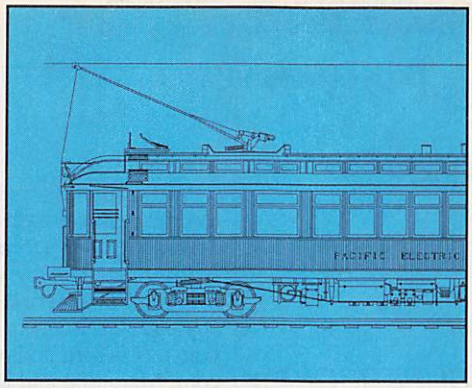
Market Realities

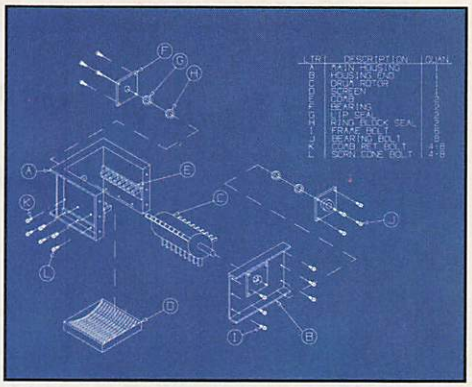
With earlier, longitudinal recording devices, the mechanical parts accounted for most of a tape subsystem's cost. The use of rotary heads in helical-scan technology shifts much of the cost to the electronic components. Thus, electronic sophistication and tolerances are substituted for mechanical sophistication and tolerances.

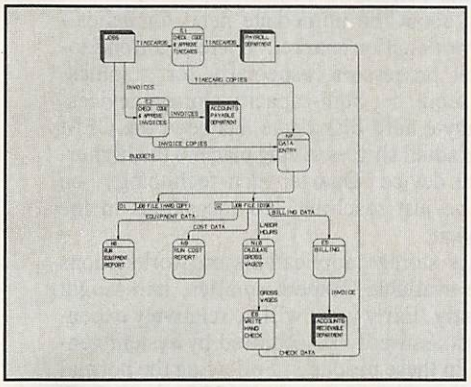
To obtain capacities and transfer rates similar to those of helical recorders, companies that make longitudinal recorders will need to develop new heads, stronger motors, and so forth. But these improvements will add cost to an already costly device. Therefore, if capacities and transfer rates remain about equal, there will be a growing disparity between the costs associated with these formats.

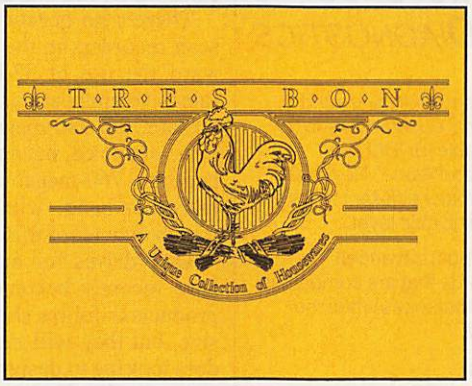
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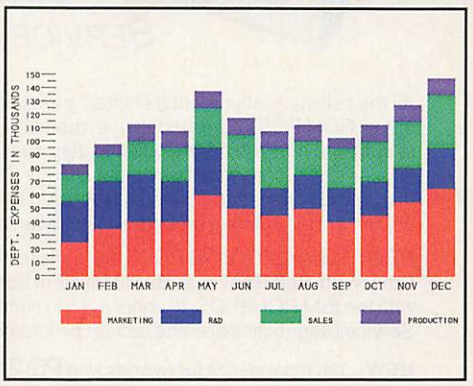


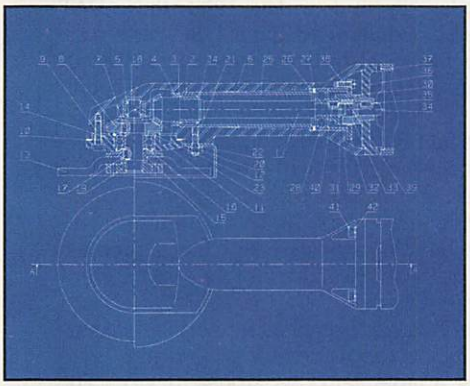


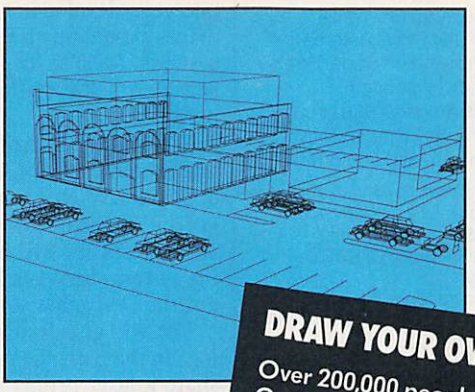


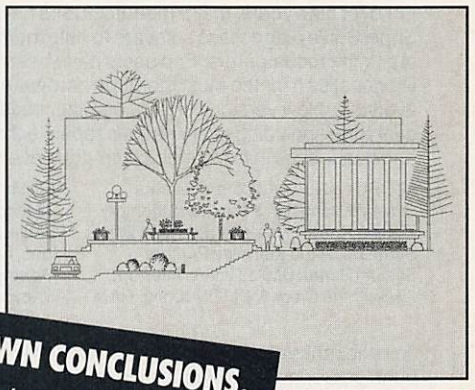


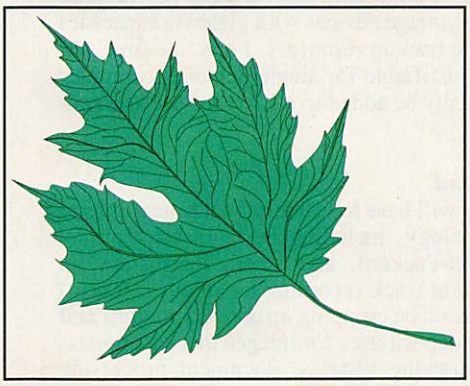






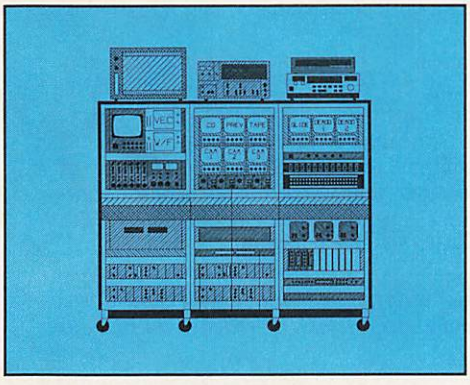


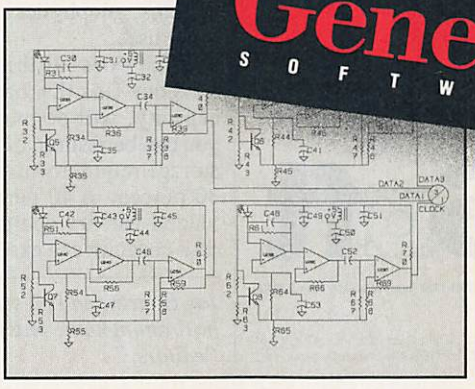














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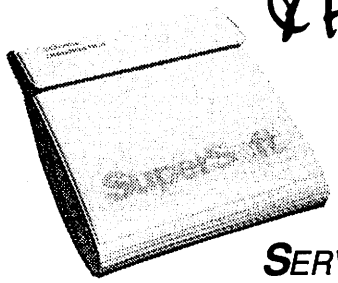
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VHS and 8-mm recorders are already available, but they are too large and too expensive to use for personal computers. VHS drives have won acceptance, but only for niche applications on a few minicomputers and workstations. The 8-mm product is slowly gaining acceptance within this same general group. Exabyte claims to have shipped 15,000 units in the last year, and that was before it signed contracts with NCR, Northern Telecom, Motorola, and Data General.

There's no question about the immediate need for helical-scan recorders in the workstation market. There is a trend toward the use of 32-bit processors, especially for graphics-intensive applications requiring high-capacity storage devices. Of late, the 380-megabyte hard disk drive has been the OEM drive of choice, but a gradual shift is taking place to the higher-capacity 760-megabyte device. Quarter-inch technology, on the other hand, will be just reaching 320 megabytes in the fourth quarter of this year.

DAT drives for mass storage applications on workstations have recently become available. Expect smaller, half-height products to follow shortly. Early units will be relatively expensive, but they will most assuredly be acquired by system vendors looking to design-in these products. Following the normal one-year development lag, by mid- to late 1990, these DAT drives should be offered as standard equipment on workstation systems. In 1992, expect to see affordable, commercially available 3½-inch-form-factor recording devices for personal computers.

While the 8-mm product is positioned to increase its performance and capacity, the 4-mm drive will continue to shrink in both size and cost, making it a viable personal computer product within the next two to three years. In the meantime, value-added resellers will be building attractive new image processing systems based on Intel's 80386 and Motorola's 68030 chips and the DAT mass storage device.

You will also find DAT on LANs created for peripheral sharing. In the past, the principal motivation for networking was to share a laser printer or a large hard disk storage device. The implementation of tape storage devices with gigabyte capacities adds the ability to share backup resources. For some time yet, DAT may not be cost-justifiable for single personal computer systems, but it could easily be added to a LAN for use as a centralized backup device.

Down the Helical Road

Although you probably will have to wait until early next year to use helical-scan technology, including DAT, investments by Sony, Hitachi, Hewlett-Packard, and others foreshadow an eventual shift to the slant-track recording technique. Helical-scan recorders should soon be cropping up on workstations and personal computers as depositories for images in such applications as CAD/CAM drawing systems, document processing systems, geophysical data-collection systems, and a myriad of other uses.

What does all this mean to you? For one thing, you may someday find that backing up your hard disk, regardless of its capacity, will be much easier. With helical-scan technology, you can be assured of a 1-to-1 disk-to-tape capacity ratio even if storage requirements continue to increase at the current rate of 30 percent to 40 percent per year. The trend is toward unattended backup operations, even on personal computers with disk capacities in excess of 150 megabytes. ■

Jay Bretzmann is a senior analyst for International Data Corp. in Framingham, Massachusetts. He can be reached on BIX c/o "editors."

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PAPER, MAGNETS, AND LIGHT

The long history of data storage devices is intertwined with the more recent, meteoric rise of personal computers

Robert R. Gaskin

Storage devices used with today's desktop and laptop personal computers are derived from a long history of large and often cumbersome devices. Many storage technologies of the past predominated for a time and then faded from the scene.

The earliest storage device for controlling machines was the punched paper card. It was used as early as 1804 for controlling silk-weaving looms. The first computer-like application was in machines that tabulated the 1890 U.S. census. The inventor of that tabulation machinery was Herman Hollerith, and the media has been called Hollerith cards ever since (see photo 1). The "modern" form of the card was introduced by IBM in 1928 and remained a mainstay of the computer industry through the 1960s.

On the Way There

When computers were in their infancy, many types of esoteric volatile memory appeared on the scene as precursors to the nonvolatile mass storage devices that we know today. The Williams Tube (1948), used on some of the earliest IBM mainframes, was a CRT similar to that found in today's personal computer monitors. Instead of being used as a display, however, it was used as memory. The Williams Tube was not very reliable and was soon abandoned for other schemes.

In 1949, mercury delay lines were used as volatile memory in the EDSAC (for Electronic Delay Storage Automatic Calculator) computer. In 1953, ferrite core memory appeared in the MIT Whirlwind computer (see photo 2) and the IBM 704. Core memory used tiny doughnut-shaped pieces of ferrite to store a single bit. When wired together in what is known as a *coincident current array*, core memory provides completely random access to any bit location without going through any other bit locations to get there. In addition, core memory is nonvolatile and retains data indefinitely when the power goes off.

The original cores were 80 mils in outside diameter; the diameter was reduced to 14 mils by the late 1970s. Although no longer used in commercial computers, core memory is still used in some military applications. Core memory was expensive and slower than the semiconductor RAM memory that replaced it. The closest that core memory got to being used for everyday applications was its use as the song-selection memory in the early Seeburg jukeboxes.

Drum and Bubble Memory

Off-line storage in the form of drum memory appeared in 1951. Drum memory was made up of magnetically coated rotating cylinders with multiple read/write heads (see photo 3). The IBM version had 58 tracks, with 100 characters per track. Fifty tracks were used for storage, and eight were used as an I/O buffer to the card machine or printer. The drums were fast but couldn't be stacked like disk platters, and they faded away in the 1960s.

Bubble memory caused quite a stir in the early 1970s because it was all solid-state, yet nonvolatile. In the presence of a bias field, the bubbles formed cylindrical magnetic domains in a thin film of magnetic material on a garnet-based substrate. Bubble memory faded away in the 1980s, largely because of long design times and cost. One product that still uses this technology, produced by Magnesys, is a floppy disk drive emulator for personal computers used in rugged environments. A 720K-byte version of it for the IBM 7552 Gearbox industrial computer costs $2000.

On to Tape

Of all the magnetic storage devices, tape drives have been around longest. They first appeared as half-inch reel-to-reel audio recording devices in 1934. The first model was made by the German company AEG using tape media made by BASF. By 1945, IBM had developed digital reel-to-reel versions.

The Univac Uniservo reel-to-reel drive, which used 1200 feet of metal tape, was introduced in 1951 (see photo 4). This

continued

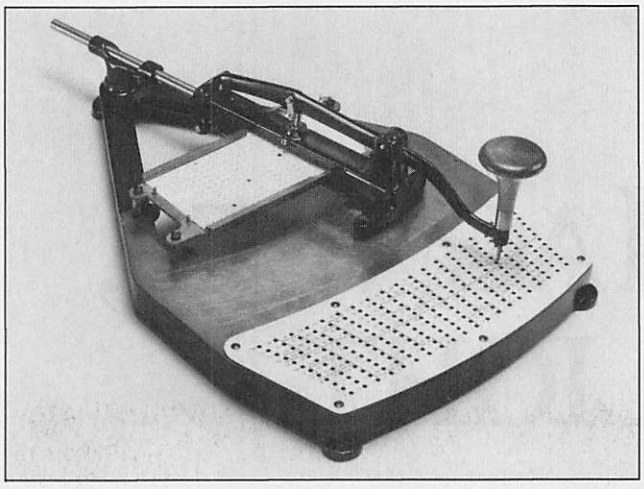


Photo 1: *A Hollerith machine with card. First used in the nineteenth century for controlling silk-weaving looms and tabulating the U.S. census, Hollerith cards were punched on a machine like the one shown.*
(Photo courtesy of The Computer Museum, Boston)

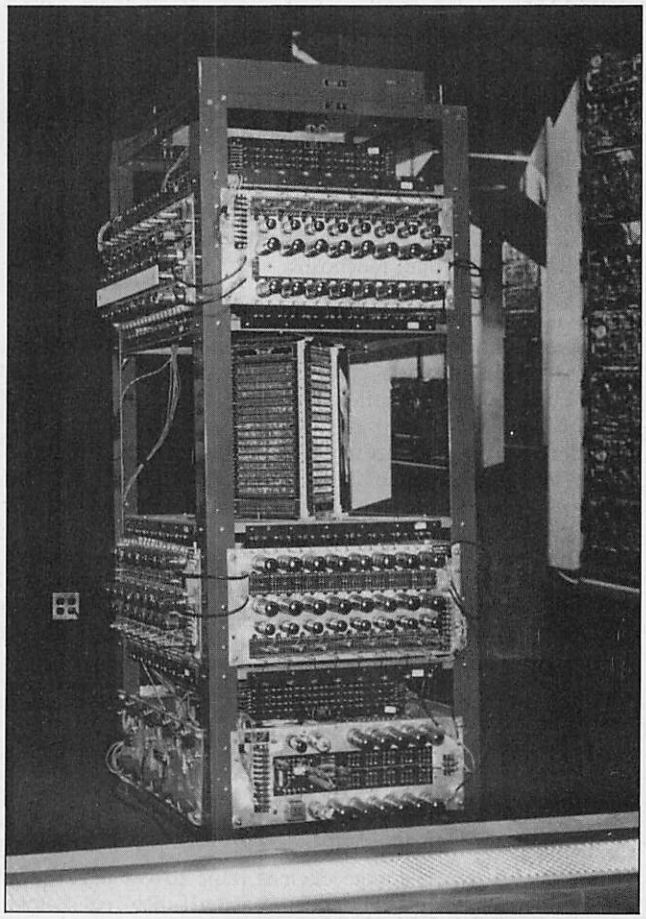


Photo 2: *Core memory was used in the Whirlwind project, a wind-tunnel experiment carried out at MIT. In this 1953 photo, you can see the Whirlwind Core Stack, providing 16K bytes of core memory.*
(Photo courtesy of The Computer Museum, Boston)

was followed in 1952 by IBM's 701, which used plastic-backed tape. IBM followed with several more models through 1971 that pioneered first the NRZI format, then phase encoding, and, finally, group coding. It remained for 3M to introduce the quarter-inch drive and cartridge media in 1971, which made desktop use of tape drives a practical reality. However, the first major use of quarter-inch tape drives did not come about on computers; in 1975, Western Electric endorsed their use by selecting them to handle the storage needs of PBX systems. Quarter-inch drives have since been made smaller, cheaper, and with larger capacities, to the point that 320-megabyte versions are expected to ship this year. The capacity of the drives in 1971 was only 30 megabytes.

In 1985, Irwin Magnetics introduced a low-cost drive based on the ⅛-inch DC1000 cartridge that utilized a floppy disk drive interface. The combination of these features in a tape drive proved to be extremely popular.

Ampex developed rotary-head tape drive technology for the broadcast industry in 1956 and added the Terabit model for computer applications in 1972. These were the forerunners of the tiny digital-audio-tape recorders that use 4-millimeter tape and are about to enter the personal computer market today (see the article "A New Twist on an Old Technology" on page 380). The DAT format will store over 1 gigabyte of data on a cartridge about the size of an audio cartridge. Helical-scan tape drive technology for personal computers has been most successfully pursued by Exabyte Corp., which makes a helical-scan tape drive that uses a $10, 8-mm video cassette–based cartridge that stores about 2.5 gigabytes. The drive price is in the $3000 range, so it is more suited for high-end business applications than for the average user.

Floppy and Hard Disk Drives

IBM invented the floppy disk drive as an 8-inch-diameter read-only single-sided device in 1971. The model 23FD was used as a program load device. It was followed in 1973 by the 33FD (code-named Igar), a read/write 8-inch drive with an unformatted capacity of 400K bytes double-sided (formatting consumes about 28 percent to 30 percent of the usable capacity). The 33FD was used as a replacement for punched cards on the 3740 data-entry system. Shugart Associates announced the SA901, an OEM version of the 33FD, that same year. Shugart's modest pricing set the stage for the use of floppy disk drives in personal computers. In 1975, Shugart announced a double-density version of its drive that could store up to 800K bytes (unformatted) and leapfrogged IBM's efforts.

The first IBM hard disk drive was the RAMAC 350, introduced in 1956. It stored 4.4 megabytes on 50 24-inch platters—a capacity chosen because it equaled 50,000 punched cards. IBM produced the first 14-inch drive (the 1311) in 1963, and the first removable-pack drive (the 2314) in 1966. In 1975, the only hard disk drives available were 14-inch-diameter devices that were totally unsuited for personal computers. Therefore, the early personal computers used floppy disk drives, not hard disk drives, for storage.

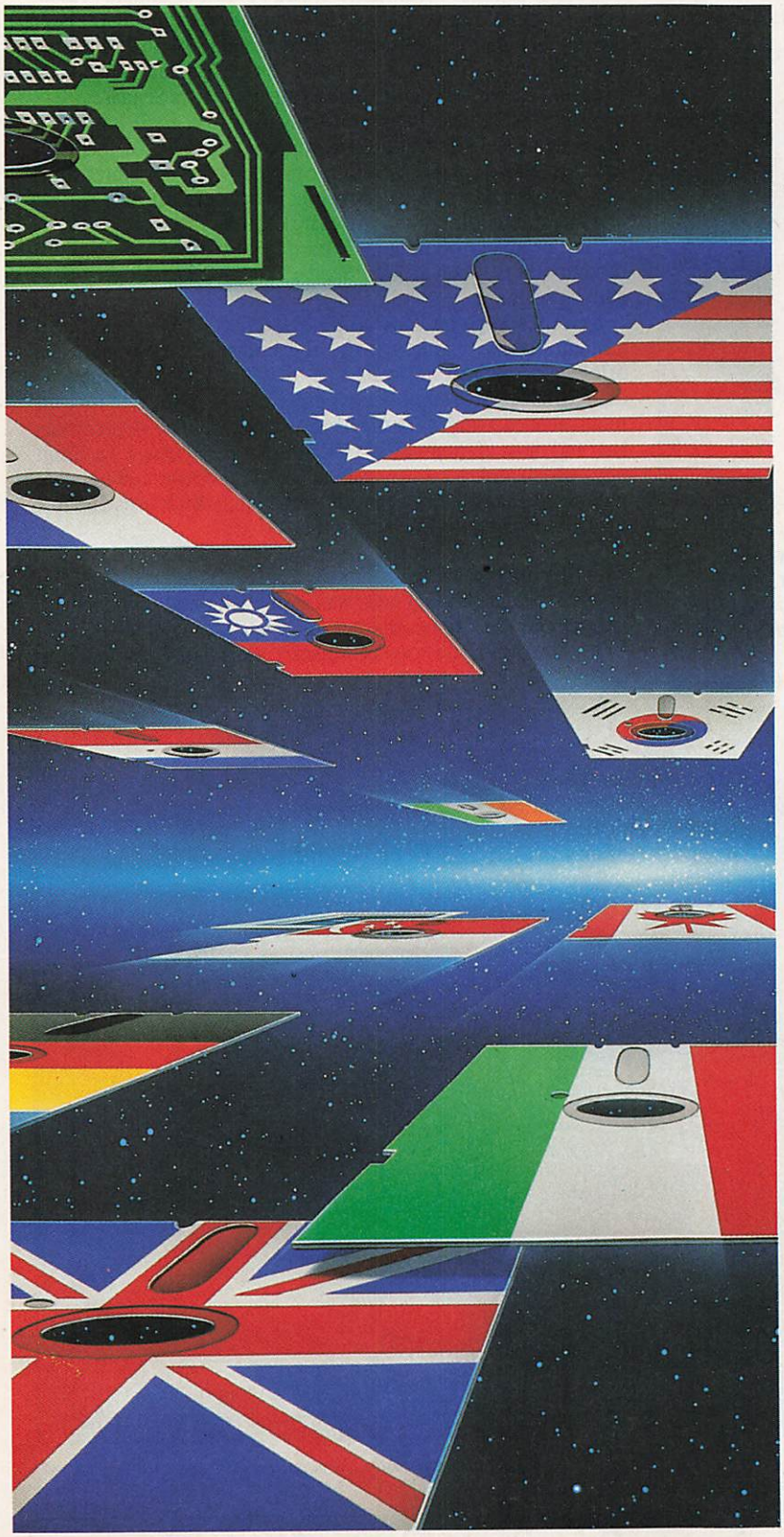
Then There Were PCs

The first microprocessors, such as the Intel 8008 and 8808, became available in 1975. Their advent marked the beginning of the personal computer era. These pivotal inventions made the downsizing of computers and their storage devices possible.

The peripheral storage devices available in 1975 did not fit personal computer needs very well. The 3M quarter-inch

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cartridge drive was a step in the right direction, but it was still too large and expensive. Thus, early microcomputer users converted many audio tape cartridge drives into "home brew" storage systems.

Hard disk drives were unsuitable in both size and cost to be used on personal computers from 1975 until 1980. The 8-inch drives announced in 1979 by both IBM and International Memories were of no help. During these five years, the floppy disk was king.

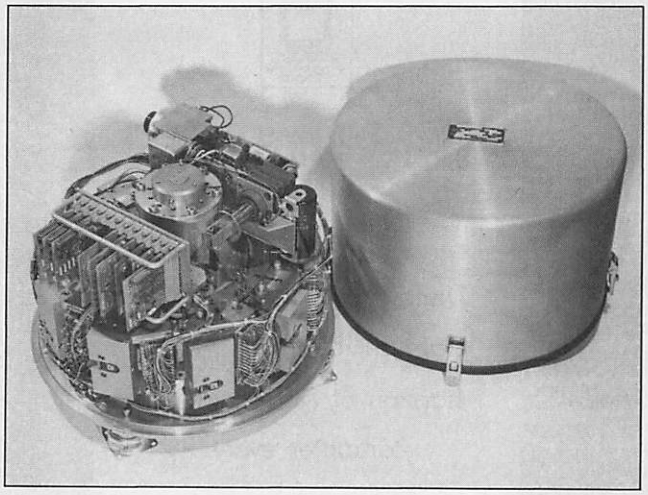


Photo 3: *Drum-memory off-line storage came into use in 1951. Drums were magnetically coated rotating cylinders with multiple read/write heads. They were fast but couldn't be stacked like disk platters, and they faded away in the late 1960s. (Photo courtesy of Vermont Research, North Springfield, Vermont)*

But Al Shugart and Finis Conner had learned a crucial lesson about product form factor while operating Shugart Associates (before Xerox bought the company). Al Shugart later formed yet another company called Shugart, with Finis Conner as part of the team. Xerox soon persuaded Shugart to change the company name, and it was reborn as Seagate.

Seagate's product was a 10-megabyte 5¼-inch hard disk drive that used trailing-edge technology to make it inexpensive and easy to manufacture for the personal computer market. The product was an overnight success in all distribution channels, including retail aftermarket sales. Seagate has been the top producer of affordable hard disk drives ever since, although others, such as MiniScribe, are now challenging Seagate's position.

Several companies, including Maxtor, Micropolis, and Priam, entered the business on the high end of capacity and price, offering drives that now range up to 760 megabytes in the 5¼-inch form factor. A number of companies were formed to offer removable cartridges for the hard disk personal computer market, and most of them failed. Exceptions are SyQuest Technology, which makes a 44-megabyte cartridge drive, and Iomega, with its 44-megabyte Bernoulli cartridge, which uses flexible media but performs like a hard disk drive.

The Shrinking Disk

In 1975, Shugart Associates was well positioned in the new 8-inch floppy disk drive market and had little competition. In 1976, Jim Adkisson, one of Shugart Associates' engineering

continued

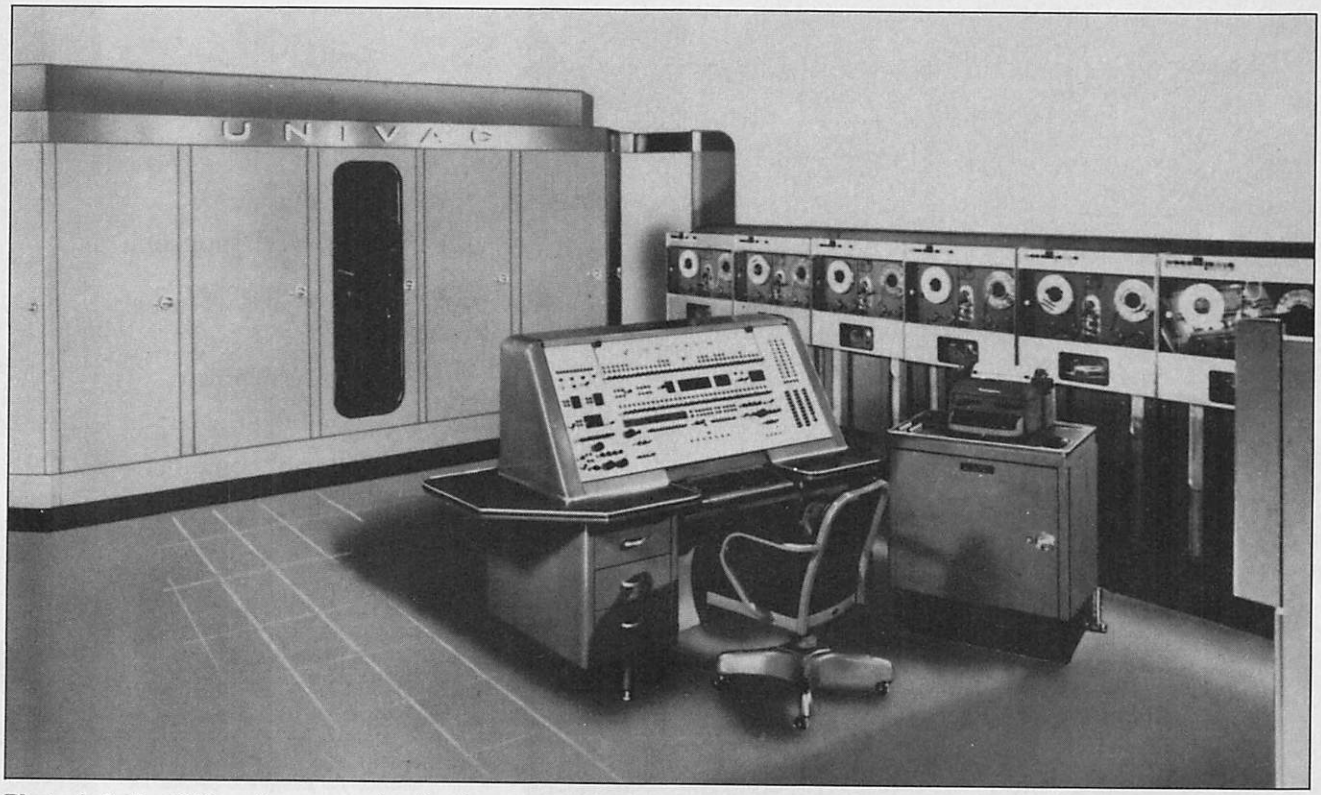


Photo 4: *In the 1950s, when companies first began using the Remington Rand Univac computer, several megabytes of mass tape storage filled entire rooms. (Photo courtesy of The Computer Museum, Boston)*

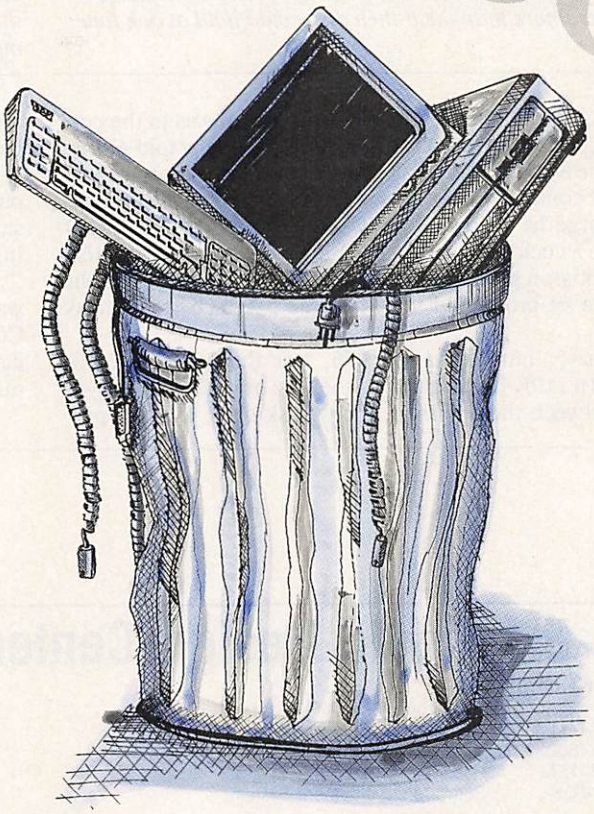
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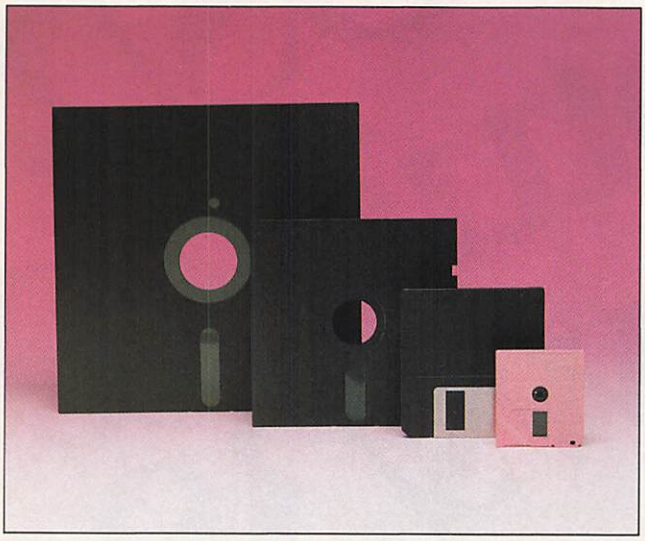


Photo 5: *Shown are 8-, 5¼-, 3½-, and 2-inch floppy disks for use with personal computers. At first, as floppy disks decreased in size, so did their capacities. Now they've gone in the opposite direction. The 2-inch floppy disk shown stores 720K bytes, more than the 8-inch disk could hold at one time.*



Photo 6: *Optical disks are known for their extremely large capacities. Shown here are a WORM (write once, read many times) disk, a CD-ROM, and a magneto-optical erasable NeXT cartridge. You can store almost a gigabyte of information on the WORM disk, 550 megabytes on the CD-ROM, and 256 megabytes per side on the NeXT disk.*

managers, was approached by a customer who was in the personal computer business. Over lunch, the customer told Adkisson that the 8-inch floppy disk drive was far too large to go into a personal computer (see photo 5). Adkisson asked the customer how large he thought the disk should be. The customer pointed to a cocktail napkin on the table and said, "About that size." Adkisson picked up the napkin and took it back to the lab, where he proceeded to design the 5¼-inch floppy disk drive.

That drive, introduced in 1976, was the Model SA400, which had a 110K-byte capacity—the first of its kind. The synergism between the 5¼-inch floppy disk drive and the personal computer was so great that ultimately, at its peak, Shugart Associates was shipping about 4000 drives per day, most of them 5¼-inch units. The 5¼-inch production was farmed out to Matsushita in Japan (a move that ultimately led to Matsushita's becoming the largest floppy disk drive manufacturer in the world).

But it was Alps Electric of Japan that blew Shugart out of the water at one of Shugart's biggest 5¼-inch accounts: Apple Computer. The loss of this contract is what started Shugart's demise in the floppy disk industry. By 1979, another manufacturer—Tandon—had become a major competitor for the 5¼-

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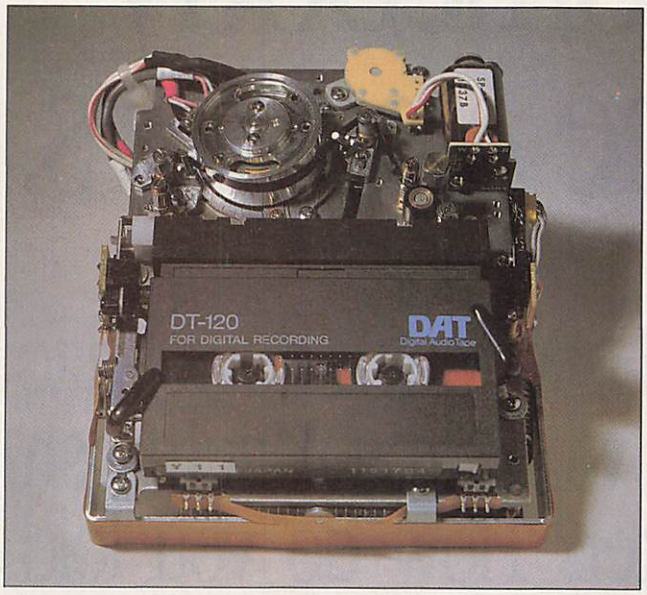


Photo 7: *A digital-audio-tape mechanism, showing tape wrapped around 90 degrees of the drum's circumference. This 90-degree wrap angle improves reliability and enables fast repositioning. (Photo courtesy of Hewlett-Packard)*

inch disk drive business, but it rapidly lost market share to the Japanese and soon after changed its emphasis from peripherals to personal computers. In 1982, various Japanese companies announced half-height versions of the 5¼-inch floppy disk drive, and U.S. production decreased almost to the vanishing point.

During 1981, Sony had introduced a 3½-inch floppy disk drive that could store 438K bytes with a 600-rpm spindle speed. Sony submitted it to ANSI for approval as a new standard. Sony's arguments were that the smaller disk, with its hard case and its shutter over the head access area, was much better protected than the 5¼-inch disk, and that this new product would fit into a shirt pocket. The ANSI committee ultimately accepted the product as standard, but in a revised form. The capacity was increased to 1 megabyte (720K bytes formatted), and the spindle speed was reduced to 300 rpm—but it still would fit into a shirt pocket. Thus, the garment industry unwittingly contributed to floppy disk standards.

During 1982, several manufacturers challenged Sony's 3½-inch form factor. Hitachi proposed a 3-inch floppy disk with a 250K-byte capacity (later raised to 1 megabyte) in a similar hard cartridge. Tabor Corp. (with Dysan backing) proposed a 3½-inch miniature version of the 5¼-inch floppy disk. IBM proposed a 4-inch "demi-diskette," one-half the diameter of the company's original floppy disk, but its drive had deficiencies, a very poor system interface, and an ultraslow access time.

All three companies lost out—Hitachi because it lacked the lobbying power of Sony and had no U.S. computer manufacturers as champions; Tabor because its product, with its flexible jacket and wide-open head-access slot, was just as vulnerable to damage as the original 5¼-inch product; and IBM because of the inadequacies of its drive and because it had an unprotected disk.

Early acceptance of the 3½-inch format by Apple and Hewlett-Packard got it off to a good start, and its use in the IBM PS/2s in 1987 put it over the top. The shipments of 3½-inch floppy disk drives now exceed those of 5¼-inch floppy drives worldwide. Zenith has recently introduced a 2-inch, hard-shell "mini-disk" for its MinisPort portable computer (see "The Ever-Shrinking, Ever-Expanding Laptops," August BYTE). The 2-inch drive stores 720K bytes.

Let There Be Laser Light

The idea of optical storage has been around a long time. In 1927, John L. Baird demonstrated a "Phonovision System" based on a waxed disk with information displayed by an optical scanner. During 1935, Baird Radiovision offered for sale, through a London department store, 6 minutes of video display pictures from the stored images. In 1961, 3M started work on optical recording and, by 1965, was granted several patents.

In July 1971, the *Bell System Technical Journal* published a paper by D. Maydon entitled "Micromachining and Image Forming on Thin Film by Laser Beams." It was a harbinger of things to come. In 1974, Philips demonstrated a laser recording and playback system. The company followed this with a 1979 demonstration of the CD audio disk system, which has since made the phonograph record obsolete.

The first optical drives for computer use began shipping in 1983. These were 12-inch WORM (write once, read many times) products that are still priced out of the range of the personal computer market. Somewhat more affordable 5¼-inch WORM products began shipping in 1985 (see photo 6).

The audio CD formed the basis of the computer CD-ROM, which started shipping in 1985 and has slowly developed into a new form of publishing via storing information, such as encyclopedias, on optical disks. At first, CD-ROM drives were expensive, and disks were few. But this situation is rapidly changing. New titles, such as Microsoft's Office, are now appearing. This program is designed to provide on CD-ROM all the software applications that are needed by the typical small business using a Macintosh environment. NEC and Amdek are now offering CD-ROM drives for $600. The NEC unit is portable and plays CD audio disks, as well as reading CD-ROM disks.

In 1988, Sony, Canon, Ricoh, and Maxoptix introduced 5¼-inch rewritable optical products. Like the early WORM drives, these are expensive and, for the time being, will appeal only to the high-end workstation portion of the personal computer market.

Tomorrow's Mass Storage

During the next five years, you can expect to see the following improvements to personal computer storage products.

Tape drives. Quarter-inch cartridge drives will have more than 1 gigabyte of storage. Eastman Kodak has already demonstrated such drives, as has 3M. DAT drives (see photo 7) will provide over 1 gigabyte on a 4-mm tape cartridge, about the size of a credit card but thicker.

Hard disk drives. 5¼-inch drives will store up to 1.6 gigabytes. High-end 3½-inch drives will be storing 600 megabytes in full-height versions. Notebook-size computers will commonly use 2½-inch hard disk drives that are three-eighths of an inch high and store 50 megabytes.

Floppy disk drives. The "floptical" drive from Insite Peripherals will store 20 megabytes on a 3½-inch floppy disk, using a combination of optical and magnetic storage techniques (see photo 8). Insite's president is the same Jim Adkisson who invented the 5¼-inch floppy disk. The Brier Technology magnetic drive will store 20 megabytes and holds promise of storing as much as 50 megabytes on a single 3½-inch disk. A whole stable of floppy magnetic drives will be available from

Japan in the near future, offering storage capacities of from 4 to 27 megabytes per disk.

The catch in all of this is that none of the present or foreseeable future offerings are compatible with the present interchange standards. This incompatibility will rule out one of the main functions of floppy disks: software distribution. It could eventually lead to software distribution on CD-ROM, which already has an interchange standard.

The 2-inch floppy disk drive, already seen on the Zenith MinisPort and DynaBook notebook-size computers, will prevail among these machines—and possibly among the coming pocket-size computers. The pocket-size machine may be the one that provides the demand for IC memory cards for loading programs.

Optical disk drives. The write-once drive will continue to exist for high-end applications that benefit from a permanent audit trail. Capacity will stabilize at around 1 gigabyte for the 5¼-inch WORM product.

The prices of CD-ROM drives will drop to the $300 range during the next five years, and many personal computer vendors will offer them as options—if not as standard equipment. Write-once CDs (essentially, another type of WORM) will be more widely available than they are now, and rewritable versions will finally appear within five years.

The capacity of 5¼-inch rewritable drives—just beginning to arrive in forms such as the hard disk shell in the NeXT computer—will be mostly 650 megabytes, the present International Standards Organization standard, because most suppliers are adhering to it. Manufacturers will also offer proprietary formats ranging from 1 to 2 gigabytes for users who do not care about data interchange.

A new class of rewritable optical 3½-inch drives will soon appear and will drop in price to less than $1000. At this price level, such drives make sense for personal computer users who could benefit from having a removable disk drive in addition to a magnetic hard disk drive. Capacity will be as high as 280 megabytes on the removable disk.

Laser cards. After years of selling licenses to the technology but not producing drives, the Drexler LaserCard may be getting close to real-world use in the field of medical record keeping for clinics and medical insurance companies. The LaserCard stores up to 2 megabytes of data on a credit card–size card containing an optically written strip (see photo 9). Under development are optical drives and compatible "laser cards" that can store around 40 megabytes.

Digital paper. A write-once Bernoulli Box from Iomega will become available. This 5¼-inch drive will use flexible optical write-once media called digital paper (see photo 10) from Imperial Chemical Industries in a cartridge that stores 1.2 gigabytes (see "Digital Paper," February BYTE). The cartridge's target price is about $50. The drive price has not been announced, but it should be affordable for the personal computer business user.

Solid-state disk drives. The products available in the current market tend to cost around $1000 per megabyte—sometimes even higher. They have value in speeding up systems that otherwise would need to be replaced, but the systems that use them are normally in the minicomputer category. Development efforts are under way to bring them down in cost and to make them suitable for the personal computer environment. ■

Robert R. Gaskin is a senior industry analyst at Dataquest, Inc., in San Jose, California. He specializes in and writes about the computer storage industry. He can be reached on BIX c/o "editors."

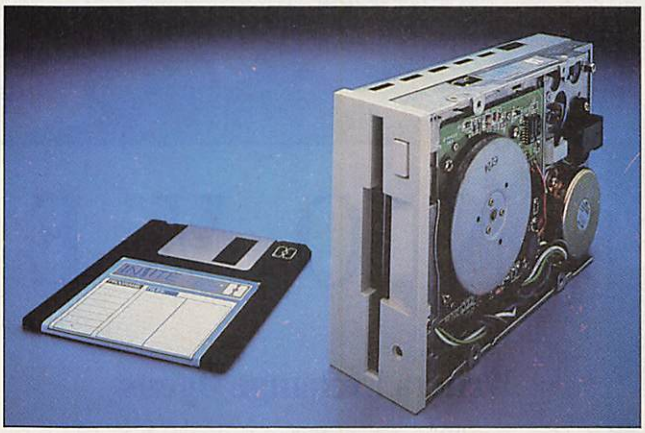


Photo 8: *A "floptical" disk is a 3½-inch floppy disk that uses optical and magnetic recording technologies and can hold 20 to 25 megabytes.*



Photo 9: *Drexler's wallet-size LaserCard contains a 35-mm strip that can permanently store several megabytes of data. Its current use is storing medical and insurance data.*



Photo 10: *"Webs" of digital paper, a removable optical data storage medium, can either be split into lengths as tape or stamped into disks and inserted into cassettes.*

BIX CALENDAR NOVEMBER

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Writers Exchange Opens

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Most Writers Exchange conferences are open to the public, although journalism.pro and writers.pros are reserved for practicing professionals only. A special conference—sfwa—serves as a private forum for members of the Science Fiction Writers of America. Other conferences include: journalism, new.writers, poetry.prose, writers, write.fiction, and writers.talk.

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blue tuesdays—Join the IBM Exchange moderators for a cbix session every Tuesday night at 9 PM EST. (join main cbix, channel 1, band b)

games people play—Here's the Interactive Games Exchange schedule for November. Watch for specials, as well:

Sundays, 9 PM EST—Poetry, art, music and stories. (join fun.n.games/game.room)

Sundays, 9:30 PM EST—Learn about role-playing games on line and off line at Fantasy Foundation College. (join ff/ff.col)

Mondays, Thursdays, and Saturdays, 9 PM–Midnight EST—Meade & Mirth. (join mnm/inn)

Tuesdays, Wednesdays & Saturdays, 9:30 PM EST—Ledinworld. (join lworld/ledinworld)

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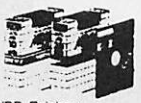
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THE ABCs OF DIGITAL TYPE

Digital type—like its ancestor, movable type—is revolutionizing the way we publish documents

John Collins

In the beginning was Gutenberg, setting pieces of lead into a press and so mechanizing the process of printing—formerly a laborious job done by hand, one document at a time. (See the text box "Gutenberg Had It Easy" on page 404.) The typesetting machine and the typewriter succeeded Gutenberg's press, and now the personal computer has largely replaced the typewriter.

At first, all personal computer displays and output devices emulated the look and feel of the typewriter. Characters were generated by specialized hardware that wrote a matrix of bits into a computer's video memory. Characters appeared on the screen made up of spots corresponding to these bits. Needless to say, the type of font you got was determined solely by the characteristics of the computer's character-display hardware.

Things really got interesting when you attempted to print the document, because the font used by the printer to print characters onto the page seldom matched the characters in your computer's video hardware. If you were really resourceful, you might be able to coax out of your printer condensed, expanded, bold, or underlined text. However, there was little chance that what you printed out would match what you saw on your computer's screen. WYSIWYG it wasn't.

The Macintosh changed this by merging the imaging operations of the computer screen and the printer. The Mac has no character-display hardware or character-based screen mode—it operates entirely in graphics mode. The System file stores a bit map of a typeface and the point size used. Characters are assembled from a "library" of bit maps—the actual pattern of dots that makes up the shape of each character. When you print a document, the printer operates in the graphics mode and draws the characters in much the same way they're drawn on the Mac's screen. This method has important consequences.

Text output is no longer coupled to display hardware; characters can be larger than the typical 9×7 matrix. Moreover, since stored bit maps are used to generate the characters, the type style can be anything—for example, Times Roman, Old English, Courier, Cyrillic, kanji, or Arabic.

When you use this process, whatever climbs out onto the printer tray closely matches what you have on the Mac's screen. Making bit maps appear on a screen or from a printer simply requires copying the data to the output device, so it is virtually instantaneous.

One trade-off with bit maps is that a different one is required for each type style and point size. Furthermore, additional bit maps may be required to handle the resolutions of different output devices. Another major disadvantage of bit maps is that they require enormous storage capacity, especially for large sizes.

Digital Type—Fonts Are Us

With the advent of digital type (i.e., typefaces represented as electronic data) came the potential of using a single typeface master on a wide variety of—perhaps all—output devices produced by different manufacturers. With this technique, you can easily produce output in just about any type style and size you choose on a variety of machines for a variety of applications.

Font portability makes it easier and more economical to create and distribute fonts for use in a variety of devices. It also provides users with a greater availability and wider variety of typefaces. Device-independent digital fonts significantly reduce compatibility problems. As more and more devices are networked together, this device independence becomes particularly important. Finally, portability preserves your investment in type when you upgrade to new devices.

Digital type can be provided in three forms: Bit maps, outlines, and stroke fonts. For situations where only a few faces and point sizes are needed, bit maps are ideal because of their simplicity and high performance. Bit maps can be hand-edited and customized to produce the best-possible type quality on various kinds of output devices (see figure 1).

Where typographic flexibility (e.g., several faces, several point sizes, and rotation) is required, outlines are the preferred form. An outline is a mathematical description of the shape of a

continued

Gutenberg Had It Easy

When Gutenberg introduced movable type 500 years ago, fonts were simple and portable. Hand-cast hot metal type from any one foundry could be easily mixed with that of another foundry. This flexibility gave users great freedom and variety in specifying fonts.

When typesetting became mechanized, about 100 years ago, things got more complicated. Each typesetter manufacturer required—and most designed and sold—a particular kind of type for its equipment. Users who changed from one manufacturer to another had to purchase another library of type for the new device.

With the emergence of phototypesetting 20 years ago, type became even more machine-specific. Phototypesetting machines created type by projecting light through negative images of letters onto photographic paper. The type required for these machines was unique to each model. Even if you wanted to upgrade within the same line of typesetters, you usually had to purchase a completely new library of fonts. While this situation was good business for typesetter manufacturers, it limited users in their choice of type to those styles and formats made for their particular device.

When phototypesetters became digital in the 1970s, type was often encrypted so it would work only within a single installation. This is analogous to compact disks that are specially encoded to be played on one particular CD player. Music lovers would never go for this when their records historically could be played on any phonograph.

What we've seen over the last 500 years is a series of major technical advances in the mechanization of typesetting. These advances, unfortunately, have gradually stripped type of its initial portability to the extent that it has become very specialized and localized. The irony here is that digital type has greater potential for portability on a number of different machines than any other form that type has taken during its evolution.

Because it has been so long since type was truly portable and device-independent, users have become accustomed to closed font architectures. We are, however, at a stage where technological advances in digital typography are beginning to provide the freedom of choice and open market that existed in the early days of movable type. More and more users are becoming aware of this. As a result, the demand for open and portable font architectures is growing rapidly.

character (see figure 2). As outlines can be scaled and rotated, only one outline is needed to represent a character in any size and for any device resolution. Thus, outlines are much more compact than bit maps, especially where many sizes are required. Their major disadvantage is that a significant amount of computation is required to convert them into the bit-map form eventually required by the output device. As a result, going from an outline to an image on the screen or printer is a relatively slow process. To do so at high speed takes a significant amount of processing power.

The third representation that is occasionally used is stroke fonts (see figure 3). Stroke fonts, sometimes called vector fonts, describe the spine of a character. Drawing a character from a stroke font onto the screen or into the printer memory can be as simple as drawing a series of pixels along the strokes that make up the character. For large point sizes, a thicker path of pixels needs to be drawn to prevent the character from looking stick-like. Like outline fonts, stroke fonts are size- and resolution-independent and can be rotated to any angle.

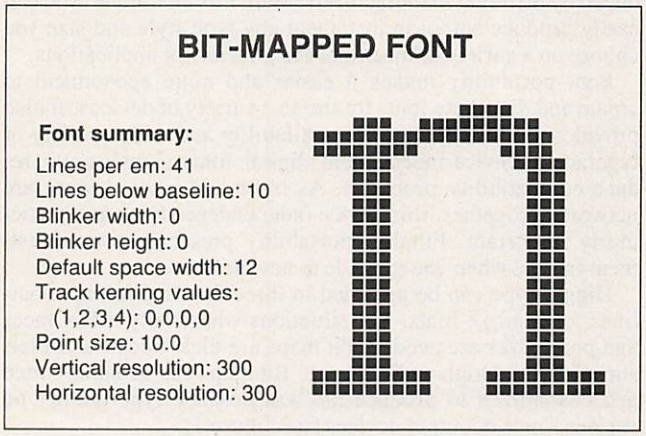


Figure 1: *Bit maps define the actual pattern of dots that composes a character. For optimal quality, bit maps can be hand-edited.*

Less computation is required to image a stroke font than is needed for outlines, so the results are faster. Stroke fonts also require a relatively small amount of storage—typically 50 percent less than outline fonts. The catch with stroke fonts is that only a tiny percentage of the world's typefaces can be effectively represented as stroke fonts. Only those faces with even stroke weights and simple round or square ends of strokes can be represented (e.g., Courier). Attempts to represent other faces will produce results that require more storage and take more time to draw than outline data.

There is more to digital fonts than just the shape of the characters. For an application program to lay out the characters on a page, it needs to know how much space each character takes up. The height of a character is determined simply by the point size that the user specifies. But the width of each character is not so straightforward. Most typefaces in general use are proportionally spaced; that is, each character has a different width. The program needs this information so it can decide how the characters fit side by side, how many characters fit in the line, and where the line should be broken. Character widths are unique to each font.

Merely describing the widths of each character does not ensure the highest-quality reproduction. Certain character pairs, such as "To" and "AV," look much better when the spacing between them is reduced; others look better when the spacing is increased. This technique is known as *kerning*. Most fonts contain kerning data that describes spacing adjustments to be applied to certain character pairs as they occur in the text.

Other data, such as scale factors for making small caps, superscripts, and subscripts, and instructions for building fractions, is sometimes provided with fonts. This data, along with character widths and kerning data, is called *font metrics*.

Another aspect of fonts concerns character sets—groups of letters, figures, symbols, and so on. If there were one universal character set, all fonts would provide the same collection of characters. Unfortunately, it's not that simple. There are character sets associated not only with different countries, but also with different printers (e.g., LaserWriter and LaserJet), operating systems (e.g., Macintosh and DOS), page-description languages (e.g., PostScript and QuickDraw), and application programs (e.g., WordPerfect and Lotus 1-2-3). A great number of character sets is in common use today. Hewlett-Packard's LaserJet, for example, supports more than 40 sets for its resident fonts.

But Are They Portable?

Even though bit-map output devices are the most common type of output device used today, the manner in which they work with fonts varies widely. Graphical displays can handle a wide range of typographic styles. It is the responsibility of the application program or the operating system to copy the bit-map character data from the font into the appropriate place in the display buffer. The font format required is therefore determined by the application program or the operating system.

Dot-matrix printers operating in graphics mode have capabilities similar to those of graphical displays. They depend on the application program or operating system to build a bit-map image of the page in memory. The resulting data is then output to the printer. As with graphical displays, the font format required for dot-matrix printers depends on the application program or operating system.

Laser printers, on the other hand, have the processing ability to use resident fonts or additional user-installed fonts. Laser printers accept instructions from the host computers by means of a page-description language. The two most common PDLs in use today are Hewlett-Packard's Printer Control Language and Adobe's PostScript. PCL devices use bit maps that are either resident or downloaded from the host. Additional fonts may be made available for PCL devices in the published PCL bit-map font format.

PostScript devices expect fonts in outline format. Because PostScript is a programming language, it is possible to encode fonts in various forms. Thus, you can use PostScript fonts from a variety of vendors with PostScript typesetters and laser printers. (See the text box "Open Fonts: A Break for Users?" on page 406.)

Managing Your Fonts

Although MS-DOS is a widely used operating system, it provides no font-management capabilities. That function is left to the application programs. As a result, MS-DOS software developers have chosen different approaches to handling fonts, font metrics, character sets, and other typographical data. Therefore, font formats and font-metric data required for one application program are likely to be different from those required for another.

Graphical user interfaces (GUIs) that are compatible with MS-DOS, such as Microsoft Windows and Digital Research's GEM, have brought some order to this chaos by managing fonts for displays and dot-matrix printers. Applications that take advantage of these facilities, therefore, use a common font format. Increasing acceptance of these operating environments has helped the IBM PC improve its ability to handle fonts. OS/2 and Presentation Manager promise to accelerate this trend as they become established in the PC environment.

In the Macintosh environment, fonts are managed within the operating system itself. Thus, there is standardization among Mac application programs that use fonts. From the perspective of the independent font vendor, this is a much simpler environment for which to provide fonts. Apple recently announced its System 7.0, which will bring dramatic increases in font capability with future Mac releases.

Unix was late in providing a GUI, let alone any kind of font management. Recent developments along this line, though, should create a trend toward standardization in the way fonts, character sets, and font-metric information are handled for application programs running under future extensions of Unix.

A Font Is Born

Fonts are conceived by type designers, who start with an idea for a typeface design, make sketches, and then do detailed

continued

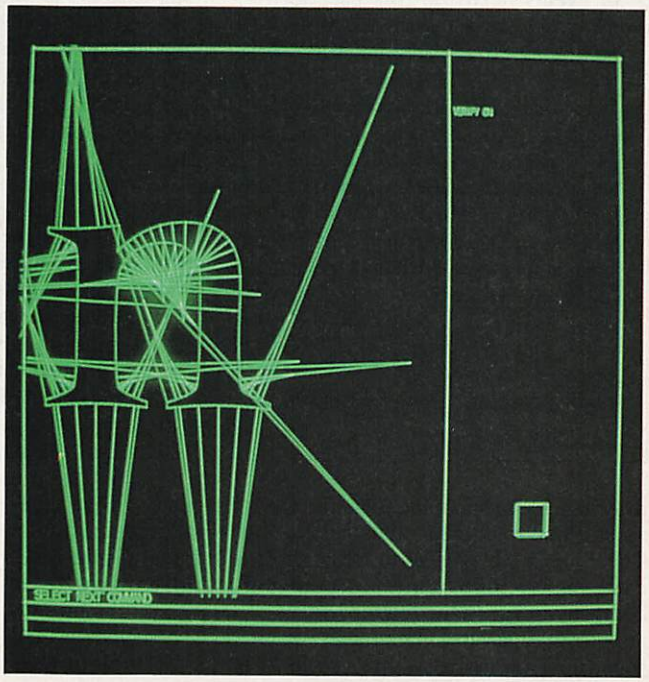


Figure 2: *An outline font, mathematically plotted as a series of lines and arcs. Outlines are scalable to a range of sizes and are resolution-independent.*

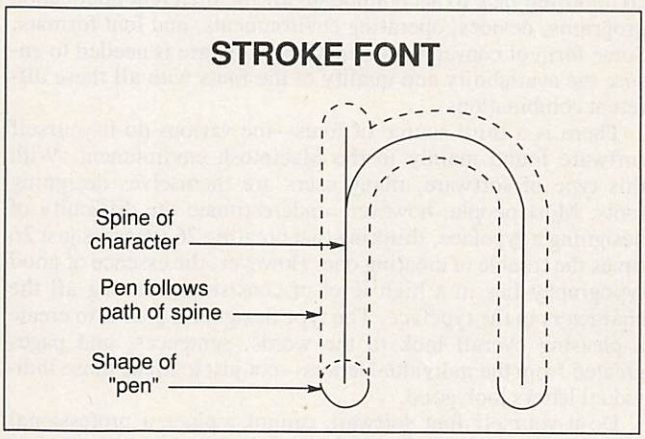


Figure 3: *A stroke font. Stroke fonts are defined by a pen of a certain width that follows the spine of a character.*

Open Fonts: A Break for Users?

Marlene Nesary

While Adobe's PostScript has been a boon to electronic publishing or to those who just want the flexibility of using a variety of fonts in their work, the atmosphere surrounding the use of its technology has been, shall we say, a bit close-ended. Until recently, users had to have a PostScript-licensed printer to read Adobe-encrypted fonts. A couple of events occurred this past spring, however, that changed things for the better—as far as users are concerned, that is.

In an apparent bid to wrest control of Adobe's proprietary technology, Sun Microsystems announced its own font-scaling system, called OpenFonts. According to a Sun spokesperson, the system is a "self-contained font-scaling module that lives independent of the imaging model." In other words, the product (developed by Folio, a company that Sun acquired last summer) is "software that automates the font-description and scaling process. It won't be an end-user program; you will license the technology like you would PostScript and put it into your printer software or your Windows driver." At this writing, however, OpenFonts isn't available and remains an unknown.

About the same time that Sun made its announcement, a Boulder, Colorado, company called Raster Image Processing Systems let loose another salvo at Adobe. RIPS stated that it had broken the encryption scheme used by Adobe's PostScript fonts. Both the character description and the so-called hints were decoded, said company president Lynn King.

What this means is that users can now "purchase Adobe fonts off the shelf and run them on clone printers," stated a RIPS representative. He added that "while others have cracked the PostScript code, we have made it possible for users to run Adobe fonts on less-expensive printer controllers." Until now, because only Adobe-licensed printer controllers could decipher the company's code, the only way you could use Adobe fonts was to run them on more-expensive PostScript-licensed printers.

But this activity hasn't put a damper on Adobe's marketing efforts. If anything, they've ramped up. This past spring, the company announced that it had increased the number of licensed PostScript printers and expanded its PostScript-compatible font library through licensing agreements with three major type foundries—agreements that may yield as many as 600 new typefaces by the end of 1989.

Adobe has also released its font-scaling technology as a separate product for displays. The subset of Display PostScript, a new software utility called Adobe Type Manager, is due to become available this fall to computer and system software OEMs and to Macintosh users, who should be able to purchase ATM directly from their usual retail channels.

drawings to flesh out the idea into the form of a complete typeface. Font foundries take these designs and digitize them. There are two classes of font foundries. First, there is the dedicated foundry that creates fonts only for machines made by the company in which the foundry exists. This is the common situation with typesetter manufacturers. Obviously, such dedicated foundries don't have to produce fonts in the different formats and character sets in use elsewhere.

In contrast, independent font foundries are not tied to a specific piece of hardware. They must make fonts that can work with any and all devices. Therefore, it becomes a much more complicated task to accommodate all the different application programs, devices, operating environments, and font formats. Some form of conversion or enabling software is needed to ensure the availability and quality of the fonts with all these different combinations.

There is a third source of fonts—the various do-it-yourself software found mainly in the Macintosh environment. With this type of software, many users are themselves designing fonts. Most people, however, underestimate the difficulty of designing a typeface, thinking that creating 26 letters is just 26 times the trouble of creating one. However, the essence of good typography lies in a high level of consistency among all the characters in the typeface. The type designer's goal is to create a pleasing overall look to the words, sentences, and pages created from the individual letters—not just to make those individual letters look good.

Do-it-yourself font software cannot replace a professional type designer's training and experience, just as music software cannot replace a musician's conservatory education and actual performance experience. Such programs, however, are useful for creating logos and other special characters that may be missing from generally available fonts or character sets.

The Font Store

Some printers and typesetters have fonts built right in. PostScript printers, for example, generally come equipped with 35 resident fonts. But many users want a much wider variety than can be accommodated by resident fonts, particularly now that desktop publishing is so popular and people are realizing how many thousands of typefaces exist. User-installed fonts offer a much wider variety of faces than can be provided as resident fonts. They are available from numerous vendors.

A number of such fonts are available that are device-specific. The best known are cartridge fonts for use in printers such as the LaserJet. While these are by far the easiest to use, they have major disadvantages. Cartridge fonts work with only one model of printer, offer limited styles and point sizes, and don't provide fonts for use with screen displays. Font-metric information must be built into the applications or printer drivers or supplied with the cartridge.

Somewhat more flexible device-specific fonts are soft fonts, which consist of a downloadable bit map sent to the printer by the application program or printer driver. Unfortunately, most prepackaged soft fonts are configured for one particular printer and offer a limited set of point sizes for each typeface.

A third kind of device-specific font is the PostScript font. While not quite as device-specific as the others—it works with a wide variety of PostScript printers and typesetters—it will not, of course, work on non-PostScript devices. User-installed PostScript fonts are generally provided in downloadable outline form, and, like soft fonts, they are sent by the driver or the

application program to the printer for rasterization.

There are two classes of PostScript fonts. One class, often called Type I fonts, makes use of Adobe's proprietary mechanisms built into the output device. The other class, called user-defined or Type III, makes use of only the published PostScript language. Type I fonts offer significant advantages over user-defined fonts in terms of data size, performance, and typographic quality.

Several soft-font vendors provide a software utility that can scale typeface outlines and convert them into bit maps for supported printers. Glyphix, from Swfte (Wilmington, DE), offers 16 typefaces that work with one of its utilities, called Font Manager. There are separate Font Managers for Microsoft Word 4.0, WordPerfect 5.0, PageMaker 3.0, and Ventura Publisher 2.0. Font Manager scales the outlines from 6 to 60 points for LaserJets and compatibles. The utility can also oblique (i.e., slant) and alter the weights (e.g., boldface) of the fonts. Glyphix fonts can also be used with Lotus Manuscript 2.0, WordStar 2000, and other applications.

A RAM-based printer controller will provide an upgrade path to new font-scaling technologies and PDLs as they become available.

Bitstream's Fontware Installation Kit is a menu-driven utility that scales typeface outlines from 2 to 144 points and rasterizes them into bit maps especially configured for the user's devices. For PostScript devices, the outlines are simply converted to the required PostScript format and can then be scaled to any point size. The program handles font management by building and updating directories for font files.

Fontware installation kits are available for most popular desktop publishing, word processing, graphics, and spreadsheet programs. (They are generally offered to users directly by the applications developer.) The library of 52 Bitstream typeface packages works with any of these kits. Hewlett-Packard and Compugraphic together offer a similar utility called Type Director that works with their typeface packages.

Some vendors offer editing programs that let users customize fonts. With these programs, you can create logos, special characters, and additional weights and styles of existing and original typefaces. SoftCraft (Madison, WI) offers the Font Solution Pack, an IBM PC program that uses Bitstream typefaces or Hewlett-Packard-compatible bit-map fonts. You can install, scale, curve, rotate, reverse, and edit typefaces, and create custom character sets and special styles.

Fontographer, a product for the Macintosh from Altsys Corp. (Plano, TX), enables users to create characters from scratch. Six typefaces are also available that can be user-customized by adding special effects such as variable tints and outline weights. You can configure the fonts, logos, and characters created into bit maps for the ImageWriter LQ or LaserWriter

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IISC, or into user-defined PostScript fonts for PostScript compatibility.

With Publisher's Type Foundry by ZSoft Corp. (Marietta, GA), you can create custom fonts, logos, and symbols from scanned typefaces or from scratch. Publisher's Type Foundry has both a bit-map editor and an outline editor. Fonts can be translated to formats required for PostScript printers, as well as for applications such as Aldus PageMaker and Ventura Publisher. Running under Microsoft Windows, Publisher's Type Foundry requires scanned type to be entered into PC Paintbrush and then transferred into one of the font editors. With Type Foundry, users can also oblique and boldface the characters.

These are only a sampling of the font products on the market. There are obvious differences that users should examine closely for variety, flexibility, availability, and compatibility.

A Font's Golden Years

Most laser printers today come with built-in printer controllers. Thus, they can accept instructions from a PDL, together with downloadable fonts, in order to generate the page image. In the future, more and more laser-printer controllers will be resident in the hosts to which they are attached. Installing the printer controller in a workstation or personal computer simplifies communication to the printer and speeds loading of fonts from a disk. The disk can also be used for caching bit maps, thereby greatly improving the controller's performance.

Printer controllers, which are currently almost all ROM-based, will most likely become RAM-based in the future. This will provide a much higher level of flexibility. It's practical to have a RAM-based controller because it can be quickly booted from the disk. A RAM-based controller will provide an upgrade path to new font-scaling technologies and PDLs as they become available. This architecture will create a much higher level of openness than exists in today's ROM-based printer controllers.

Font management will, in time, become a standard feature of operating environments. With this enhancement, and without having to delve into the intricacies of font technology, software developers will find it easier to develop word processing, desktop publishing, and other application programs requiring fonts. At the same time, they will create a level of standardization that will encourage and improve typeface portability.

There is a trend toward more openness in digital fonts. So you can expect more and more operating environments, printers, and typesetters to have open font architectures that will allow all font vendors, as opposed to multiple and independent font vendors, to provide their products for those devices. More standardization of font formats will minimize the need for format conversion.

It's interesting that even today, some typesetter manufacturers continue to build devices that accept only type made by the manufacturer itself. But it's likely that users will demand more openness with respect to the source of fonts, especially as different pieces of equipment from different manufacturers get connected and used together. A trend toward openness and standardization will hasten the day when there is complete portability of digital fonts across application programs, operating environments, and output devices. Gutenberg would surely approve. ■

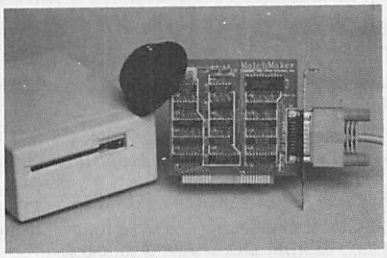
John Collins is vice president of technical development for Bitstream (Cambridge, MA). He holds a Ph.D. in electrical engineering from the University of London. He can be reached on BIX c/o "editors."

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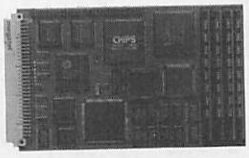
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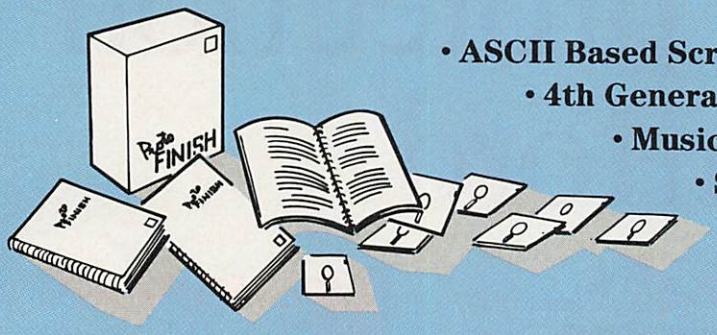
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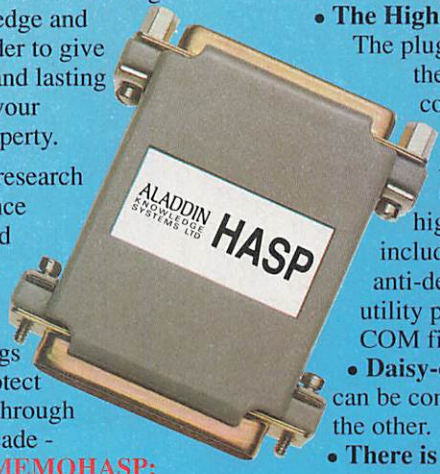
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MACH: THE MODEL FOR FUTURE UNIX

Will a new, object-oriented kernel change the face of Unix?

Avadis Tevanian Jr. and Ben Smith

Unix is over 20 years old. While the computer hardware for Unix has radically changed since Unix was first designed, the basic concepts of the operating-system kernel have remained the same.

The Mach kernel is designed to take advantage of new computer architectures and provide for the needs of modern programs. It is also a return to the original Unix concept of having only the most essential functions in the kernel—a concept that has been lost in the versions of Unix from the big-iron computer manufacturers, whose kernels can exceed 2 megabytes.

Great Ideas from a Small Team

A small group of researchers at Carnegie Mellon University started the design of Mach in 1984. They wrote the first lines of code in 1985. Originally, Mach was intended to support large-scale parallel computation. However, early on in the design phase, the team decided that designing only for large-scale parallel computation would be of limited life and utility. So they changed the design to make it independent of the hardware architecture. Mach was initially implemented on the VAX-11/780 and now runs on a wide range of hardware, including almost all VAX processors, the IBM RT PC, Sun-3 workstations, the Encore Multimax, the Sequent Balance 21000, various 80386 machines, and the NeXT Computer.

Mach is designed to handle problems associated with both parallel programming on multiprocessor machines and distributed programming, where the work is done by several separate computers communicating over a network. The concept of multiple threads of control executing in parallel within a single task facilitates parallel computing. A capability-based interprocess communication mechanism eases distributed programming. Finally, an extremely powerful virtual memory system allows applications of all sizes to efficiently share the memory resources of these complex architectural designs. With Mach, these very same concepts work equally well on inexpensive, single-processor machines.

To derive Mach, the Carnegie Mellon team extended the model of Unix computing by adding five abstractions: the *task*, the *thread*, the *port*, the *message*, and the *memory object*. Obviously, the language and concepts of object-oriented programming permeate the design of Mach. Many people call Mach an "object-oriented operating system."

The Mach kernel maintains only the most basic services: processor scheduling, interprocess communication, and management of virtual memory. All other services are *service tasks*, independent user-level programs.

Tasks and Threads

Mach splits the traditional Unix abstraction of a process into a task and threads. A task is the environment in which threads run. It includes protected access and control of all system resources, including the CPUs, the physical I/O ports, and memory (virtual and real). The structures associated with files are in the domain of the task. A task address space uses a structured map of memory objects (see below).

A thread is an entity (an object) capable of performing computation, and for low overhead, it contains only the minimal state necessary. Another term for a thread is a *lightweight process*. A thread contains the processor state, the contents of a machine's registers. All threads within a task share the virtual memory address space and communications privileges associated with their task. The Unix abstraction of a process is simulated in Mach by combining a task and a single thread. However, Mach goes beyond this abstraction by allowing multiple threads to execute simultaneously within a task. On a multiprocessor, multiple threads can, in fact, execute in parallel on separate processors, whereas on a uniprocessor they only conceptually execute in parallel.

Ports, Port Sets, and Messages

A port is a communications channel, a sort of object reference for tasks, threads, and other objects. Application programs

continued

Mach on the NeXT Cube

While most current users of Mach are content to rely on Unix compatibility, NeXT has found the basic functionality of a Unix system to be insufficient to produce high-quality end-user applications software. NeXT utilizes the Mach functionality for communication between applications and window servers, sound playback and recording servers, and other applications.

Applications on the NeXT Computer convey information to a user according to the NextStep User Interface, which comprises several components: The Window Server manages all the windows on a display; the Application Kit is an implementation of the classes that define the user interface; the Interface Builder is a tool that allows the user interface for NextStep-conforming applications to be built with little or no programming; finally, the Workspace Manager provides a graphical user interface to a user's files and applications.

Two major types of communication occur between NextStep applications. First, applications communicate with the Window Server in order to implement a graphical user interface according to the client/server model. Second, applications communicate with each other using the Workspace Manager as a rendezvous point. Both types of communication are performed using Mach's intertask message-passing primitives.

Sound playback and recording make extensive use of Mach features. On a NeXT machine, compact-disk-quality sound can be synthesized in a digital signal processor. The device driver responsible for controlling the DSP and the sound direct-memory-access channels is accessed using Mach's message-passing primitives. This allows great flexibility in how the hardware can be accessed and provides network-transparent access to the driver. Threads are also used by high-level sound software to control sound I/O for an application that needs to perform normal processing while playing or recording sounds.

communicate with objects managed by the kernel and server tasks through the objects' ports. This is the software counterpart to the communications ports on the hardware. An object is said to have "access rights" to a port if it has dealings with that port. A port can move around from object to object, like moving a board and the cables connected to it from one machine to another.

The object that has the port screwed into it is said to have *receive access rights* to the port. Receive access rights imply send access rights as well. More than one thread may concurrently attempt to receive messages from a given port, but all the threads must be within the same task. In other words, only one task can have receive access rights to the port.

The object intending to pipe messages to the port has *send access rights*. More than one thread and more than one task can hold send access rights to any port. Messages travel from the object with send access rights to the port on the object with receive access rights.

For the time being, there is also a third port access right, *ownership*, which determines which object gains receive rights when these rights are relinquished. The Mach documentation implies that ownership rights will probably not be implemented in future releases—a definite discouragement for using this privilege.

Both tasks and threads have a special *kernel port* by which the kernel recognizes them.

Some special types of ports are associated only with tasks: the *notify port*, through which the task receives messages from the kernel about its port access rights and the status of messages it has sent; the *exception port*, through which the task receives messages from the kernel when an exception occurs (see "Exception Handling," below); and the *bootstrap port*, with which new tasks attach to any services that they need.

Threads also have some special types of ports: the *thread reply port*, for early messages from a young thread's parent and early remote procedure calls (RPCs); and the *thread exception port*, similar to the task exception port. Ports can be strung together into *port sets*, through which several objects can grab any messages from a single message queue.

A message is a string of data prefixed by a header. The header describes the message and its destination. The body of the message may be as large as the entire address space of a task. There are *simple messages*, which don't contain any references to other ports; and *non-simple messages*, which can make reference to other ports—conceptually similar to indirect addressing.

Messages are the primary way that tasks communicate with each other and the kernel. They can even be sent between tasks on different computers.

The Memory Object

Each Mach task can use up to 4 gigabytes of virtual memory for the execution of its threads. This space is used for the memory objects but also for messages and memory-mapped files.

When a task allocates regions of virtual memory, the regions must be aligned on page boundaries. The task can create memory objects for use by its threads; these can actually be mapped onto the space of another task. Spawning new tasks is more efficient because memory does not need to be copied to the child. The child needs only to touch the necessary portions of its parent's address space. When spawning a child task, it is possible to mark the pages to be copied or protected (the child is prohibited access).

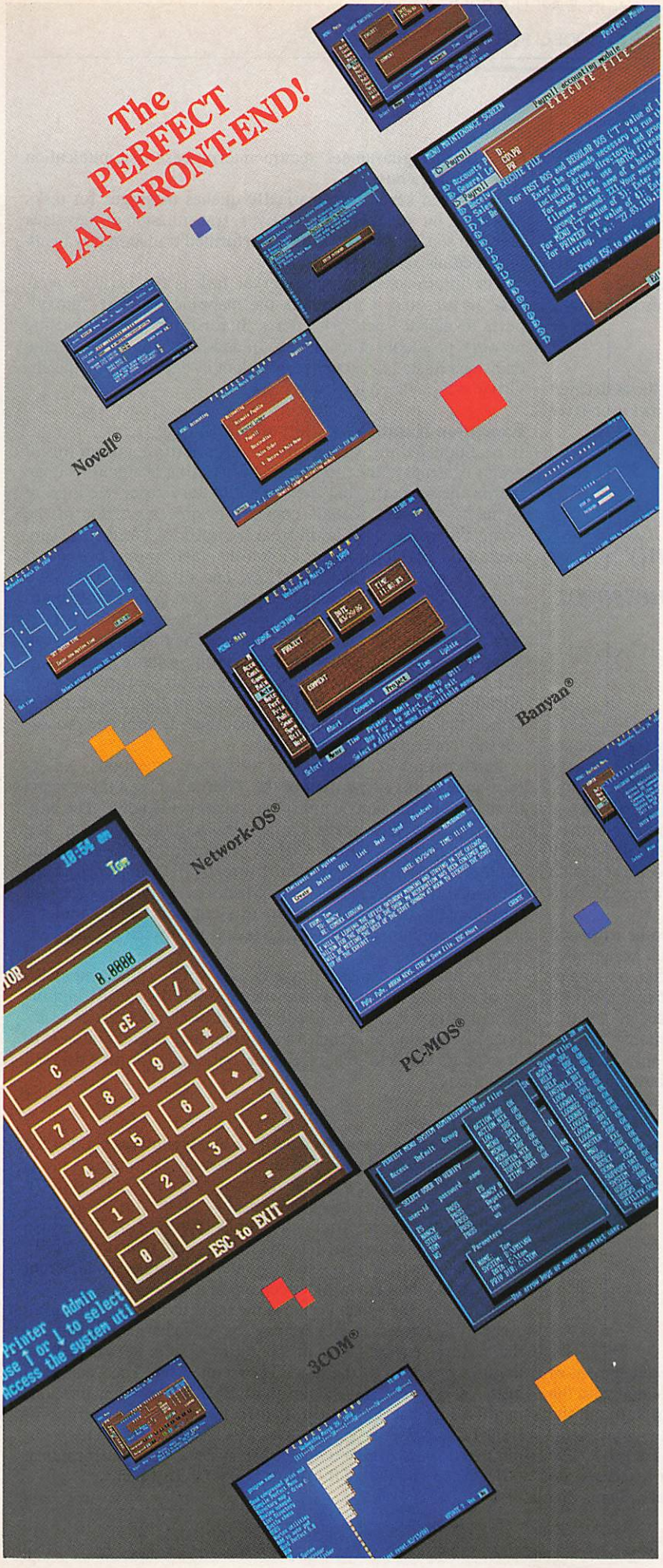
Since messages are actually mapped into the virtual memory resources of tasks, intertask (interprocess) communication is far more efficient than old-time Unix implementations where the messages are copied from one task to the limited memory space of the kernel and then to the task receiving the message. In Mach, the message actually resides in the memory space shared by the communicating tasks.

Memory-mapped files facilitate program development by simplifying memory and file operations to a single set of operations for both. However, Mach still supports the standard Unix file read, write, and seek system calls.

Virtual Memory

The Mach virtual memory system provides the programmer with a clean interface, which allows virtual memory to be allocated and deallocated at arbitrary addresses and sizes, restricted only by the page size of the underlying hardware. Applications can, on a page-by-page basis, specify access modes such as read-only, read/write, or shared. Finally, also on a page-by-page basis, virtual memory can be shared between

continued



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tasks in a controlled fashion that is based on inheritance.

The virtual memory system achieves portability by splitting its implementation into two parts. The first part, the architecture-independent part, is common to all implementations of Mach. The second part, the architecture-dependent part, is specific to each hardware architecture that Mach runs on. This split makes it possible for Mach to provide a consistent, high level of functionality on all hardware architectures with only a minimal porting effort.

Open Memory Management

Instead of limiting virtual memory semantics to those defined by the kernel, Mach provides an interface that allows user-level programs (external memory managers) to define the exact semantics of virtual memory that can be mapped into any task's virtual address space. Such programs are responsible for handling operations such as "page in" (when a page of memory is referenced) and "page out" (when a page of memory is moved out of the normal working set). In addition, external memory managers can instruct the Mach kernel to take special action on memory, such as restrict access to data in order to provide data consistency and security.

The Mach kernel guarantees that only authorized senders can send messages on a particular port.

External memory management allows Mach to be extended in powerful ways without changing the base Mach kernel. For example, network-consistent shared memory can be implemented by an external memory manager. The shared memory manager can use the external memory interface to control which pages of memory can be accessed by which machines at various times in order to guarantee control. Not only does this remove that complexity from the kernel, but it allows the shared memory manager to choose which algorithms it uses to enforce consistency and security.

The Mach Kernel and IPC

The kernel functions can be classified into the following five groups:

- Task and thread management
- Port management
- Message queuing and support
- Virtual memory management
- Paging management

The kernel is responsible for the creation and management of all tasks and threads, the structure of ports associated with the tasks and threads, the messages between objects (through the object ports), and the allocation of physical and virtual memory. It manages what and how port capabilities are used. The kernel guarantees that only authorized senders or receivers can send or receive messages on each particular port. Thus, the Mach kernel guarantees secure interprocess communication (IPC) within a host.

The Mach kernel automatically queues messages for tasks executing on its machine. However, transmission of messages between separate Mach hosts is performed transparently by an intermediate server task.

The intermachine-process-server task is the *network message server*, and it maintains the mapping of local "proxy" ports to global "network" ports. It forwards messages using network protocols of its choice. In addition, it is free to make decisions related to security, or lack of it, depending on the environment in which it is run.

Exception Handling vs. Signal Handling

In traditional Unix, *signals* are used for notifying programs of events external to the program. The handling of signals is done within the program, but the semantics vary from one kind of signal to another. Signals come from only a portion of the events that affect a program from the outside. Bus errors, segmentation and protection violations, arithmetic processor errors (e.g., underflow, overflow, and divide by zero), and events associated with debugging also need to be able to communicate with programs. External events that affect the execution of a program are called *exceptions*. The traditional ways of handling exceptions (through application program signal handling and kernel handling of hardware errors) separate the application program or service program from the hardware that caused the exception and assume that there is only one processor (no longer a valid assumption).

Mach has taken a generalized view of all exceptions. An exception requires suspension of the "victim" thread that caused the event and the notification of an exception handler. The handler performs some operations as a result of the exception, and then the victim is either revived or terminated. Because the handler is never within the victim thread, all the exception handling involves a form of RPCs. Mach ports and messages are the elements through which all this happens. The handler's port for communicating with the task is the thread (or task) exception port.

This design provides a single facility with a consistent method of handling all exceptions, a simple interface, full support for debuggers and error handlers, and no duplication of functionality within the kernel. In addition, and of great interest to developers and researchers, this design allows for user-defined exceptions.

System Layers

The Mach kernel provides only the basic primitives needed for building distributed and parallel applications. Although Unix is an operating system, it is also a complete environment suitable for use by developers and end users. Mach is just a kernel. The operating-system environment is built on top of it. But, since Mach makes few traditional operating-system decisions within the kernel itself, it is possible to build a completely different operating-system environment on top of it.

Currently, the Mach kernel is the basis for a BSD 4.3 Unix–compatible system. In this system, the Mach kernel implements the features particular to an operating-system kernel and the features provided by the Mach kernel interface. Unix compatibility is provided by the original BSD 4.3 implementation, modified for use with Mach. In effect, many of the internals of BSD 4.3 have been replaced with Mach equivalents. This technique yields a highly compatible system with performance often exceeding that of the original BSD 4.3 system.

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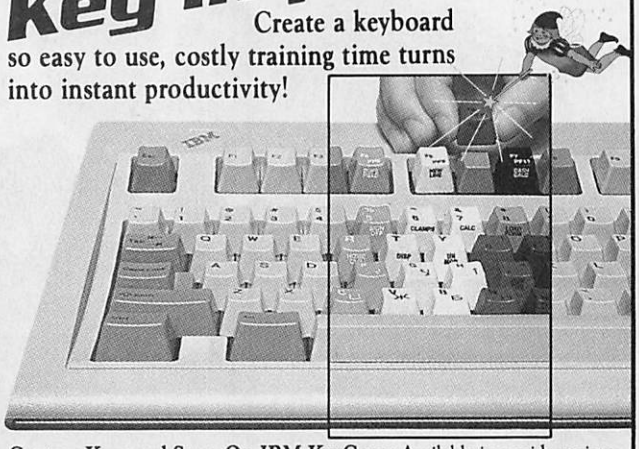
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OS/2 and Mach

Like Mach, OS/2 supports threads, virtual memory, and message-passing mechanisms. Although Mach and OS/2 provide similar types of functionality at the lowest levels, they differ in important ways.

OS/2 threads, for example, have some unusual semantics. Instead of the Mach model of all threads being equal, OS/2 treats some threads (e.g., the first thread in a process) specially. It manages virtual memory in segments, rather than pages—a finer grain and more flexible control than segments. Also, OS/2 imposes some other restrictions, such as the use of different memory allocators for different-size memory regions. Rather than provide one coherent mechanism for interprocess communication, OS/2 provides many different mechanisms (e.g., semaphores, pipes, queues, and signals). OS/2 lacks multiuser operations. Finally, OS/2 was designed to run on Intel 80286/80386 processors and is not portable to other processor families. This is not to say that OS/2 doesn't do well in its own niche, but it is not as complex or universal as Mach.

The Future of Mach

Unix compatibility makes Mach attractive to a wide audience by allowing it to transcend its role as a research project and emerge as a viable commercial operating system. The NeXT Computer already provides an excellent example of how to tie visual displays to audio input and output. The primitives of Mach were essential for NeXT to implement this functionality efficiently in a true multitasking environment. (See the text box "Mach on the NeXT Cube" on page 412.)

Mach is also influencing how other systems evolve. In the future, more and more systems are likely to support Mach features. Mach has become the platform for experimental Unix operating-system work. For instance, Trusted Information Systems, under a Defense Advanced Research Projects Agency contract, evaluated Mach as a possible base for a verifiably secure operating system, a "trusted system" meeting the B3 level of security as specified in the National Computer Security Center's "Orange Book." (See "Safe and Secure?" in the May BYTE.) Researchers at Trusted Information Systems ascertained that Mach's design made implementation of classification labels and access control lists much easier than in traditional Unix. The design separation of the kernel and services made modification of the operating system much more straightforward and easier to verify as being a trusted system. They have gone on to build a proof-of-concept prototype trusted system. But until Mach is free of BSD code, a truly trusted Mach operating system will not be possible. Meanwhile, they are working with the Mach team at Carnegie Mellon to ensure that facilities for trusted systems be properly implemented in future releases.

Work on Mach continues at Carnegie Mellon and organizatons such as NeXT. Eventually Mach will stand on its own and be completely free of BSD code. It will have been shaped by the tortuous tests of many other institutions, including industry and government. Thanks to the availability of Mach on the NeXT Computer, the ideas of thousands of researchers and students will add to its clever design and continue to shape it for modern computer design and software. It's a great example for all developers of applications and operating systems. But as operating systems go, Mach is very young, and few people understand all the possibilities it really provides. ■

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INSIDE EISA

Probing the mysteries of the newest industry standard for IBM PCs

This fall marks the advent of an important new standard in the Intel/IBM PC–compatible marketplace: the Extended Industry Standard Architecture, or EISA (pronounced "ee-sa"). Created by a consortium of computer, peripheral, and chip vendors ranging from Compaq to AST Research to Intel, EISA machines are built around a unique 32-bit-wide bus structure that's downward-compatible with older Industry Standard Architecture (ISA, or "eye-sa") peripheral cards (i.e., cards intended to work in the IBM PC, XT, or AT).

When IBM announced the PS/2 series of computers, it announced that these machines used a new 16-/32-bit bus—the Micro Channel—which was not compatible with the ISA bus. Users balked at the high cost and limited availability of peripheral cards for the Micro Channel, and manufacturers balked at IBM's demands for licensing fees—which included not only a percentage of revenue acquired from using the new bus design, but also a retroactive fee for use of the ISA bus that IBM was putting out to pasture.

The result was the formation of the EISA consortium—centered around a group of clone makers, the "Gang of Nine" (i.e., Wyse, AST Research, Tandy, Compaq, Hewlett-Packard, Zenith, Olivetti, NEC, and Epson—mnemonically, watchzone). Struggling to finish their EISA specification while the Micro Channel gained market share, this group kept information on EISA mostly under wraps. You could obtain detailed information about the bus only by signing a nondisclosure agreement and paying $2500.

The lack of publicly available information on EISA has led some to call it a "vapor bus." However, by the time this issue of BYTE arrives on the newsstand, the wait will be over, and EISA systems—and the specification—will be available to everyone. See "EISA Arrives" on page 93.

What's inside EISA? And how does it work? The best way to understand EISA is to trace its evolution from its earliest roots: the 8-bit backplane of the original IBM PC.

Recapitulating Phylogeny

The original PC and XT bus was introduced in the first IBM PCs in 1981. It's a relatively simple synchronous 8-bit bus with parity protection and edge-triggered interrupts, which means that each interrupt line can be used by only one adapter card (see table 1).

The original PC bus had no provision for an external bus master; either the host CPU or the direct-memory-access (DMA) controller on the motherboard controlled the bus at all times.

Enter the IBM PC AT, circa 1984. IBM wanted to extend the 8-bit IBM PC bus to 16-bit operation in a compatible way, so all the signals on the original 62-pin connector were maintained and a new connector was added at the bottom. Table 2 shows the additions that created the AT bus.

IBM added a number of features to the AT for downward compatibility. Because the AT's 80286 ran faster than the original PC's 8088, the company added a wait-state generator to lengthen bus cycles. Also, the one previously unused line was assigned a function: Pin B8 became the $\overline{\text{0WS}}$ (zero wait state) line. When this line is pulled low, some or all of the wait states generated by the AT motherboard are removed. By putting this signal on the 62-pin connector, IBM let manufacturers make fast 8-bit boards as well as fast 16-bit boards.

The new connector, which had two rows of 19 pins each, added four new address lines (LA20–LA23), plus copies of three lower address lines (LA17–LA19). Why the duplication? Because the address lines on the original PC bus were latched, and the latching process caused propagation delays that would slow down peripheral boards. (See the glossary on page 423 for definitions of *latched* and other bus-related terms.) By providing these unlatched address lines, the AT bus let 16-bit cards find out early in the cycle whether they were being addressed. They could then activate special signals that said, "I'm a 16-bit card; please make this a 16-bit cycle, if you can."

Those special signals—$\overline{\text{MEM CS16}}$ and $\overline{\text{I/O CS16}}$—are key to the AT bus's downward compatibility. If the 80286 attempts to perform a 16-bit access to a board and one of these signals is not asserted, special hardware on the motherboard takes over and causes two 8-bit cycles to be performed.

Alas, there was a catch. Only seven unlatched address lines could fit on the connector, meaning that this "early warning" could tell the board only which 128K-byte region of memory was being addressed. Thus, memory boards that didn't consume a full 128K-byte block of scarce real-mode address space could not activate the signal, and thus couldn't do 16-bit transfers. In practice, this meant that most EMS boards and memory-mapped peripherals were forced to do transfers 8 bits at a time, even over the 16-bit AT bus.

Enter EISA

Like the AT bus before it, the EISA bus was built on the older standard by adding more address lines, more data lines, and more control signals. Before this could be done, however, its designers had to generate a firm specification for the ISA bus.

The timings of the PC and AT backplanes were never formally specified in

continued

Table 1: *Because of its simple design, each interrupt line can be used by only one adapter card.*

PC AND XT BUS SIGNAL LINES

Lines	Description
A0-A19	Twenty system address lines. During I/O cycles, only the lowest 10 lines are actually used.
D0-D7	Eight bidirectional data lines.
ALE	Address latch enable. This signal goes high to indicate that a valid address is present on A0-A19 during a memory access.
IRQ2-IRQ7	Six maskable interrupt request lines.
DRQ1-DRQ2, DACK1-DACK3	DMA request and acknowledge lines. There's no DRQ0 on the bus; DMA channel 0 is used for DRAM refresh on the PC and the XT.
IO CH RDY	A signal used by a memory or peripheral board to generate wait states.
IOR, IOW SMEMR, SMEMW	I/O and memory read and write strobes.
OSC	A 14.31818-MHz clock used by some video boards. It's not synchronized with respect to the rest of the bus.
CLK	The bus clock signal (4.77 MHz in the original PC and proportionately faster on later machines). This clock is synchronized with respect to the read and write strobes.
AEN, TC	Address enable and terminal count. These control signals are used during DMA cycles.
IO CH CHK	Alerts the processor to parity and other errors via a nonmaskable interrupt.
RESET DRV	Indicates that the system is being reset.
+5VDC, –5VDC, +12VDC, –12VDC GND	Power-supply rails.

any published IBM document. EISA, which was to extend the bus yet again, could not be so lax. It needed to rigorously define not only the new standard, but also a set of timings that would retain compatibility with the older ones. Fortunately, the participants in the EISA consortium were old hands at IBM clone design and probably the best people to do the job.

As the specification developed, the developers exchanged timing information as spreadsheet files. The spreadsheet format let them watch what happened to the worst-case timings as they tuned the specification, and it helped them flag problems.

Table 3 shows the resulting new signals. The new pins for the EISA bus were placed physically between the pins of the ISA bus. (See figure 1 for a comparison of the lines.)

Covering All the Bases

Now that I've listed the signals that EISA adds to the standard PC bus, I'll look at some of the features they provide. A key feature of EISA is that the host or any bus master can access any memory device or peripheral in the system, even if their bus widths differ.

The EISA bus controller can adapt accesses from the host CPU, a 32- or 16-bit EISA master, or even an ISA bus master to any of five kinds of slaves on a cycle-by-cycle basis. These include EISA 32-bit slaves, EISA 16-bit slaves with burst capability, EISA 16-bit slaves without

Table 2: *New signal lines added in the AT's 16-bit bus. By duplicating some of the address lines, the AT bus maintains backward compatibility while providing unlatched address lines for faster cards.*

ADDITIONAL SIGNAL LINES FOR THE 16-BIT ISA BUS

Lines	Description
D8-D15	The eight new data lines.
SBHE	System bus high enable, which indicates when these data lines are being used.
IRQ10-12, IRQ14-15	More interrupt lines. IRQ13 is absent because that interrupt is reserved for the math coprocessor.
DRQ0, DACK0, DRQ5-DRQ7, DACK5-DACK7	More DMA control lines for new DMA channels. On the AT, DMA channel 0 is no longer used for refresh and is therefore available for other purposes.
MEMR, MEMW	Memory read and write strobes. These signals are active on all memory cycles, while SMEMR and SMEMW are active only on cycles that fall within the address space of the PC for compatibility reasons.
MASTER	A new signal that lets a board become a bus master on the AT bus. A bus handoff using this signal requires several cycles, and the master must relinquish the bus periodically to allow memory refresh (or do the refresh itself).
MEM CS16, I/O CS16	Signals used by a peripheral board to tell the motherboard that it's capable of handling a 16-bit data transfer.

burst capability, ISA 16-bit slaves, and ISA 8-bit slaves. How is this accomplished? The answer lies in a key feature of the EISA bus—and its controller—called *cycle translation*.

Suppose that a 32-bit EISA bus master card wants to do a write into a memory location on an 8-bit ISA card. The bus master will begin by requesting the bus, setting up the address and data, and asserting the $\overline{\text{START}}$ signal. It will then look at the signals $\overline{\text{EX32}}$, $\overline{\text{EX16}}$, $\overline{\text{MEM CS16}}$ (called $\overline{\text{M16}}$ in the EISA specification), and $\overline{\text{0WS}}$. As these signals return, the bus controller samples them, too.

When the bus master and the bus controller see that the cycle can't be completed with a simple 32-bit transfer, the bus controller takes over. Having sampled the address and data from the bus master, the bus controller begins to drive the same signals onto the bus while the bus master is still doing so. (There's no conflict and no glitch because both are driving each line the same way.) Then, half a cycle of the bus clock later, the bus master bows out by turning off its drivers. The bus controller, now in charge of the cycle, executes four separate ISA byte transfers to deliver the data, much the same as the AT motherboard can break up a word access into two byte-size accesses.

The beauty of this "handoff" facility is that none of the DMA peripherals or bus masters need to contain the byte-shifting and cycle-generating logic to handle the wide variety of possible transfers. For example, Intel's 32-bit bus master chip, the Bus Master Interface Controller (BMIC), can handle only 32- and 16-bit burst transfers without help, but the other combinations are neatly handled by the EISA Bus Controller (EBC) chip (see table 4).

Another novel situation occurs when a 16-bit master addresses the upper word of a 32-bit memory location on a 32-bit slave. The EBC handles this situation by copying the information from the lower two byte-wide lanes of the data bus up to the higher two lanes, so that the information arrives at the right place. This procedure is known as *copy-up*, and it lets a 16-bit master access a 32-bit slave without containing drivers for all 32 data lines.

Fast Transfers

One of EISA's key selling points is raw speed. Under the right conditions, EISA peripherals can do 32-bit burst transfers at up to 33 megabytes per second. This sort of bandwidth is necessary when a machine is servicing a high-speed LAN (e.g., Fiber Distributed Data Interface, or FDDI), a fast disk drive (e.g., IPI or SCSI-2), or a high-resolution graphics display.

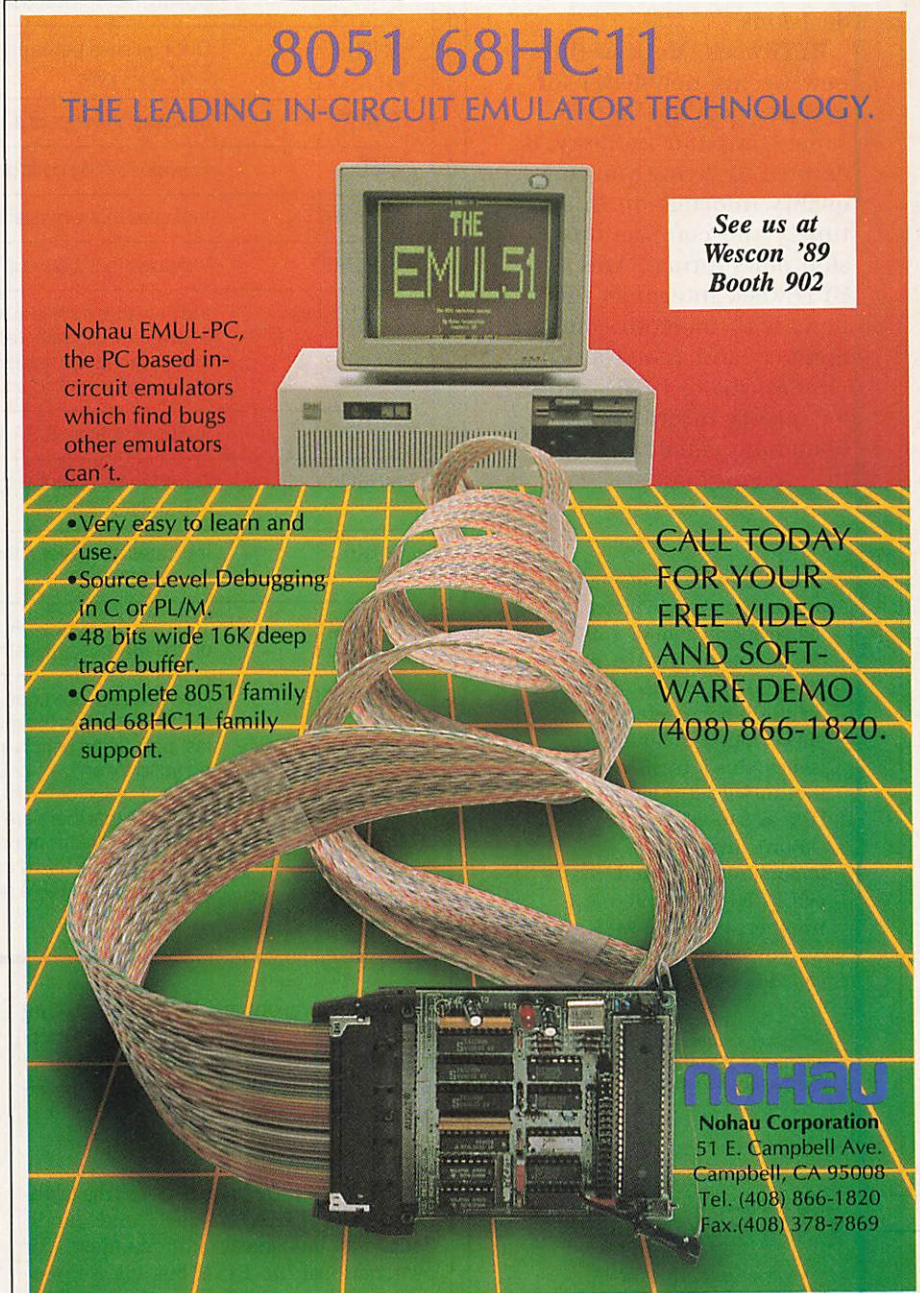
But not all bus transactions will fall into this category. If you're using ISA peripheral cards, they will exhibit lackluster performance compared to EISA-specific cards.

Shared Interrupts

One of the most common and frustrating problems you encounter when expanding an IBM PC or compatible is a lack of available interrupt lines. ISA machines do not allow sharing of interrupt lines; each is edge-triggered and driven by a TTL tristate driver.

EISA, however, provides pull-ups on the interrupt lines and can make them level-sensitive. This means that EISA cards, which use open-collector drivers to drive the interrupt lines, can share

continued



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Table 3: *Signal lines added to ISA to create EISA. The addition of the new lines, including 32-bit data and address lines, almost doubles the total number of lines.*

SIGNAL LINES ADDED TO ISA TO CREATE EISA

Lines	Description
$\overline{BE0}$-$\overline{BE3}$	Byte enables. These signals indicate which byte lanes of the 32-bit data bus are involved in the current bus cycle. They're analogous to the $\overline{BE0}$ through $\overline{BE3}$ signals on the 80386 and 80486 microprocessors.
M-IO	Distinguishes between an EISA memory cycle and an EISA I/O cycle.
$\overline{START}$	Indicates the start of an EISA bus cycle.
$\overline{CMD}$	Provides timing control within an EISA bus cycle.
$\overline{MSBURST}$	Indicates that a master is capable of performing burst cycles.
$\overline{SLBURST}$	Indicates that a slave is capable of accepting burst cycles.
EX32, EX16	Indicate that a slave is an EISA board and can support a 32- or 16-bit cycle, respectively. If neither of these signals is asserted at the beginning of a cycle, the bus falls back to an ISA-compatible mode for that cycle.
EXRDY	Indicates that an EISA slave is ready to terminate a cycle.
$\overline{MREQn}$	Asserted by potential master number *n* to request the bus.
$\overline{MAKn}$	Indicates to master *n* that it has been granted the bus.
D16-D31	The new data lines that, combined with the data lines on the ISA bus, make the EISA 32-bit data bus.
LA2-LA16, LA17-LA31	New address bus lines. Like LA17-LA23, these lines aren't latched on the motherboard and so provide a fast path to the peripheral boards. Note that there's no need for an LA1 or LA0; the byte enable lines indicate which of the four byte lanes are used. Also note that there are now 32 address bits, supporting the full address range of the 80386 (rather than the 24-bit address range of the 80286). This lets system RAM grow above 16 megabytes.

these scarce resources. Beware of mixing EISA and ISA cards on the same interrupt line, however; an ISA card cannot share an interrupt, even when plugged into an EISA backplane.

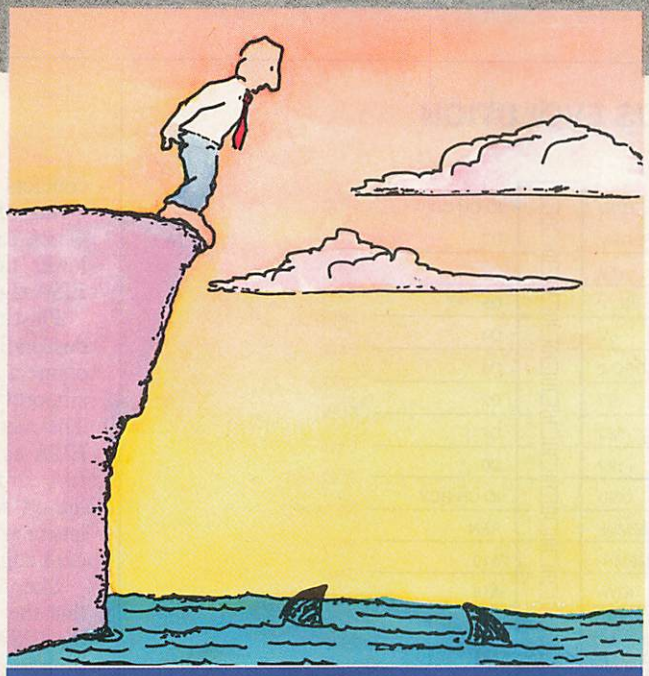
Taking Turns

The memory refresh controller, the highest-priority DMA channel, and candidates for bus mastership compete for ownership of the EISA bus via a three-way rotating arbitration scheme. This scheme guarantees that no bus master will ever starve, although it is possible for a low-priority DMA channel to be starved for use of the bus. It also ensures that memory will be refreshed on a regular basis. In addition, the Intel chip set contains a special watchdog timer that makes sure no one entity retains control of the bus for too long. If this timer expires, the master is removed from the bus and a nonmaskable interrupt is generated on the host CPU.

The EISA Connector

The EISA connector, developed by Burndy, is designed to be 100 percent compatible with existing ISA cards. The

continued



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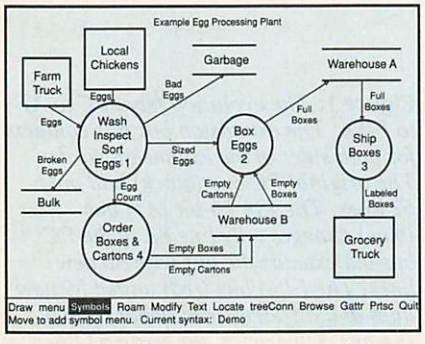
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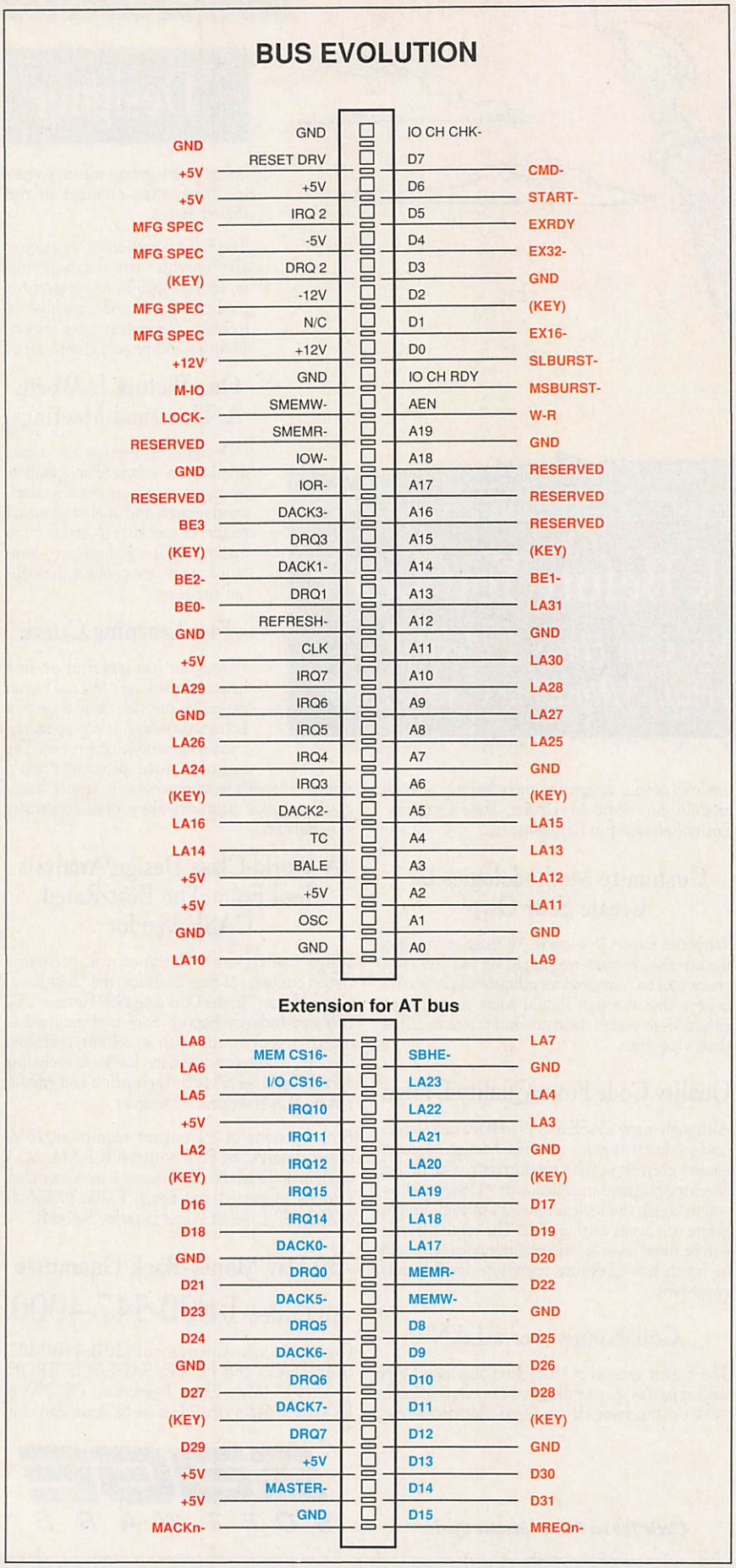


Figure 1: *The evolution from PC to AT to EISA. The expansion bus has contacts for both sides of the expansion cards. The original PC bus (black) had only 62 lines. The ISA 16-bit (AT) bus (blue) changes only line 8A of the PC bus but extends the bus with 36 new lines. The EISA bus (red) added 59 new lines at a different card depth from the ISA bus. Otherwise, the basic 62 lines stayed the same. Note that EISA attempts to "wrap" power and ground lines around clock lines and to position power rails so that they can be combined into thick traces on a motherboard. EISA nearly doubles ISA's number of bus lines.*

contacts in the card edge connector are arranged in two tiers: an upper tier, which carries all the ISA signals, and a lower tier, which carries all the new EISA signals (see figure 2).

Plastic keys prevent an ISA card from descending far enough into the slot to connect with the EISA signals but slide smoothly into notches in an EISA card. The metal "fingers" on the edge of an EISA card are thinner than those on an ISA card, and the new signals are interleaved with the old. This arrangement lets nearly twice as many leads reach the card edge.

Skeptics originally voiced concern that the insertion and removal forces of the EISA connector would be extremely high, but this has not turned out to be the case. I found that I was able to insert and remove EISA cards with one hand with relatively little effort.

The Intel Chip Set

Intel's EISA chip set—currently the only game in town—consists of three key components (see figure 3): the Integrated System Peripheral (ISP) and the aforementioned BMIC and EBC.

The EBC generates cycles on the EISA bus and manages the buffers that connect it to the host CPU's local bus. The EBC also provides reset signals for the CPU and the cache controller, and it supports snooping on the EISA bus for either the 82385 or the 80486's internal cache. (It's not clear, however, whether it's possible to use the EBC with a more powerful cache controller or with a write-back cache.)

The EBC is closely coupled to (and, in fact, can't run without) the ISP. The ISP

continued

EISA vs. the Micro Channel

IBM announced its Micro Channel architecture in 1987. Because EISA is being released more than two years later, its designers have had the benefit of being able to track industry experience with IBM's design. (Intel has developed both a Micro Channel chip set and the first EISA chip set.)

Some similarities are found between the two standards. As is true with Micro Channel systems, EISA systems can do full 32-bit transfers and can configure themselves automatically. (EISA systems can even tell you how to set the DIP switches on older ISA-type cards). But unlike the Micro Channel, the EISA bus is fully synchronous and can perform cycles in long rapid-fire bursts. (The maximum throughput of the Micro Channel is 20 megabytes per second, while the EISA bus can support a maximum burst transfer rate of 33 megabytes per second.)

It may be easier to manufacture EISA boards than Micro Channel cards. They sport nearly double the surface area, making expensive surface-mount technology less of a necessity. An EISA adapter can use more than twice the power of a Micro Channel card. This will make peripherals like on-the-card hard disks, relay boards, and intelligent I/O boards with a large amount of RAM (e.g., disk-caching controllers and laser printer controllers) simpler and cheaper to implement on EISA than on the Micro Channel.

IBM makes Micro Channel machines with both 16- and 32-bit CPUs today. But while it's possible to build an EISA system with a 16-bit host processor (e.g., a 16- or 20-MHz 80286), it may be a while before you see such systems on the market. Intel—in an attempt, perhaps, to discourage the use of these second-sourced processors—supports only the 80386 and 80486 with its EISA chip set. Since Intel's chips are, at this writing, the only ones available to support the EISA bus, users may have to wait for silicon from other vendors before they can enjoy the economic benefits of the 80286—or even Intel's own 80386SX.

EISA's main advantage is that it does not have to "catch up" to the Micro Channel right away in order to be useful. Users can install cards designed for ISA machines while waiting for fast EISA cards to appear.

Glossary

bus master The entity that drives the address lines and the control signals for a bus cycle; with EISA, the bus controller can operate some of the lines on behalf of the bus master.

DMA Direct memory access, the process by which information is transferred between two slaves on the bus (e.g., a memory card and an I/O device), under the supervision of a DMA controller.

edge-triggered An edge-triggered interrupt is one that is activated by a transition in an interrupt signal on the backplane. Compare to **level-sensitive**.

ISA The Industry Standard Architecture, an unofficial designation for the bus upon which the IBM PC AT and compatible systems are built.

latched A signal is latched when its logic level is sampled into and held by a flip-flop. The flip-flop, or latch, is a memory element that is guaranteed to maintain its current output until explicitly set to a different value.

level-sensitive A level-sensitive interrupt is triggered by a specific level (high or low) of that signal. Electrically, it is possible for more than one source to drive a level-triggered interrupt line, but not an edge-triggered one. Compare to **edge-triggered**.

open-collector An open-collector bus line is one that is normally held at a logic high level by a pull-up resistor. Such a line can be pulled low by a chip output that presents a substantially smaller resistance between that line and a low logic level (ground). An output that drives an open-collector line usually consists of a single transistor whose collector is attached to the pin and nothing else (hence the name open-collector). The transistor is driven to saturation (i.e., turned on all the way) to present the necessary low resistance between the signal line and ground.

parity protection A system with parity protection includes 1 or more bits that accompany the data and indicate whether the number of ones (or zeros) in the data is odd or even. Parity bits can be used to check the integrity of the data. Virtually all IBM PC–compatible memory has 1 parity bit for each 8 bits.

refresh The process by which the DRAM chips are continuously recharged, without which they will lose the data they contain.

reset signals Signals that reset chips (e.g., the CPU) to their power-on conditions.

snooping The process in which a memory cache watches to see how peripherals are accessing memory. (See "Caching in on Memory Systems," March BYTE.)

synchronous In a synchronous system, all state transitions, including changes in the states of bus lines, are synchronized with the transitions of a clock signal. In an asynchronous system, objects can change state at any time.

tristate A driver whose output can be at a low logic level, a high logic level, or high impedance—which means that it does not control the bus line at all.

wait-state generator A circuit that causes a CPU (or other bus master) to increase the length of a bus cycle to accommodate slow memory or peripherals.

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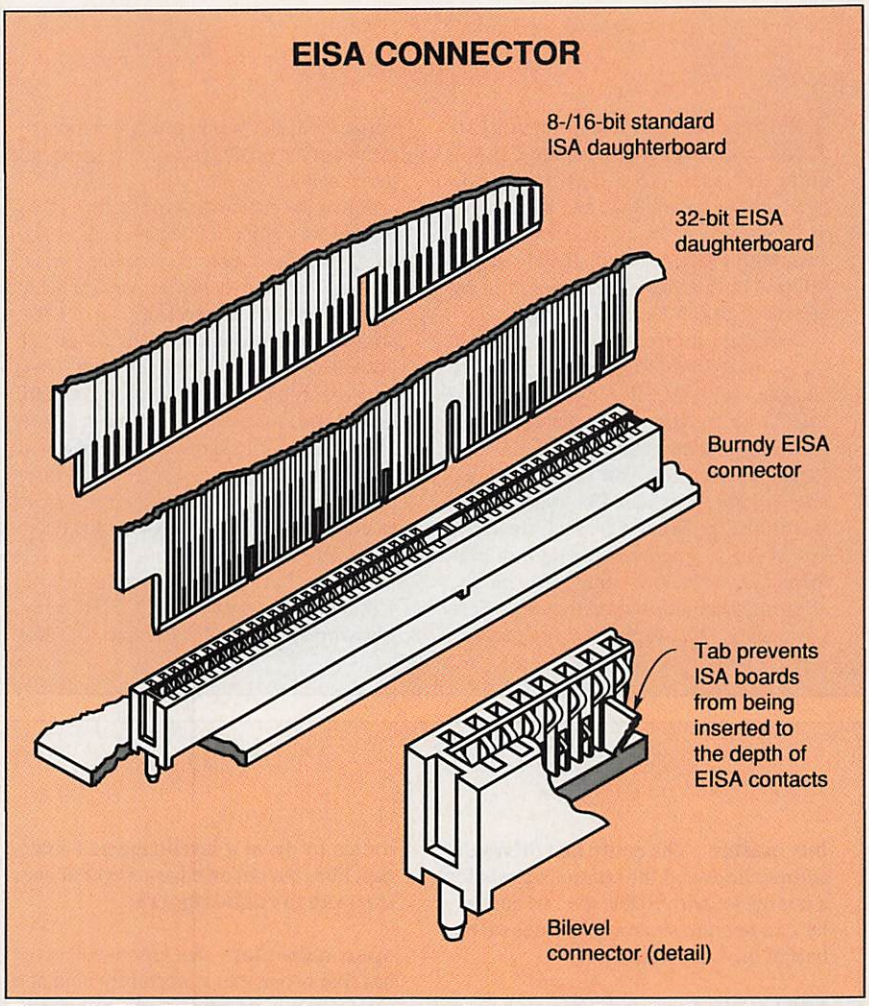


Figure 2: *The EISA two-level expansion card connector allows backward compatibility with the ISA card in the same slot, while letting EISA cards have twice as many signal lines.*

Table 4: *The EISA bus controller needs to step in to help a bus master complete a cycle. The Intel Bus Master Interface Controller has a downshift feature that lets it do 16-bit transfers by itself, even if it's configured as a 32-bit master. A board that can do this is called a "downshiftable master."*

	WHEN THE BUS CONTROLLER STEPS IN			
MasterSlave	**32-bit EISA**	**16-bit EISA with burst capability**	**16-bit EISA**	**ISA**
32-bit EISA	B	M	M	M
16-bit EISA	C	B	B	M
Intel BMIC (32-bit with "downshift" capability)	B	B	M	M

B = Burst-mode cycle possible.
C = Copy-up cycle. EBC copies the contents of the lower two byte-wide lanes onto the upper two byte lanes, so the 16-bit slave does not need to drive them directly.
M = Mismatch. EBC performs one or more cycles on behalf of the master.

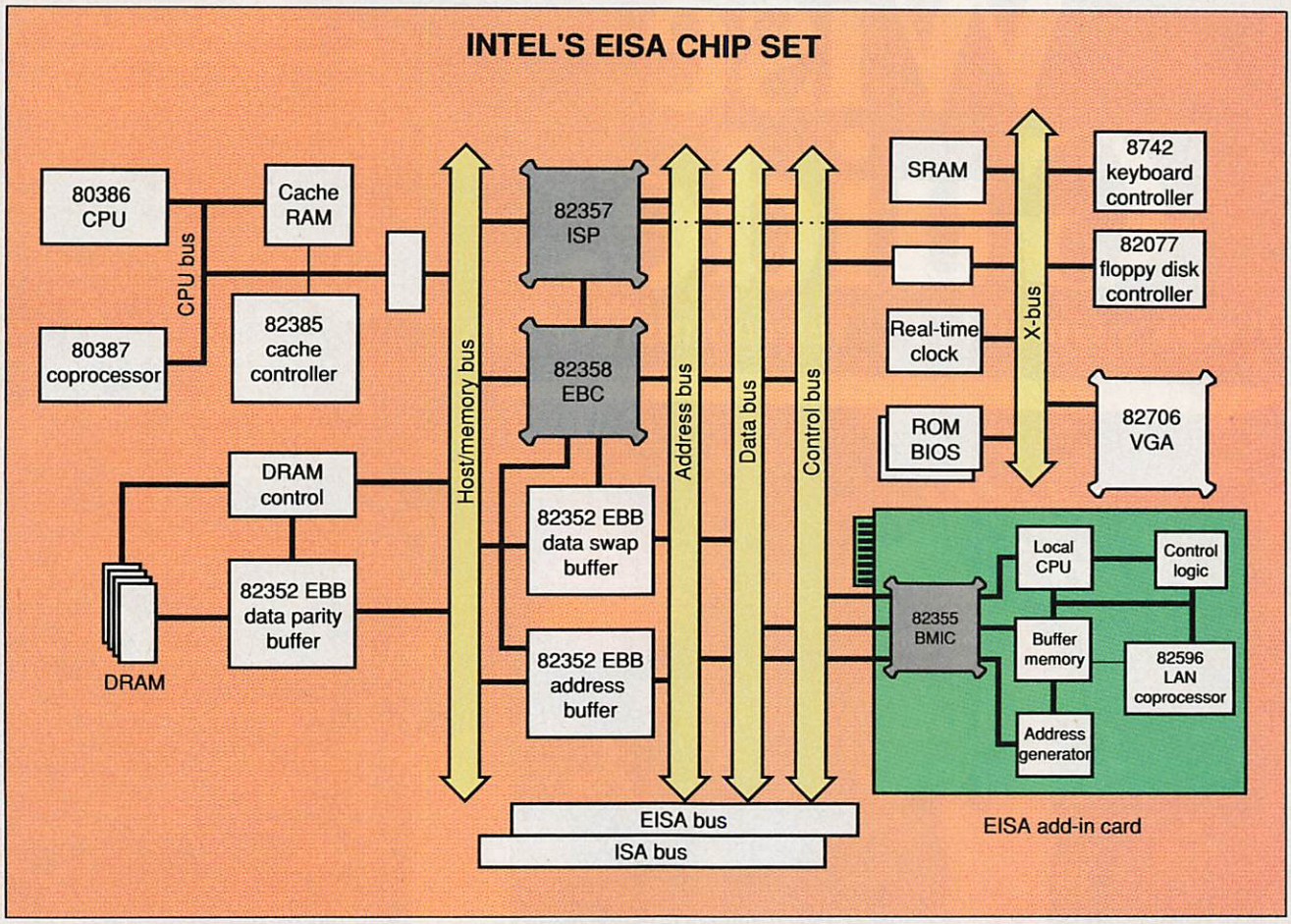


Figure 3: *The Intel chip set for supporting EISA consists of the 82358 EISA Bus Controller, the 82357 Integrated System Peripheral, and the 82355 Bus Master Interface Controller.*

provides the host CPU with an interrupt controller, a DMA controller, counters, and timers. It also manages DRAM refresh, performs EISA bus arbitration, and tests for memory parity errors. The ISP even has a "slowdown" mode that delays the CPU and makes it appear to be running at a slower speed—a necessary feature for certain copy-protected software.

Because these two chips integrate so many necessary system components along with the EISA functions, manufacturers who use them are unlikely to use third-party AT chip sets (e.g., those made by Chips & Technologies) in the same machines. Thus, these companies will most likely have to develop their own complete chip sets to cash in on the market for EISA machines.

The final component in the Intel chip set is the BMIC. It's intended to be used as a bus master interface on intelligent peripheral cards, and it has a local bus interface that's specifically tailored for use with the 80186. The host can communicate with the processor on the peripheral card using "mailbox" and "doorbell" registers and/or via an interface that lets an entity on the EISA bus access the peripheral card's local address space. It's also possible to use the BMIC on a card that doesn't have a local CPU.

Identifying EISA Products

Every EISA card supports a product identifier, which is accessible at a preassigned address determined by the slot the card is in. EISA product identifiers identify a peripheral card the same way that Micro Channel card IDs do, but with one important difference: EISA's product identifiers are not centrally managed, as IBM's are. The manufacturer creates them, following guidelines published by the EISA consortium.

Which to Buy?

The mysteries of EISA have fostered a wait-and-see attitude in the industry. Many corporate customers, unsure which standard will win, have deferred computer purchasing decisions until they know more about EISA.

By the time this article goes to press, there should be real EISA machines that users can see, benchmark, and compare to systems that use the Micro Channel (see the text box "EISA vs. the Micro Channel" on page 423) and other bus architectures. ■

ACKNOWLEDGMENT

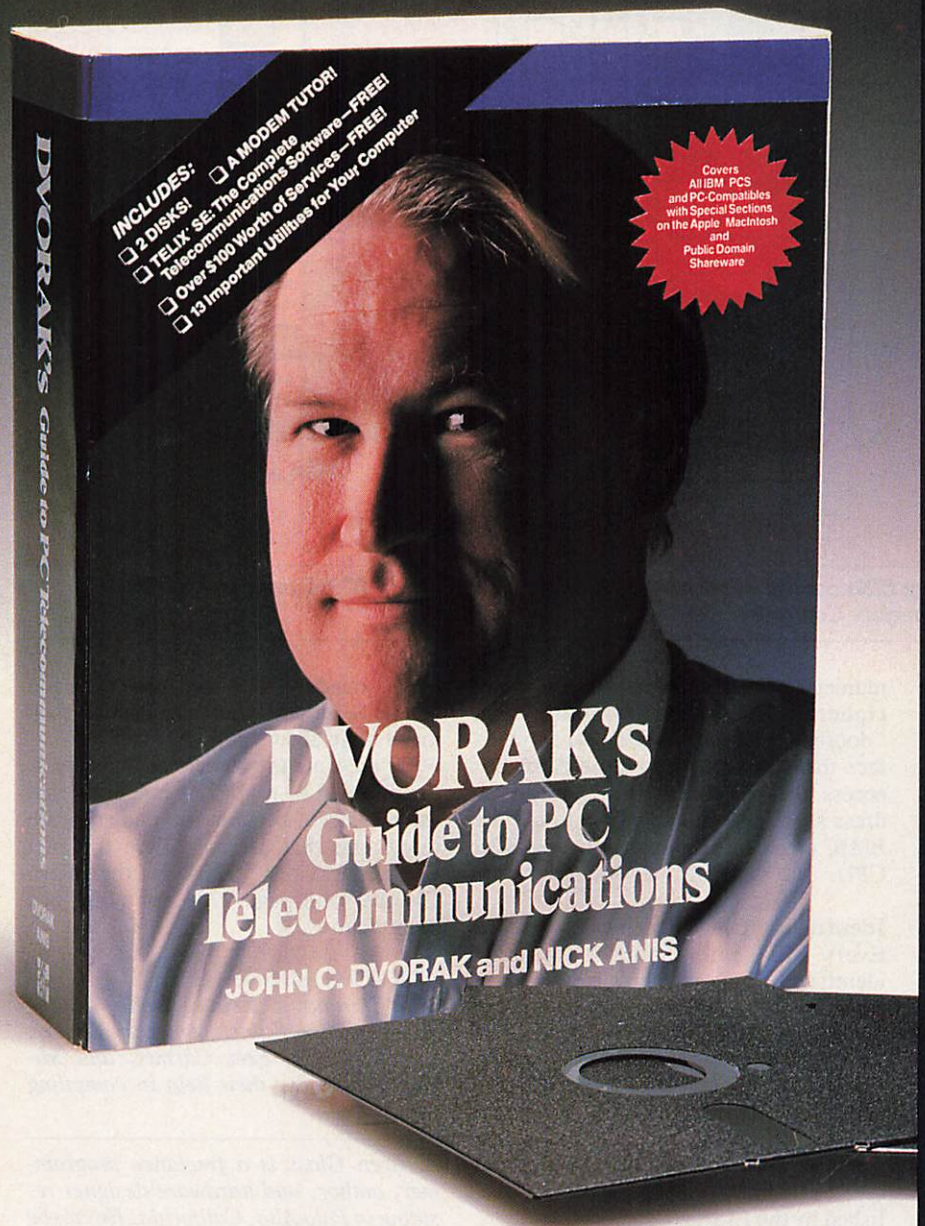
Many thanks to Kristin Bailey, Steve Spangler, Rob Kubick, Amaresh Kumar, Chris McAfee, Erez Carmel, and Michael Slater for their help in compiling this article.

L. Brett Glass is a freelance programmer, author, and hardware designer residing in Palo Alto, California. He can be reached on BIX as "glass."

Your questions and comments are welcome. Write to: Editor, BYTE, One Phoenix Mill Lane, Peterborough, NH 03458.

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Part 2



TWO TIN CANS AND SOME STRING

The investigation of network interfaces continues, this time with the popular NetBIOS

Whether you've got a Macintosh, an IBM PC, a Unix system, or whatever, there's a slot or a connector somewhere on your machine begging to be hooked into a network. The begging has probably gotten louder—some networks are down to just a couple hundred dollars per connection. Soon, you may find yourself capitulating; you'll be bent over your machine, screwing a coaxial umbilical into an adapter card. There, you're jacked in. Now what?

In last month's installment, I described a simple file transfer application as a means of exploring the capabilities of two popular network systems: AppleTalk and NetBIOS. I began with AppleTalk, so now it's time for NetBIOS to show its stuff. I should warn you now, I'll frequently refer to Part 1 to draw parallels between the mechanics of NetBIOS and those of AppleTalk. You may want to keep your October issue on hand.

I spent a good portion of last month's article discussing the *layers* of functions of which AppleTalk is composed. It's important to be clear about layers, since the AppleTalk Transaction Protocol, which I used in my program last month, resides one floor down from NetBIOS. Specifically, ATP operates at the transaction layer, while NetBIOS operates at the session layer.

After reading this two-part series, you might conclude that NetBIOS has superior capabilities and that ATP should thus be scorned as inferior by comparison. That would be a mistake, for the simple reason that ATP is a transaction-layer protocol and is not meant to include functions from the session layer. For many applications, the transaction-handling functions of AppleTalk are more than sufficient for the task. AppleTalk does have a set of session-layer functions that I intend to cover in a future column.

As in AppleTalk, the upper-layer functions of NetBIOS call on functions in the lower layers. Unlike AppleTalk, most NetBIOS installations hide the lower layers from applications. For simplicity, I'll split the layers of NetBIOS into upper and lower. This division is of my own doing, and it's merely to group the layers into manageable portions.

Upper Layers

The NetBIOS Session Management Protocol (SMP) handles sessions (which I'll describe in a moment) between named processes on the network. A named process is similar to AppleTalk's socket client: a program that has made itself accessible to other programs on the network via a network-visible name.

The Name Management Protocol is the counterpart to AppleTalk's Name Binding Protocol (NBP). NMP allows the user to create unique, symbolic names that are made visible on the network. On AppleTalk, a name is associated with a socket client; in NetBIOS, a name is associated with one end of a session.

AppleTalk names are also more versatile than NetBIOS names. AppleTalk names consist of three fields: zone, object, and type. These fields could be used as filters, or as a mechanism for dividing a physical network into logical subnets (departments). NetBIOS names are flat strings of 16 characters, and NetBIOS provides no filtering or partitioning. For example, you can't perform wild-card searches to locate all the names on the network beginning with "Print." Application programs have to add their own wild card–matching capabilities.

The NetBIOS User Datagram Protocol is analogous to AppleTalk's Datagram Delivery Protocol. As with AppleTalk's DDP, UDP manages packet transmission from source to destination with no guarantee of delivery. UDP packets can be up to 512 bytes long. There are some advantages to using DDP. Its usage does not require you to first set up a session; you just pick the name you want to send the datagram to and fire away. Also, you can use DDP to send broadcast datagrams, which are sent to all names on the network. The file transfer program I'll present makes no use of UDP functions; for an application of datagrams, see "Understanding NetBIOS" in the January BYTE.

Finally, the NetBIOS Diagnostic and Monitoring Protocol has no real counterpart in AppleTalk (except, perhaps, the AppleTalk Echo Protocol, AEP). DMP commands allow a program to acquire status information from local as well as remote nodes on the network. You can also obtain traffic information, along with data such as the number of cyclic-redundancy-check errors that have occurred, the number of collisions that have occurred, and more.

Lower Layers

The lower layers are less clear than the upper and depend largely on the hardware in use. The transport layer on the PC Network uses IBM's proprietary Reliable Stream Protocol. Other network systems use the Transmission Control Protocol. You can find the Datagram Transport Protocol at the transport layer, as well; UDP and DMP use it heavily.

Beneath the transport layer resides the network layer, which often becomes confused with the layer beneath it. IBM PC networks use the Packet Transfer Protocol, which more or less calls the Link Access Protocol directly. Other vendors may use XNS (Xerox Network Systems), TCP/IP, or—in the case of Novell's NetBIOS emulation—IPX.

Finally, the physical layer is inhabited

continued

by a diversity of creatures. Here you'll find token rings, Ethernets, or even RS-232 connections.

As confusing as all this seems, the reality is that unless you're in the business of actually building network hardware, you usually don't have to work in the catacombs of the lower layers. I'll focus on the upper layers (the SMP and NMP), since this month's program deals with them.

Transactions and Sessions

Aside from the fact that NetBIOS and AppleTalk run on completely dissimilar machines, the main difference in the kinds of commands available under these two network systems can be traced to the difference between a transaction and a session. In last month's column, I went into some detail concerning an AppleTalk transaction: Communication between network entities in ATP takes place as a series of request/response cycles. The requester says "Give me some data," and the responder replies with "Here it is." The relationship between applications on ATP does not go beyond this request/response exchange. This is no surprise, since ATP is, after all, a transaction-layer protocol.

Applications under NetBIOS, however, establish a session between one another. A session is like a telephone call. First, both parties must make themselves visible on the network using the ADD NAME command—analogous to providing all phone system subscribers with a universal phone book. Next, one party calls the other using the NetBIOS CALL command. The second party answers using the LISTEN command. Once they have established the session, both sides can talk or listen using the commands SEND and RECEIVE. In fact, both sides can simultaneously send and receive; hence, NetBIOS is said to support full-duplex operation.

NetBIOS, then, is a step up from the transaction layer of ATP. A NetBIOS session can contain numerous request/response transactions. Furthermore, either side can play the role of requester and responder. The dialog continues until one (or, preferably, both) of the parties issues the HANG UP command and terminates the connection.

Table 1: *Format of the NetBIOS control block (NCB). In some literature, you may see this referred to as the message control block (MCB).*

FIELDS IN THE NETBIOS CONTROL BLOCK

Field name	Description
COMMAND	(1 byte) The command field, which tells NetBIOS which function to execute. If the high bit is set, the command is a "no-wait" command (see text).
RETCODE	(1 byte) Returned by NetBIOS when the command completes, this field is 0 if all went well. Otherwise, this field holds an error code.
SESSION NUMBER	(1 byte) When a CALL or LISTEN command completes, this field holds the number of the established session. If you issue a SEND or RECEIVE command, you must load this field with the appropriate session number.
NAME NUMBER	(1 byte) When an ADD NAME or ADD GROUP NAME command completes, this field holds the number associated with that name; used with UDP commands.
BUFFER	(4 bytes) For SEND commands, this field holds the offset and segment of the buffer holding the message to be transmitted. For RECEIVE commands, this field points to the buffer where incoming data is to be stored.
LENGTH	(2 bytes) The number of bytes in the buffer pointed to by the BUFFER field.
CALL NAME	(16 characters) Used by the CALL and LISTEN commands to hold the name of the remote station that will become your session partner.
NAME	(16 characters) Holds the local name (i.e., holds your name) for ADD NAME and DELETE NAME commands.
RECEIVE TIMEOUT	(1 byte) Indicates the time-out in ½-second increments for RECEIVE commands.
SEND TIMEOUT	(1 byte) Indicates the time-out in ½-second increments for SEND commands.
POST	(4 bytes) This field points to a post routine, which NetBIOS executes after completing a no-wait command; should be set to 0 if not used.
ADAPTER NUMBER	(1 byte) Network-adapter number; indicates which network adapter card the command should be issued to.
COMMAND COMPLETE	(1 byte) A value of 255 in this field indicates that the command specified by the NCB has not completed. NetBIOS sets this field to 0 when the command is finished.
RESERVED	(14 bytes) Reserved by NetBIOS.

Talky-Talk

You issue commands to NetBIOS via a data structure known as the NetBIOS control block (see table 1 for a description of the NCB's fields). The NCB's function is roughly equivalent to that of AppleTalk's parameter block, although this is more coincidental than intentional. Each NCB is a message sent to NetBIOS describing a command that the calling application needs carried out. The NCB remains the property of NetBIOS while the command is in progress. (I'll present NetBIOS commands in uppercase.)

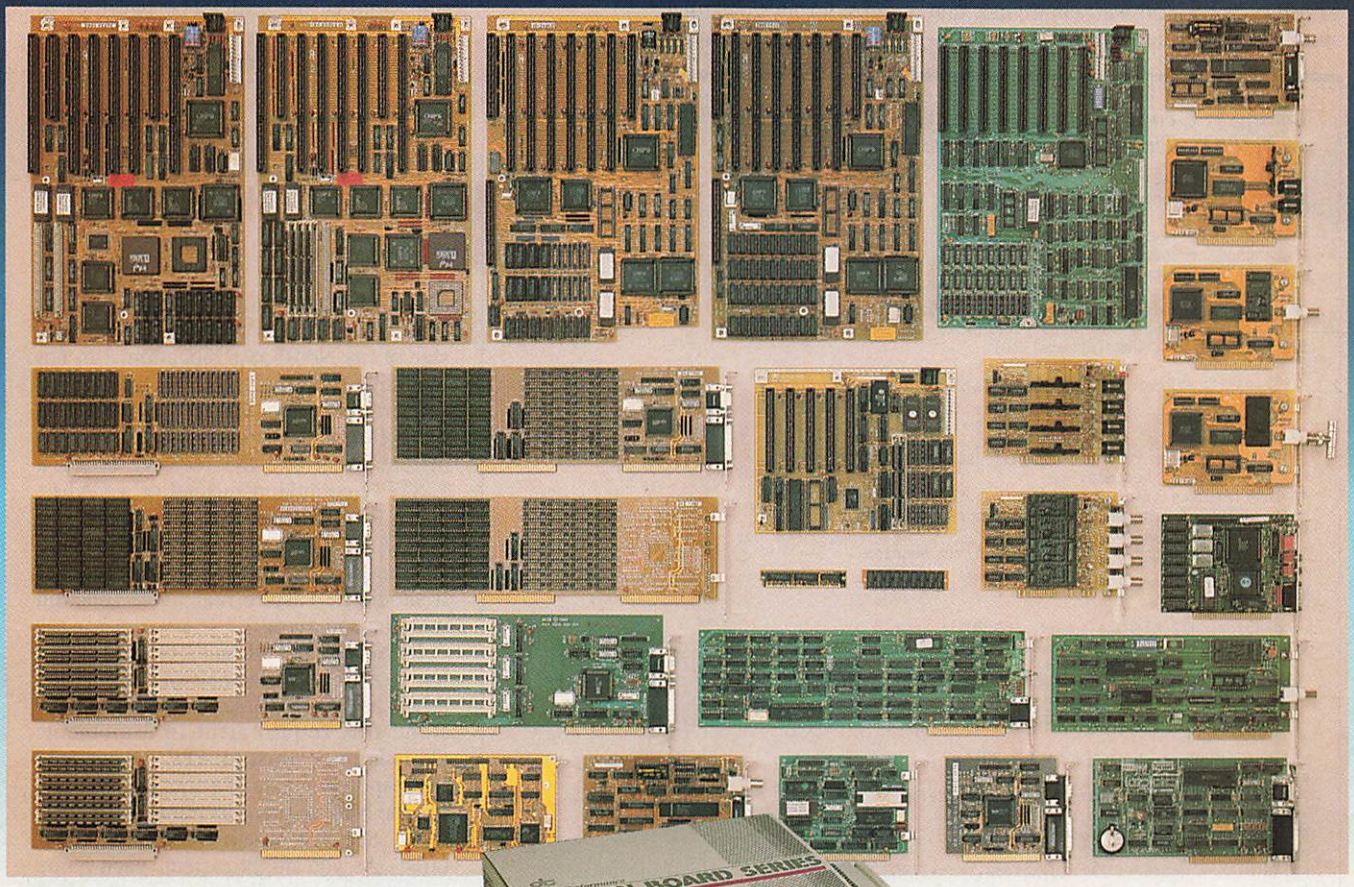
Ordinarily, conjuring up NetBIOS involves loading up the fields of the NCB with the information appropriate for whichever command you want NetBIOS to perform, executing an INT 5CH, and examining the RETCODE field of the NCB when NetBIOS returns. (If you're in assembly language, the AL register mirrors the contents of the RETCODE field.) NetBIOS commands issued in this fashion are referred to as "wait" commands; your program waits for the command to complete before proceeding—not the best use of the computer's time.

If you set the high bit of the NCB's COMMAND field to a 1, that command becomes a "no-wait" version. NetBIOS will return immediately and multitask with your application. Your program can be performing computations while NetBIOS twiddles its thumbs, waiting for

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response packets and such.

If you've pointed the POST field to an interrupt-handling routine (i.e., one that concludes with an IRET instruction), NetBIOS will call that routine when the command has completed. The post routine can examine the RETCODE field and take appropriate action. Alternatively, you can clear the POST field, call NetBIOS using a no-wait command, and simply monitor the COMMAND COMPLETE field. NetBIOS will set COMMAND COMPLETE to 0 when the job is done. (Sharp-eyed readers will recognize these two ways of handling no-wait commands as being interrupt-driven and polled techniques, respectively.) The sample program I've written this month completely wimps out and uses nothing but the wait version of commands. I apologize for my cowardice.

To be fair to AppleTalk, most of its commands can be executed in no-wait fashion, as well. AppleTalk refers to no-wait commands as *asynchronous*. Calling a routine asynchronously causes an immediate return to your program, whereupon AppleTalk does its work in the background. (For assembly language programmers, you signify an asynchronous command by setting bit 10 of the trap word of the call.) The parallels to NetBIOS go further: You can either poll the AppleTalk command's parameter block, looking at the `ioResult` field (typically at offset 16 in the parameter block) and waiting for it to change from 1, or you can specify a *completion routine* whose job is identical to NetBIOS's post routine.

Listing 1: *C code fragment for the operations used to establish a file-send on NetBIOS. The receive code is very similar.*

```
/* Open the file.*/
filehand=getfilename(argv[3]);

/* Delete your session name to make sure it's not
** hanging around. */
NBios_DelName(myname);

/* Add your session name to the name table.
** Variable 'myname' contains your local name. */
if((rcod=NBios_AddName(myname))<0)
{
   printf(">>>Error adding name: %d\n",rcod);
   exit(0);
}

/* Open a session for the transmit using the CALL command.
** Timeout is 30 seconds.
** This routine tries indefinitely...it keeps trying
** in spite of command time-out (error 5) as well as
** a "no answer" error (error 20).
** Variable 'hisname' is the name of our session
** partner. */
do
{
rcod=NBios_Call(hisname,myname,200,200);
if ((rcod<0) && (rcod != -5) && (rcod != -20))
   {
   printf(">>>Error calling session: %d\n",0-rcod);
   exit(0);
   }
}
while ( (rcod == -5) || (rcod == -20));
sessnum=rcod;
/* Read file, transmitting 1K-byte blocks.
** Xblock is the message buffer. */
Xblock.Text[0]='D'; /* Data block */
count=0;
while(blen = getrec(filehand,Xblock.Text+1,BLOCKSIZE))
{
   Xblock.TextLength=blen+1;
   printf("Sending..%d\n",count++);
   if(rcod=NBios_SessionSend(sessnum,&Xblock))
   {  printf(">>>Send error: %d\n",rcod);
      NBios_Hangup(sessnum);
      exit(0);
   }
}

/* Send EOF block. */
Xblock.Text[0]='E';
Xblock.TextLength=1;
if(rcod=NBios_SessionSend(sessnum,&Xblock))
{   printf(">>>Send error: %d\n",rcod);
   NBios_Hangup(sessnum);
   exit(0);
}

/* Hang up the session. */
NBios_Hangup(sessnum);

/* Delete your name. */
if(rcod=NBios_DelName(myname))
{   printf(">>>Error deleting name: %d\n",rcod);
   exit(0);
}
/* Transmit went ok. */
printf("DONE!!\n");
close(filehand);
exit(0);
```

The Real Stuff

The code fragment in listing 1 shows most of the source code for the sending side of my NetBIOS application. I'm not including the receiver's source code for the simple reason that it is virtually a twin of the source in listing 1. The major difference is that the receiver issues a LISTEN command instead of a CALL, and a RECEIVE command instead of a SEND. (You'll notice functions in listing 1 corresponding to NetBIOS commands. It should be easy to match the function with the command.)

In NetBIOS, both ends of the session log a name on the network using the ADD NAME command. You'll understand this requirement in a moment. (This is in contrast to ATP, where only the responding side of a transaction must use the NBP to place its name on the network. See last month's column for details.) As you might expect, each name must be unique. The examples that I've provided allow you to define the names as command-line arguments. This permits numerous versions of the same program to run simultaneously on the network.

When a program calls ADD NAME, NetBIOS's first job is to make certain that no other program has laid claim to the name. It does this by broadcasting a name claim packet across the network. Actually, it broadcasts the packet several times as a fail-safe measure. If no other station contests the name claim, NetBIOS adds the name to its local name table. As with AppleTalk, a single station on the network can be known by several names—aliases, if you will. A typical NetBIOS installation can handle up to 12 names per station.

Once each side has added its name to the network's name table, it's time to

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GLOSSARY

A brief list of the NetBIOS commands mentioned in the article. Note that there are many more NetBIOS commands available than are presented here.

ADD NAME Requires a 16-character name in the NAME field. This name is added to your local name table and is associated with your station. NetBIOS verifies that the name is complete.

CALL Requires a remote user's name in the CALL NAME field; attempts to establish a session and assumes the other party is executing a LISTEN command with your local name in his CALL NAME field.

DELETE NAME Deletes any local names added by ADD NAME.

LISTEN The other end of the CALL command.

RECEIVE The catcher's mitt for a SEND command.

SEND Requires the session number returned by a successful CALL or RECEIVE; also requires a pointer to a buffer. The contents of the buffer are transmitted to the session partner.

establish the session. Harking back to the telephone call analogy, one station—the computer sending the file in my application—issues a CALL. This command requires as one of its parameters the name of the station being called (variable `hisname` in the listing). The system at the other end of the session—the computer receiving the file—issues a LISTEN command. This command takes as a parameter the name of the station to listen to. When the station listening "picks up" on the station calling, a session has begun. (You see why *both* stations need to use the ADD NAME command?)

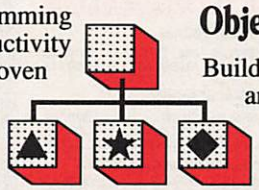
Both the CALL and LISTEN commands return a session number. This 8-bit number is similar in function to a file handle. As you call NetBIOS commands, you indicate which session partner the command is meant for by using the session number. This is more than just a convenience; a single computer can have several simultaneous sessions active. When one command has completed, your program has to figure out which one completed in order to know what action to take next. With no session number, your program would have to scan tables of 16-character names for the one matching the completed NCB. It boils down to this: 8 bits are easier to carry from routine to routine than a 16-character name.

You send a message to your session partner with the SEND MESSAGE command. This command takes as input the session number and a pointer to the buffer holding your message. A message can be up to 64K bytes long. The program on the receiving end calls the RECEIVE MESSAGE command to accept the message. Again, this will require a session

continued on page 482

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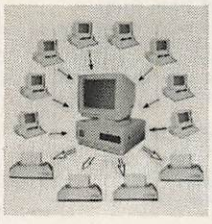
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7400

Part No.	1-9	10+	Part No.	1-9	10+
7400	.29	.19	7474	.39	.29
7402	.29	.19	7475	.49	.39
7404	.29	.19	7476	.45	.35
7405	.35	.25	7483	.59	.49
7406	.39	.29	7485	.65	.55
7407	.39	.29	7486	.45	.35
7408	.35	.25	7489	2.25	2.15
7410	.29	.19	7490	.49	.39
7411	.35	.25	7493	.45	.35
7414	.49	.39	7495	.59	.49
7416	.35	.25	74107	.29	.19
7417	.35	.25	74121	.39	.29
7420	.29	.19	74123	.49	.39
7427	.29	.19	74125	.49	.39
7430	.29	.19	74147	1.99	1.89
7432	.39	.29	74150	1.35	1.25
7438	.39	.29	74151	.39	.29
7442	.49	.39	74154	1.35	1.25
7445	.75	.65	74161	.69	.59
7446	.89	.79	74173	.79	.69
7447	.89	.79	74174	.59	.49
7448	1.95	1.85	74175	.59	.49
7473	.39	.29	74193	.79	.69

74LS

74LS00	.26	.16	74LS139	.49	.39
74LS02	.28	.18	74LS151	.49	.39
74LS03	.28	.18	74LS153	.49	.39
74LS04	.28	.18	74LS154	1.29	1.19
74LS05	.28	.18	74LS157	.45	.35
74LS06	.59	.49	74LS161	.49	.39
74LS07	.59	.49	74LS163	.49	.39
74LS08	.28	.18	74LS164	.59	.49
74LS09	.28	.18	74LS165	.75	.65
74LS10	.26	.16	74LS166	.89	.79
74LS11	.29	.19	74LS173	.45	.35
74LS14	.49	.39	74LS174	.39	.29
74LS20	.28	.18	74LS175	.39	.29
74LS21	.29	.19	74LS191	.59	.49
74LS27	.35	.25	74LS192	.69	.59
74LS30	.28	.18	74LS193	.69	.59
74LS32	.28	.18	74LS194	.69	.59
74LS38	.35	.25	74LS221	.69	.59
74LS42	.49	.39	74LS240	.59	.49
74LS47	.85	.75	74LS241	.59	.49
74LS73	.39	.29	74LS244	.59	.49
74LS74	.35	.25	74LS245	.79	.69
74LS75	.39	.29	74LS257	.49	.39
74LS76	.39	.29	74LS259	.99	.89
74LS83	.55	.45	74LS273	.89	.79
74LS85	.55	.45	74LS279	.49	.39
74LS86	.29	.19	74LS367	.49	.39
74LS90	.49	.39	74LS373	.79	.69
74LS93	.49	.39	74LS374	.79	.69
74LS123	.49	.39	74LS393	.89	.79
74LS125	.49	.39	74LS541	1.29	1.19
74LS132	.49	.39	74LS590	5.95	5.85
74LS138	.49	.39	74LS688	2.39	2.29

74S/PROMS*

74S00	.25	74S188*	1.49
74S04	.25	74S189	1.49
74S32	.25	74S240	1.39
74S74	.25	74S244	.99
74S112	.25	74S287*	1.49
74S124	1.25	74S288*	1.49
74S138	.49	74S373	.99
74S153	.29	74S374	.99
74S163	.75	74S387*	1.29
74S174	.29	74S472*	2.95
74S175	.39	74S571*	2.49

CD-CMOS

CD4001	.19	CD4051	.59
CD4002	.19	CD4052	.59
CD4007	.19	CD4053	.59
CD4011	.19	CD4060	.65
CD4012	.25	CD4066	.29
CD4013	.29	CD4069	.25
CD4015	.29	CD4070	.29
CD4016	.29	CD4071	.19
CD4017	.49	CD4072	.19
CD4018	.49	CD4073	.19
CD4020	.59	CD4081	.19
CD4021	.49	CD4093	.35
CD4024	.45	CD4094	.89
CD4027	.35	CD4503	.39
CD4028	.49	CD4511	.59
CD4029	.69	CD4518	.75
CD4030	.35	CD4520	.69
CD4040	.65	CD4522	.75
CD4042	.49	CD4528	.69
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CD4046	.65	CD4543	.79
CD4047	.65	CD4584	.49
CD4049	.29	CD4585	.69
CD4050	.29		

EEPROMS

2816A	2048x8 350ns (9V-15V) 5V **Read/Write**	5.25
2816A-25	2048x8 250ns (9V-15V) 5V **Read/Write**	5.49
2817A	2048x8 350ns 5V **Read/Write**	6.95
2864A	8192x8 250ns 5V **Read/Write** (Pin 1, No R/B)	10.95
2864A-30	8192x8 300ns 5V **Read/Write** (Pin 1, No R/B)	9.95
2865A	8192x8 250ns 5V **Read/Write**	10.95
52B13	2048x8 350ns (21V) 5V Read Only	1.49

MICROPROCESSOR COMPONENTS

Z80, Z80A, Z80B, SERIES

Part No.	Price
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Z80A	1.29
Z80A-CTC	1.65
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Z80A-PIO	1.89
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Z80B	2.75
Z80B-CTC	3.95
Z80B-PIO	3.95
Z8681B1	4.95

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80C31	8.95
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8039	1.59
8052AHBASIC	24.95
8080A	1.95
8085A	1.95
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8086	3.95
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8087-2 (8MHz)	129.95
8088 (5MHz)	4.95
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Part No.	Price
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81C55	4.25
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82C11	6.95
8212	1.99
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8237-5	4.25
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82C53-5	3.95
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82C55A-5	4.49
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8755	13.95
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80287-3 (5MHz)	109.95
80287-8 (8MHz)	209.95
80287-10 (10MHz)	239.95
80386-16 PGA	259.95
80387-16 (16MHz)	349.95
80387-20 (20MHz)	399.95
80387-25 (25MHz)	499.95
82284 (8MHz)	5.49
82288 (8MHz)	6.95

DATA ACQUISITION

ADC0804LCN	2.99
ADC0808CCN	5.95
ADC0809CCN	3.69
ADC1205CCJ-1	20.95
DAC0808LCN	1.75
AY-3-1015D	4.95
AY-5-1013A	2.95

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Part No.	Function		Price
2016-12	2048x8	120ns	2.95
2102	1024x1	350ns	.89
2112	256x4	450ns MOS	2.49
2114N	1024x4	450ns	.99
2114N-2L	1024x4	200ns Low Power	1.49
21C14	1024x4	200ns (CMOS)	.49
5101	256x4	450ns (CMOS)	1.95
6116P-1	2048x8	100ns (16K) CMOS	3.19
6116P-3	2048x8	150ns (16K) CMOS	2.79
6116LP-1	2048x8	100ns (16K) LP CMOS	3.59
6116LP-3	2048x8	150ns (16K) LP CMOS	3.09
6264P-10	8192x8	100ns (64K) CMOS	6.75
6264P-15	8192x8	150ns (64K) CMOS	6.29
6264LP-10	8192x8	100ns (64K) LP CMOS	6.95
6264LP-12	8192x8	120ns (64K) LP CMOS	6.75
6264LP-15	8192x8	150ns (64K) LP CMOS	6.49
6514	1024x4	350ns CMOS	3.25
43256-10L	32,768x8	100ns (256K) Low Power	15.95
43256-15L	32,768x8	150ns (256K) Low Power	14.95
62256LP-10	32,768x8	100ns (256K) LP CMOS	16.95
62256LP-12	32,768x8	120ns (256K) LP CMOS	16.25
62256LP-15	32,768x8	150ns (256K) LP CMOS	15.95

DYNAMIC RAMS/MODULES

41256A9A-10	262,144x9	100ns 256x9 SIP (Has Leads)	49.95
41256A9B-10	262,144x9	100ns 256x9 SIM	59.95
421000A9A-10	1,048,576x9	100ns 1MEGx9 SIP (Has Leads)	159.95
421000A9B-10	1,048,576x9	100ns 1MEGx9 SIM	159.95
421000A9A-80	1,048,576x9	80ns 1MEGx9 SIP (Has Leads)	169.95
421000A9B-80	1,048,576x9	80ns 1MEGx9 SIM	169.95
TMS4416-12	16,384x4	120ns	5.95
TMS4416-15	16,384x4	150ns	5.49
4116-15	16,384x1	150ns (MM5290N-2)	1.09
4128-15	131,072x1	150ns (Piggyback)	4.49
4164-100	65,536x1	100ns	2.75
4164-120	65,536x1	120ns	2.39
4164-150	65,536x1	150ns	2.15
41256-60	262,144x1	60ns	6.95
41256-80	262,144x1	80ns	5.75
41256-100	262,144x1	100ns	3.95
41256-120	262,144x1	120ns	3.69
41256-150	262,144x1	150ns	3.25
41264-12	64Kx4	120ns Video RAM	10.95
41464-10	65,536x4	100ns	4.95
41464-12	65,536x4	120ns	4.49
41464-15	65,536x4	150ns	4.25
51258-10	262,144x1	100ns Static Column	8.95
511000P-10	1,048,576x1	100ns (1 Meg)	12.95
511000P-80	1,048,576x1	80ns (1 Meg)	13.95
514256P-10	262,144x4	100ns (1 Meg)	14.49
514258-10	262,144x4	100ns Static Column	26.95

EPROMS

TMS2516	2048x8	450ns (25V)	4.95
TMS2532	4096x8	450ns (25V)	5.95
TMS2532A	4096x8	450ns (12.5V)	3.25
TMS2564	8192x8	450ns (25V)	6.95
TMS2716	2048x8	450ns (-5V, +5V, +12V)	6.49
1702A	256x8	2K (1µs)	4.25
2708	1024x8	450ns	6.95
2716	2048x8	450ns (25V)	3.49
2716-1	2048x8	350ns (25V)	3.95
27C16	2048x8	450ns (25V) CMOS	4.25
2732	4096x8	450ns (25V)	3.95
2732A-20	4096x8	200ns (21V)	3.95
2732A-25	4096x8	250ns (21V)	3.75
27C32	4096x8	450ns (25V) CMOS	4.25
2764-25	8192x8	250ns (21V)	3.95
2764A-20	8192x8	200ns (12.5V)	4.19
2764A-25	8192x8	250ns (12.5V)	3.49
27C64-15	8192x8	150ns (12.5V) CMOS	4.95
27128-20	16,384x8	200ns (21V)	5.95
27128-25	16,384x8	250ns (21V)	5.25
27128A-15	16,384x8	150ns (12.5V)	6.95
27128A-20	16,384x8	200ns (12.5V)	4.75
27C128-25	16,384x8	250ns (21V) CMOS	5.95
27256-15	32,768x8	150ns (12.5V)	8.49
27256-20	32,768x8	200ns (12.5V)	5.49
27256-25	32,768x8	250ns (12.5V)	4.95
27C256-15	32,768x8	150ns (12.5V) CMOS	7.25
27C256-25	32,768x8	250ns (12.5V) CMOS	5.49
27512-25	65,536x8	250ns (12.5V)	7.25
27C512-15	65,536x8	150ns (12.5V) CMOS	9.95
27C512-25	65,536x8	250ns (12.5V) CMOS	7.49
27C010-15	131,072x8	150ns (12.5V) CMOS (1 Meg)	19.95
68764	8192x8	64K 450ns (25V) (Chip Enable)	14.95
68766-35	8192x8	64K 350ns (25V) (Output Enable)	15.95

6500/6800 68000 Series

Part No.	Price
6402	3.75
6502	2.19
6502A	2.59
65C02 (CMOS)	6.95
6520	1.59
6522	2.95
65C22	4.25
6532	4.95
6551	2.69
65C802 (CMOS)	15.95
6800	1.75
6802	2.95
6808	2.49
6810	1.25
6820	2.75
6821	1.75
68B21	2.25
6840	3.49
6845	2.75
6850	1.75
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MC68000L8	9.95
MC68000L10	11.95
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MC68701	19.95
MC68705P3S	15.95
MC68705U3S	17.95
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8564	2.95
8566	6.95
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901225-01	15.95
901226-01	15.95
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901227-03	15.95
901229-05	15.95
901460-03	1.95
901486-06	2.95

*No specs available
**Note: 82S100PLA = U17 (C-64)

74C/CMOS

74C00	.25	74C174	.39
74C02	.25	74C175	.39
74C04	.25	74C192	.99
74C08	.25	74C194	.49
74C10	.19	74C221	1.79
74C14	.49	74C240	.99
74C32	.45	74C244	1.49
74C74	.49	74C373	1.49
74C85	1.29	74C374	1.49
74C86	.29	74C911	5.95
74C89	2.95	74C912	7.95
74C90	.99	74C915	1.19
74C151	1.75	74C917	3.95
74C154	2.95	74C920	3.95
74C157	1.49	74C921	3.95
74C160	.49	74C922	3.95
74C161	.49	74C923	3.95
74C162	.49	74C925	4.95
74C173	.49	74C926	5.95

MISC. COMPONENTS

TANTALUM CAPACITORS

TM.1	.1µf @ 35V	.19	TM4.7	4.7µf @ 35V	.45
TM1	1µf @ 35V	.19	TM6.8	6.8µf @ 35V	.59
TM2.2	2.2µf @ 35V	.25	TM10	10µf @ 35V	.69

POTENTIOMETERS

Values available (insert ohms into space marked "XX"): 500Ω, 1K, 2K, 5K, 10K, 20K, 50K, 100K, 200K, 1MEG

43PXX 3/4 Watt,15Turn .99 | **63PXX** 1/2 Watt, 1Turn .89

TRANSISTORS AND DIODES

PN2222	.13	PN2907	.13	1N4004	.10
2N2222A	.29	2N4401	.15	1N4148	.07
2N3055	.69	1N270	.25	1N4735	.25
2N3904	.12	1N751	.15	C106B1	.49

SWITCHES

JMT123	SPDT, On-On	1.25	206-8	SPST, 16-pin DIP	1.19
MPC121	SPDT, On-Off-On	1.25	MS102	SPST, Momentary	.39

D-SUB CONNECTORS

DB25P	Male, 25-pin .69	DB25S	Female, 25-pin .75

LEDS

XC556R	T1¾, Red .13	XC556Y	T1¾, Yellow .17
XC556G	T1¾, Green .17		

IC SOCKETS

Low Profile		Wire Wrap (Gold) Level #2	
8LP	.11	8WW	.49
14LP	.12	14WW	.65
16LP	.13	16WW	.69
24LP	.21	24WW	1.19
28LP	.23	28WW	1.39
40LP	.29	40WW	1.89

Soldertail Standard (Gold & Tin) & Header Plug Sockets Also Available

74HC HI-SPEED CMOS

Part No.	Price	Part No.	Price
74HC00	.19	74HC175	.59
74HC02	.19	74HC221	.89
74HC04	.19	74HC240	.69
74HC08	.19	74HC244	.79
74HC10	.19	74HC245	.79
74HC14	.29	74HC253	.49
74HC30	.25	74HC259	.49
74HC32	.25	74HC273	.49
74HC74	.29	74HC373	.69
74HC75	.35	74HC374	.69
74HC76	.35	74HC595	1.29
74HC85	.55	74HC688	1.49
74HC86	.29	74HC943	6.95
74HC123	.59	74HC4040	.79
74HC125	.49	74HC4049	.29
74HC132	.49	74HC4050	.29
74HC138	.45	74HC4060	.69
74HC139	.39	74HC4511	.99
74HC154	1.49	74HC4514	1.79
74HC163	.39	74HC4538	1.19
74HC174	.59	74HC4543	1.19

74HCT-CMOS TTL

74HCT00	.17	74HCT139	.39
74HCT02	.17	74HCT157	.29
74HCT04	.19	74HCT174	.29
74HCT08	.17	74HCT175	.29
74HCT14	.29	74HCT240	.69
74HCT32	.19	74HCT244	.49
74HCT74	.29	74HCT245	.49
74HCT86	.25	74HCT373	.49
74HCT138	.39	74HCT374	.39

LINEAR

Part No.	1-9	10+	Part No.	1-9	10+
TL071CP	.69	.59	DS14C88N	1.19	1.09
TL072CP	.79	.69	LM1489N	.49	.45
TL074CN	.99	.89	DS14C89N	1.19	1.09
TL081CP	.59	.49	LM1496N	.69	.59
TL082CP	.59	.49	LM1871N	1.95	1.75
TL084CN	.99	.89	LM1872N	1.95	1.75
LM307N	.45	.39	ULN2003A	.79	.69
LM308N	.65	.59	ULN2004A	.79	.69
LM309K	1.49	1.25	26LS29	2.95	2.75
LM310N	1.49	1.25	26LS31	1.19	.99
LM311N	.49	.39	26LS32	1.19	.99
LM317T	.69	.59	26LS33	1.75	1.49
LM318N	1.09	.99	ULN2803A	1.19	.99
LM319N	1.29	1.19	LM2901N	.39	.29
LM323K	3.49	3.25	LM2907N	1.29	1.19
LM324N	.39	.35	LM2917N (8 pin)	1.75	1.49
LM335Z	1.49	1.25	MC3470P	1.29	1.19
LM336Z	1.09	.99	MC3479P	3.95	3.75
LM337T	1.29	1.09	MC3486P	1.29	1.19
LM338K	4.49	4.25	MC3487P	1.29	1.19
LM339N	.49	.39	LM3900N	.49	.45
LF347N	1.49	1.25	LM3905N	1.29	1.19
LM348N	.69	.59	LM3909N	.89	.79
LF351N	.49	.39	LM3914N	1.95	1.75
LF353N	.59	.49	NE5532	.89	.79
LF356N	.89	.79	NE5534	.89	.79
LF357N	.99	.89	7805K	1.29	1.19
LM358N	.59	.49	7812K	1.29	1.19
LM380N	.89	.79	7815K	1.29	1.19
LM385Z1.2	1.75	1.49	7805T	.49	.45
LM386N-3	.79	.69	7812T	.49	.45
LM393N	.45	.35	7815T	.49	.45
LF398N	1.95	1.75	78L08	.35	.29
LF411CN	.79	.69	7905K	1.49	1.25
LF412CN	1.29	1.19	7905T	.55	.49
NE555V	.35	.29	75113	1.39	1.19
XRL555	.75	.65	75150	1.29	1.19
LM556N	.49	.39	75154	1.29	1.19
LM565N	.99	.89	75174	2.95	2.75
LM566CN	1.29	1.19	75175	2.95	2.75
LM567V	.75	.65	75176	2.25	1.95
LM723CN	.49	.39	75451	.45	.39
LM741CN	.35	.29	75452	.45	.39
LM747CN	.59	.49	75492	.89	.79
LM1458N	.39	.35	MC145406P	2.95	2.75
LM1488N	.49	.45			

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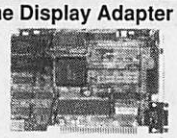
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COMPUTER ACCESSORIES

DFI Handy Scanner and 3 Button Mice for IBM PC/XT/AT

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The HS3000 offers a full 4 inch window at 400dpi resolution. Scan photos, logos, drawings, etc. Can be used with today's most popular applications.

HS3000 Pictured

HS3000	Handy Scanner	**$189.95**
DMS200	200DPI 3-Button Ser. Mouse	**$39.95**
DMS200S	200DPI 3-Button Ser. Mouse with Dr. Halo Software	**$59.95**

IBM Compatible Cases and Power Supplies



JE2011 Pictured



JE1030 Pictured

JE1010	Flip-Top Standard PC/XT Case	**$39.95**
JE1018	Slide Baby AT Case	**$59.95**
JE1030	150 watt PC/XT Power Supply	**$59.95**
JE1032	200 watt Baby AT Power Supply	**$89.95**
JE2011	Vertical Case w/300 watt Pwr. Supply	**$279.95**
JE2014	Flip-Top Baby XT Turbo Case	**$69.95**
JE2019	Flip-Top Baby AT Case	**$69.95**

Datatronics 2400/1200/300 Baud Pocket Size Modems

2400 Baud Pocket-Size Modem...Only $149.95!



2400P Pictured

1200P	1200/300 Baud Pocket Size Modem With ProComm Shareware Software	**$89.95**
2400P	2400/1200/300 Baud Pocket Size Modem With ProComm Shareware Software	**$149.95**

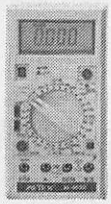
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Metex Digital Multimeters

Metex General Specs:
- Handheld, high accuracy
- AC/DC Voltage, AC/DC Current, Resistance, Diodes, Continuity, Transistor hFE • Manual ranging w/overload protection

M3650/B & M4650 only:
- Also measures frequency and capacitance

M4650 only:
- Data Hold Switch
- 4.5 Digit



M4650 Pictured

M3610	3.5 Digit Multimeter	**$49.95**
M3650	3.5 Digit w/Freq. & Capacitance	**$69.95**
M3650B	Same as M3650 w/Bargraph	**$79.95**
M4650	4.5 Dig. w/Freq., Capacitance and Data Hold Switch	**$99.95**

Jameco 16MHz 80286 NEAT Computer Kit With 2 Megabyte RAM

- *Fully IBM AT Compatible*
- *Free! DR -DOS Disk Operating System Software Included*
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- *Free! WORDSTAR EASY Word Processing Software Included!*
- *2Mb RAM Included, Expandable to 8Mb*
- *8 or 16MHz Operation*
- *AMI BIOS ROMs Included*
- *Flip-Top Case w/200 Watt Power Supply*
- *1.2Mb Disk Drive*
- *18.0 Norton SI Rating*
- *101-Key (Enhanced) Keyboard*

SALE

SAVE $82.85



Shown with VGA Option (not included)
JE2060 Monitor and Adapter Card....**$529.95**
(See Below)

JE3013 16MHz IBM AT Compatible Kit.....**$849.95**

IBM COMPATIBLE DISPLAY MONITORS



TM5156 Pictured

AMBER	12" Amber Monochrome	**$99.95**
HD55H	14" RGB 640x240	**$249.95**
TM5154	EGA 14" 720x350	**$369.95**
JE1059	EGA Monitor & Card	**$459.95**
TM5156	14" VGA 720x480	**$399.95**
TM5157	14" Multiscan 800x600	**$469.95**
JE2060	VGA Monitor & Card	**$529.95**

JAMECO IBM PC/XT/AT COMPATIBLE CARDS

JE1043	360K/720K/1.2Mb/1.44Mb Floppy Disk Controller Card (PC/XT/AT)	**$49.95**
JE1050	Monochrome Graphics Card w/Parallel Printer Port (PC/XT/AT)	**$59.95**
JE1052	Color Graphics Card w/ Parallel Printer Port (PC/XT/AT)	**$49.95**
JE1055	EGA Card w/ 256K Video RAM (PC/XT/AT)	**$139.95**
GC1500	Orchid 8-Bit VGA Card w/256K Video RAM (PC/XT/AT)	**$179.95**
GC1501	Orchid 8/16-Bit VGA Card w/256K Video RAM (PC/XT/AT)	**$299.95**
JE1060	I/O Card w/ Serial, Game, Printer Port & Real Time Clock (PC/XT)	**$59.95**
JE1062	RS232 Serial Half Card (PC/XT/AT)	**$29.95**
JE1065	I/O Card w/ Serial, Game and Parallel Printer Port (AT)	**$59.95**
JE1071	Multi I/O Card w/ Controller & Monochrome Graphics (PC/XT)	**$119.95**
JE1077	Multi I/O Card w/ 360K/720K/1.2Mb/1.44Mb Floppy Controller (AT)	**$74.95**
JE1081	2Mb Expanded or Extended Memory Card (zero-K on-board) (AT)	**$109.95**

SEAGATE HALF-HEIGHT HARD DISK DRIVES

ST225	20Mb Drive only (PC/XT/AT)	**$224.95**
ST225XT	20Mb w/Controller (PC/XT)	**$269.95**
ST225AT	20Mb w/Controller (AT)	**$339.95**
ST238	30Mb Drive only (PC/XT/AT)	**$249.95**
ST238XT	30Mb w/Controller (PC/XT)	**$299.95**
ST238AT	30Mb w/Controller (AT)	**$389.95**
ST251-1	40Mb Fast 28ms (Drive only)	**$469.95**
ST251XT	40Mb w/Controller (PC/XT)	**$419.95**
ST251AT	40Mb w/Controller (AT)	**$489.95**

Your One-Stop Center for Hard Disk Drive Needs!



ST225XT Pictured

Seagate 60Mb, 80Mb &120Mb Hard Disk Drives Also Available!

HARD & HARD/FLOPPY DISK CONTROLLERS

Computer Type	MFM Hard Part No./ Price	RLL Hard Part No./ Price	MFM Hard/Floppy Part No./ Price	RLL Hard/Floppy Part No./ Price
8088 (PC/XT) 3:1 Interleave	XTGEN $79.95	1004A27X $89.95	JE1044 $109.95	-------- --------
80286 (AT)/386 2:1 Interleave	1003VMM1 $129.95	1003VSR1 $149.95	1003VMM2 $149.95	1003VSR2 $169.95
80286 (AT)/386 1:1 Interleave	1006VMM1 $149.95	1006VSR1 $169.95	1006VMM2 $169.95	1006VSR2 $189.95

IBM PC/XT/AT COMPATIBLE 3.5"/5.25" DISK DRIVES

MF353B	3.5" 720Kb (PC/XT/AT)	**$99.95**
356KU	3.5" 1.44Mb (PC/XT/AT)	**$109.95**
JE1020	5.25" 360Kb (PC/XT/AT) Black	**$89.95**
JE1021	5.25" 360Kb (PC/XT/AT) Gray	**$89.95**
JE1022	5.25" 1.2Mb (PC/XT/AT) Gray	**$99.95**

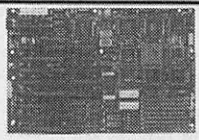


JE1022 Pictured

MOTHERBOARDS

20MHz 386 Only $649.95!

- *All w/ ØK RAM*



JE3520 Pictured

JE1001	Jameco 4.77/8MHz 8088 (PC/XT)	**$89.95**
JE1002	Jameco 4.77/10MHz 8088 (PC/XT)	**$99.95**
JE3005	Jameco Baby 8/12MHz 80286 (AT)	**$199.95**
JE3010	Jameco Baby 8/16MHz 80286 (AT)	**$299.95**
JE3020	AMI Baby 16MHz 80386	**$999.95**
JE3025	AMI Baby 20MHz 80386	**$1199.95**
JE3026	AMI Full-Size 25MHz 80386	**$1899.95**
JE3028	AMI Full-Size 33MHz 80386	**$2599.95**
JE3520	Jameco Baby 20MHz 80386	**$649.95**
JE3525	Jameco Baby 25MHz 80386	**$1299.95**

SUPER SONY SALE

720Kb 3.5" Floppy Drive

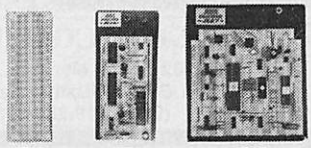


- For use with IBM PC/XT/AT and compatible computers • Double-sided, double density • 135TPI • 160 tracks • Rotation speed: 300rpm • Size: 4"W x 6"D x 1"H

MPF11	720Kb Drive	**$69.95**
SMK	5.25" Mounting Kit	**$14.95**

PROTOTYPING PRODUCTS

Jameco Solderless Breadboards



JE23 JE24 JE27

Part No.	Dim. L" x W"	Contact Points	Binding Posts	Price
JE21	3.25 x 2.125	400	0	$4.95
JE23	6.5 x 2.125	830	0	$6.95
JE24	6.5 x 3.125	1,360	2	$12.95
JE25	6.5 x 4.25	1,660	3	$17.95
JE26	6.875 x 5.75	2,390	4	$22.95
JE27	7.25 x 7.5	3,220	4	$32.95

COMPUTER ACCESSORIES

Jameco IBM PC/XT/AT Compatible Keyboards



JE2017 Pictured

JE2015	84-Key Standard AT Layout	**$59.95**
JE1016	101-Key Enhanced Layout	**$69.95**
JE2016	111-Key Enhanced w/Solar Calculator	**$79.95**
JE2017	104-Key Enhanced w/Trackball	**$99.95**

Colorado Memory 40Mb Tape Back-Up for IBM PC/XT/AT

DJ10	40Mb Tape Back-Up and Tape	**$299.95**
TB40	40Mb Tape Cartridge	**$24.95**

ENGINEERING/DATA BOOKS

21035	Sams TTL Cookbook (88)	**$14.95**
21398	Sams CMOS Cookbook (88)	**$19.95**
22453	Sams Op-Amp Cookbook (88)	**$21.95**
270645	Intel 8-bit Controller Hndbk. (89)	**$19.95**
270646	Intel 16-bit Controller Hndbk. (89)	**$19.95**
270647	Intel 32-bit Controller Hndbk. (89)	**$19.95**
400026	NSC Linear Data Book Vol. 1 (89)	**$19.95**
400015	NSC Linear Data Book Vol. 2 (89)	**$11.95**
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ICM89	1989 IC Master (3 Volume Set)	**$119.95**

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- 80286-12
- 1.2 MB Floppy Drive
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- 101-Key Enhanced Key Board
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- W/Mono Monitor
- 20 MB Hard Disk

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- 20 MB Hard Disk

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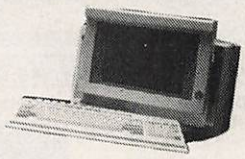
PCI-386-20

- 80386-20
- W/40 MB HD

Mono System **$1795**
VGA **$2295**

GAS PLASMA 286-12 ___ $1895

- 80286-12 CPU
- SI = 13.3
- 3½" FD 1.44 MB
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- LCD Screen (640 X 400)
- I/O Card Parallel/Serial/Game
- 640K RAM



GAS PLASMA 286-20 $1995

- CPU 80286-20
- SI = 23

LCD-286-10 PORTABLE ___ $1349

- 10 MHZ 80286 SI =10.3
- 12 MHZ SI = 13.3 (Option $50.00)
- 16 MHZ SI = 18 (Option $250.00)
- 640K RAM
- LCD Screen 640 X 200
  (Option 640 X 400 $180.00)
- Super Twist & Back Lighting
- 86 Key Board
- External / Parallel / Game
- 1.2 MB Floppy drive
- 20 MB Hard Disk
- 80287 Socket
- 200 W Power Supply
- Side 15 ¾" X 9 ½" X 8"
- 23 LBS

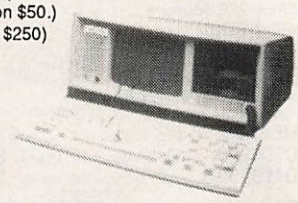


LCD-386-16 ___ $2095
- 80386-16 MHZ
- 40 MB Hard Disk
- 80387 Socket

LCD-386-20 ___ $2195
- 80386-20 MHZ
- 40 MB Hard Disk
- 80387 Socket

CRT-PORTABLE-286 ___ $1249

- Compaq Type
- 80286 (10 MHz or 12 MHz)
- 12 MHz SI = 13.3 (Option $50.)
- 16 MHz SI = 18 (Option $250)
- One 1.2 MB Floppy Drive
- 200 W Power Supply
- TTL Disply 9" Amber
- AT Key Board
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- WA2 HD & FD Controller
- 20 MB Hard Disk



CRT-386-16 $1795
- 80386-16

CRT-386-20 $1895

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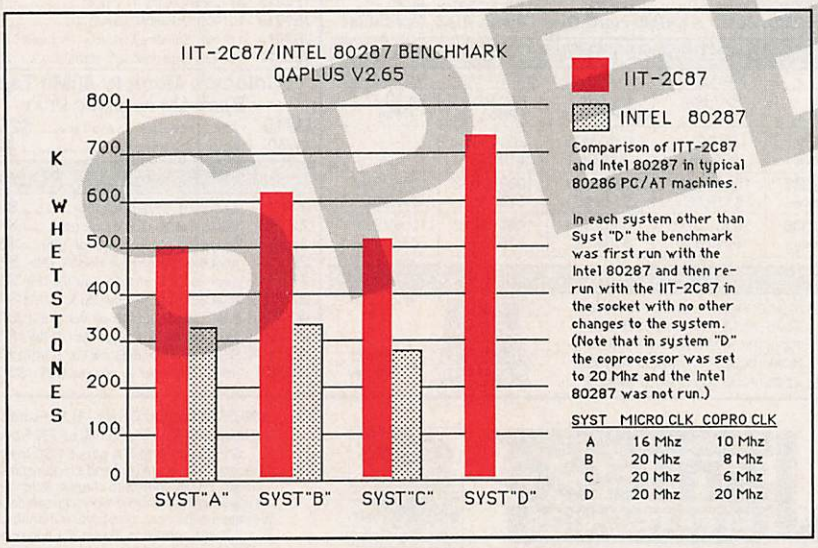
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IIT's 287 Coprocessor

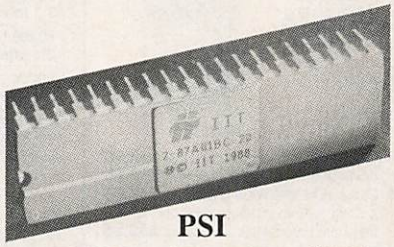
- Twice the speed of Intel's 80287 - 10 Mhz
- 100% Intel Compatible
- CMOS/NMOS Compatible
- Lower power for your laptop



Comparison of IIT-2C87 and Intel 80287 in typical 80286 PC/AT machines.

In each system other than Syst "D" the benchmark was first run with the Intel 80287 and then re-run with the IIT-2C87 in the socket with no other changes to the system. (Note that in system "D" the coprocessor was set to 20 Mhz and the Intel 80287 was not run.)

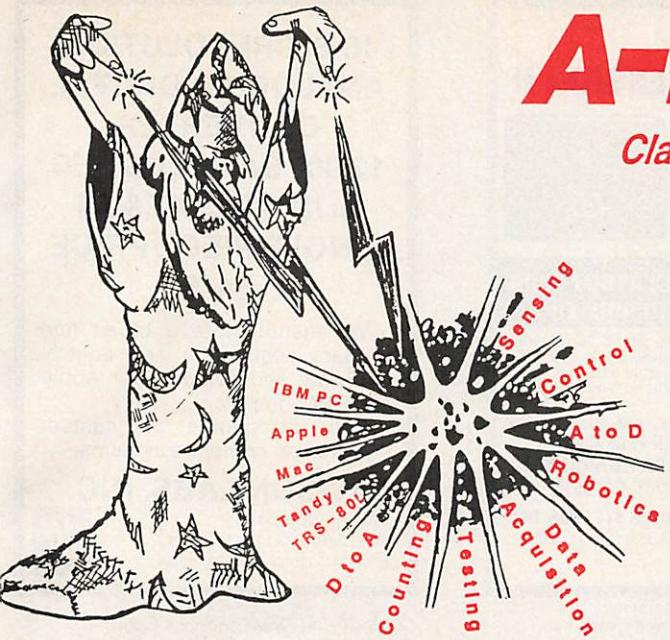
SYST	MICRO CLK	COPRO CLK
A	16 Mhz	10 Mhz
B	20 Mhz	8 Mhz
C	20 Mhz	6 Mhz
D	20 Mhz	20 Mhz



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It used to be difficult and costly to do process control, robotics, data acquisition, monitoring and sensing with your computer. Now the low-cost A-BUS system makes it easy to do almost any project you can imagine.

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Simplicity. You can start using the A-BUS in minutes. It's easy to connect, and software is a breeze to write in any language.

Reliability. Careful design and rugged construction make the A-BUS the first choice in specialized I/O.

An A-BUS system consists of: ▪ An A-BUS adapter plugged into your computer ▪ A cable to connect the adapter to 1 or 2 A-BUS function cards. ▪ The same cable will also fit an A-BUS Motherboard for expansion to up to 25 cards in any combination.

NEW: REMOTE A-BUS! Use the new Serial (RS-232) Adapter or Processor to control any A-BUS system. Cards can be up to 500 ft away using phone type cable, or off premises using a modem. Call or send for the new A-BUS Catalog which covers all the products.

Important

All A-BUS Systems: ♦ Come assembled and tested ♦ Include detailed manuals with schematics and programming examples ♦ Can be used with almost any language (BASIC, Pascal, C, assembler, etc.) using simple "IN" and "OUT" commands (PEEK and POKE on some computers) ♦ Can grow to 25 cards (in any combination) per adapter ♦ Provide jumper selectable addressing on each card ♦ Require a single low cost unregulated 12V power supply ♦ Are usually shipped from stock. (Overnight service is available.)

About Alpha Products

Founded in 1976 for the purpose of developing low cost I/O devices for personal computers, Alpha has grown to serve over 70000 customers in over 60 countries. A-BUS users include many of the Fortune 500 (IBM, Hewlett-Packard, Tandy, Bell Labs, GM...) as well as most major universities. A-BUS products are U.S. designed, U.S. built, and serviced worldwide.
Overseas distributors: England: Caldy Science Assoc. Ltd., Merseyside, 051 342 7033.
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Inputs, Outputs, etc.

Analog Input: 8 analog inputs. 0-5.1V in 20mV steps (8 bits). 0-100V range possible. 7500 conversions/second. **AD-142: $142**

12 Bit A to D: Analog to digital converter. Input range -4V to +4V, expandable to 100V. On-board amplifier. Resolution 1mV. Conversion time 130ms. 1 channel. (Expand to 8 channels with the RE-156 card.) **AN-146: $153**

Relay Card: 8 individually controlled industrial relays each with status LED's (3A at 120VAC contacts, SPST). **RE-140: $142**

Reed Relay Card: 8 reed relays (20mA at 60VDC, SPST). Individually controlled and latched, with status LEDs. **RE-156: $109**

D/A converter: 4 Channel 8 Bit D/A converter with output amplifiers and separate adjustable references. **DA-147: $149**

24 line TTL I/O: Connect 24 input or output signals (TTL 0/5V levels or switches). Variety of modes. (Uses 8255A) **DG-148: $72**

Digital Input: 8 optically isolated inputs. Input can be 5 to 100V voltage levels or switch closures. **IN-141: $65**

Digital Output Driver: 8 outputs: 250mA at 12V. Drive relays, solenoids, stepper motors, lamps, etc. **ST-143: $78**

Clock with Alarm: Powerful clock/calendar. Battery backup. Timing to 1/100 sec. Alarm relay, LED and buzzer. **CL-144: $98**

Touch Tone Decoder: Each tone is converted into a number which is stored on the board. **PH-145: $87**

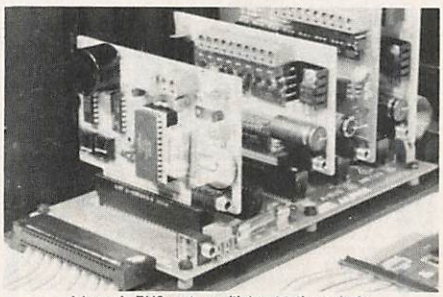
A-BUS Prototyping card: 4x4.5" card. Will accept up to 10 I.C.s. With power & ground bus. **PR-152: $16**

Counter Timer: Three 16 bit counters/timers. Use seperately or cascade for long (48 bit) counts. **CT-150: $132**

Call our application engineers to discuss your project.

Motion Control

Smart Quad Stepper Controller: The world's finest. On board microprocessor controls four motors simultaneously. Uses simple English commands like "MOVE ARM 10.2 (INCHES) LEFT". For each axis, you control coordinates (absolute or relative), ramping, speed, units, scale factors, etc. Many inputs for limit switches, etc. On the fly reporting of speed, position... Built in drivers for small motors (such as MO-103 or 105). **SC-149: $299**
Options: ► 5 amp/phase power booster for 1 motor: **PD-123: $49**
► Remote "teach" keypad for direct motor control: **RC-121: $54**



A large A-BUS system with two Motherboards
Adapter in the foreground plugs into PC,XT,AT type slot.

Stepper Driver Kit: For experimenting with stepper motors. Includes 2 MO-103 motors and a ST-143 dual driver **PA-181: $99**

Stepper Motors: (4 phase, unipolar)
MO-103: 2¼" dia. ¼" shaft, 7.5°/step, 12V, 5 oz-in torque. **$15**
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MO-105: 1.7" square. .2" shaft, 3.75°/step, 12V, 6 oz-in. **$15**

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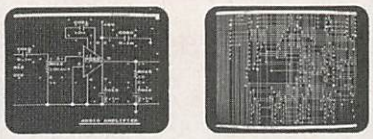
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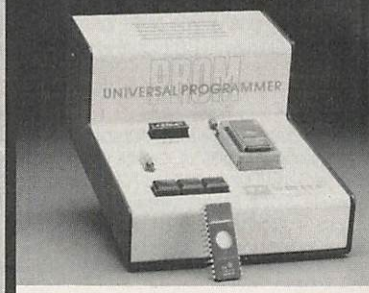
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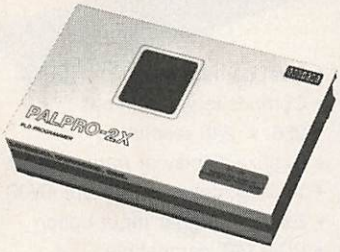
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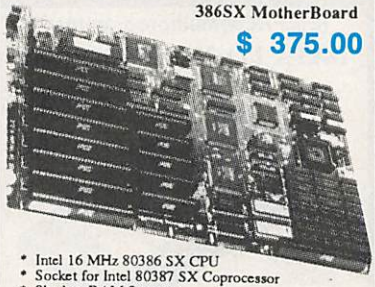
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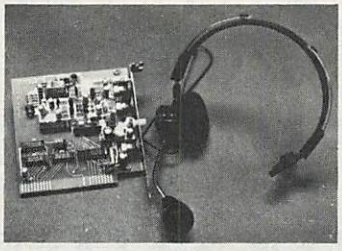
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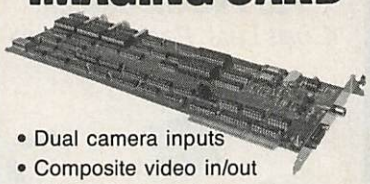
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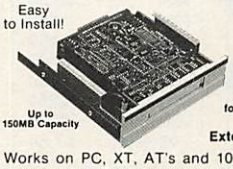
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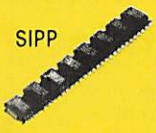
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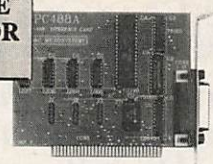
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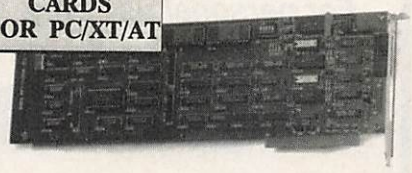
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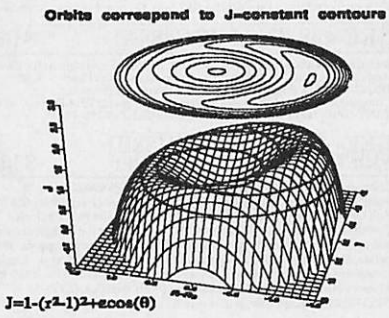
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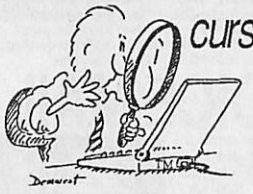
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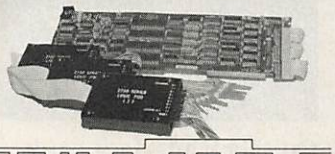
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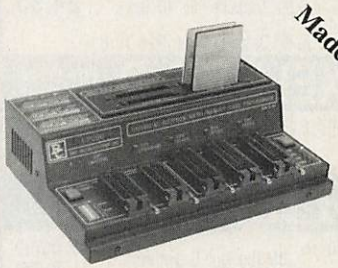


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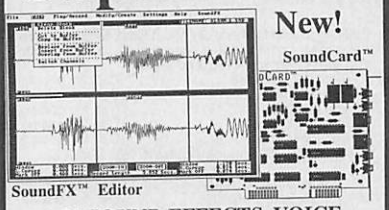
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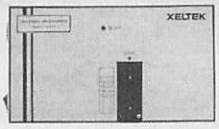
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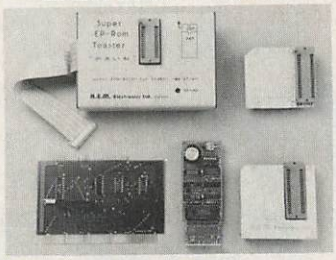
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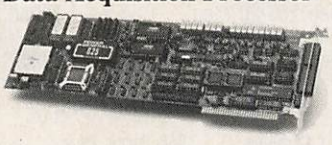
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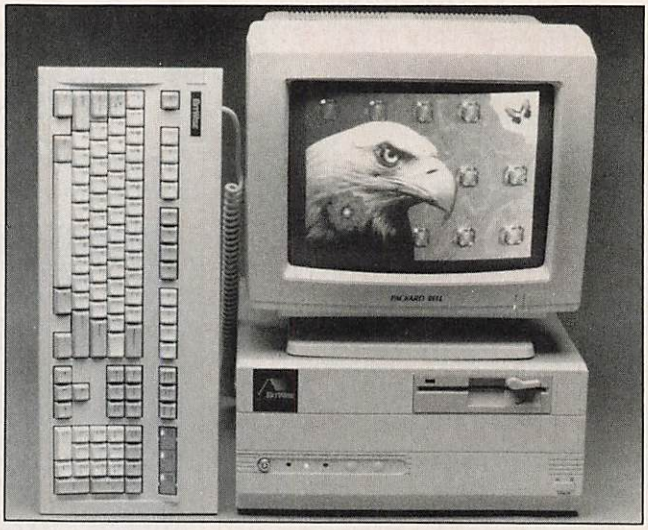
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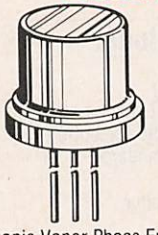
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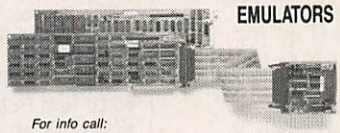
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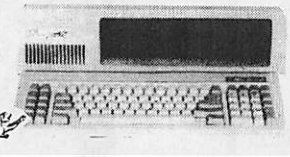
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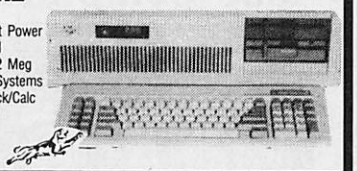
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64 x 1	2.00	2.50	2.95	3.95
64 x 4	4.75	5.25	5.75	6.75
256 x 1	3.00	3.25	3.95	4.95
1 Meg x 1	11.00	11.75	12.25	13.25
256 x 4	12.50	14.00	15.00	17.00
64x4 Video	6.00	7.00	8.00	11.00
1 Meg Video	—	24.00	—	—
8K x 8 Static	7.00	8.00	9.00	11.00
NEC V-20 — 8MHz				7.00

The above Memory Upgrades come in DIP Form. Please specify if you need ZIP - Soj - PLCC - Flat Pack or if you need Nibble Mode

MODEMS BY EVEREX

MNP ADD $20

EV-923 EverCom 12 300/1200 bps Bitcom Software.... 69.00
EV-941 EverCom 24 2400 Baud Int. Bitcom Software... 139.00
EV-945 External 2400 Baud 199.00
EV-942 2400 PS2 .....229.00 **EX-955** FAX Card 349.00

Level 4MNP 19.00 **MORE MODEMS...** Level 5MNP 39.00

1200 Baud Internal w/Software 54.00
1200 Baud External fully Hayes Compatible 99.00
2400 Baud Internal ½ card w/software CPI 99.00
2400 Baud External Fully Hayes Compatible, Zoom 129.00

Imtec/SAMSUNG MONITORS

1256A 12" Amber w/Tilt & Swivel Base 89.00
1257 12" Amber Flat Screen 720 x 350 ..... 109.00
1464 14" Color 640 x 200, 16 colors 239.00
1453 14" EGA 640 x 350. 64 colors/.31 ..... 369.00
1455N EGA 720x480 *Multisync Compatible* 449.00

VIDEO CARDS BY EVEREX

EGA EV659, 640 x 350, Auto Switch 119.00
VGA Viewpoint 16 Bit 256 Exp 512k 269.00

MORE VIDEO CARDS...

MonoGraphics or Color Graphics (Hercules Compatible)... 44.50

MEMORY FOR ALL COMPUTERS

IBM PS2

Description	Equiv. IBMPS2 Part #	For Model #	Meads Low Price
512K Upgrade	30F 5348	30/286	149.00
2MB Upgrade	30F 5360	30/286	459.00
1MB Module	6450603	70-E61 & 121	239.00
2MB Module	6450604	70-E61 & 121	499.00
2MB Mem. Board	6450608	70-A21	599.00
1MB Mem. Board	6450375	80-041	419.00
2MB Mem. Board	6450379	80-111 & 311	899.00

COMPAQ

Description	Equiv. Compaq Part #	For Model #	Meads Low Price
1MB Add-on Module	113131-001	386/20/25/20e/286E	359.00
1MB Add-on Module	113646-001	Deskpro 386S	369.00
4MB Add-on Module	113132-001	386/20/25/20E/286E	898.00
4MB Add-on Module	112534-001	Deskpro 386S	998.00
1MB Memory Exp. Bd.	113644-001	Deskpro 386/20e	499.00
1MB Memory Exp. Bd.	113633-001	Deskpro 386S	499.00
4MB Memory Exp. Bd.	113645-001	Deskpro 386/20e	1399.00
4MB Memory Exp. Bd.	113634-001	Deskpro 386S	13990
1MB Mem.Upgrade Kit	107651-001	Portable 386	499.00
1MB Memory Exp. Bd.	117428-001	286E	499.00
4MB Memory Exp. Bd.	117429-001	286E	1399.00
1MB Upgrade Bd.	110235-001	SLT/286	599.00
4MB Upgrade Bd.	108070-001	386/16	1399.00

IBM & Compaq boards & Modules come with 1 year warranty and are manufactured on a 2nd party board.

SIMM MODULES

Description	150NS	120NS	100NS	80NS
64 x 9 IBM & Compatibles	19.00	29.00	34.00	39.00
256 x 8 For Apple Products	39.00	44.00	49.00	59.00
256 x 9 IBM & Compatibles	42.00	48.00	59.00	64.00
1Meg x 8 For Apple Products	129.00	139.00	149.00	169.00
1Meg x 9 For IBM & Compatibles	139.00	149.00	159.00	169.00

HP LaserJet		Memory Boards	
1Meg	299.00	0-3Meg	109.00
2Meg	399.00	0-3Meg PS2	249.00
4Meg	699.00	0-10Meg	179.00
		0-8Meg PS2	399.00

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ST138 30Meg 40 Mil ½ Ht 3½" Drive only 299.00
ST225 20Meg w/cont. & Cables 259.00
ST238 30Meg w/cont. & Cables 289.00
ST251 40Meg ½ HT 40 Mil w/software, Drive only 349.00
ST251-1 40Meg, 28 Mil Sec, Drive only 359.00
ST277R 60MB 40 Mil ½ Ht 449.00
ST4026 20Meg Full Ht 40 Mil 299.00
ST4038 30Meg 40 Mil Full Ht 399.00
ST4053 40MB 28 Mil Full Ht 519.00
ST4096 80Meg Full HT w/software 28 Mil Sec. 639.00

WESTERN DIGITAL CONTROLLERS

WX-1 8 Bit ½ Sized for XT 79.00
MM2 16 Bit Full Sized Hard/Floppy 119.00
WD-27X 8 Bit RLL ½ Size 89.00
WAH 16 Bit Hard Drive Controller 129.00
RA2 16 Bit RLL Hard/Floppy for AT 159.00
MEAD Floppy Disk Controller for XT 19.00
MEAD 1.2 Meg & 360K Controller for XT, 720K-1.44 ... 69.00
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Mitsumi FLOPPY DRIVES

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1.44 Meg 3½" Drive w/5¼" mounting — Mitsumi 109.00
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160K Tandon TM100-1 Full Ht 59.00
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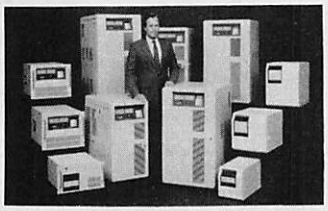
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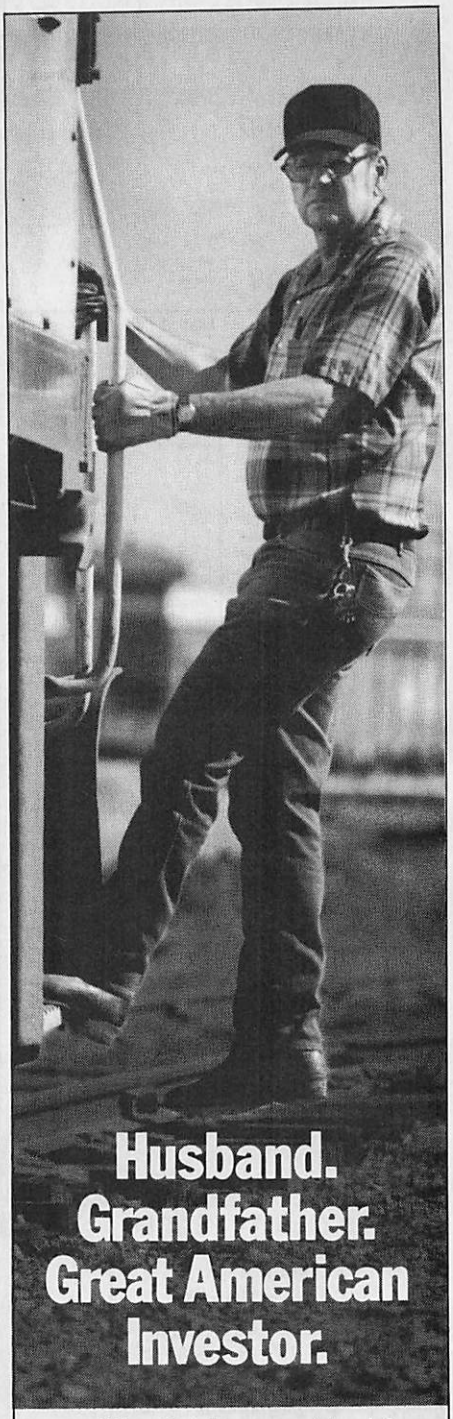
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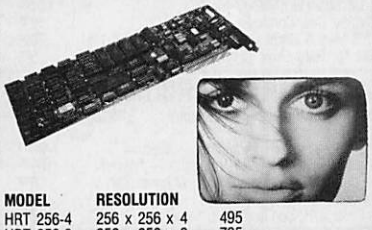
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HRT 256-8	256 x 256 x 8	795
HRT 512-8	512 x 512 x 8	995
HRT 512-24	512 x 512 x 24	1995

- IBM PC/XT/AT COMPATIBLE
- DIGITALIZE IN REAL TIME
- COMPOSITE VIDEO IN
- 24 BIT RGB OUT except model HRT 256-4
  16 level gray scale out
- SOFTWARE LIBRARY OF IMAGE ANALYSIS ROUTINES
- FREE SOFTWARE UPGRADES TO REGISTERED OWNERS
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HRT
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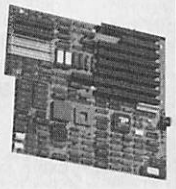
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Computers for the Blind

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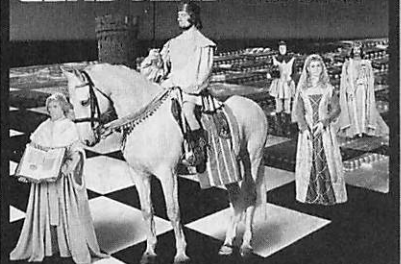
The answers can be found in *The Second Beginner's Guide to Personal Computers for the Blind and Visually Impaired* published by the National Braille Press. This comprehensive book contains reviews, written by blind users, of software that works with speech.

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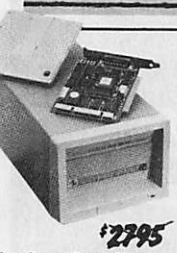
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tical storage is the perfect medium for maintaining "on line" grams or other static data. Ideal for catalogs, part lists or any plication where random accessibility is required.

e ISI/525 is available in IBM internal configuration but an exter- enclosure may be added. Supplied with one cartridge, ESDI/ controller, cable and transparent optical software. For addi- al information, contact Steven in our technical support depart- nt (213) 217-1947. The ISI/525 is a current production drive.



$539 CD/ROM Complete Kit

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se 430 external system $539	NEC interface kit for above 159
hi 1503S External system 695	Sony CD/510 internal drive only ..559
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ifornia Digital has all the components needed to customize your own nputer. Buy as much computing power as you need now, and up grade en the need arises. Here are some examples of components available:

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watt AT power supply 59	**I/O PLUS, Ser/Par'l. clock, game 59**
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40 Meg. Tape Back-up $179 ~~$659~~



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need to purchase a separate tape controller... the Alloy/40 attaches directly our existing floppy disk controller. Supplied software allows your computer ack up any time Day or Night. Come back in the morning and 40 megabytes replacable data has been stored on one Scotch DC/2000 data cassette.
k up entire hard disk, modified files only, or by file name. Loss of data is vitable but when you are backed up on an Alloy/40 its not a catastrophe. del 250 for PC/XT $179; Model 500 for AT $239.



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Original price was over $3000, now is your chance to purchase a DEST scanner for only $559.



Saba Scanner $359

~~$1299~~

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SCANNERS

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page scanner with OCR software	1299	359
hand held scanner with OCR soft.	799	159
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2000 edge feed scanner	935	719
MICROTECH300G 256 gray scales	2195	1759
DFI HandiScan 300 with Halo	359	199
PRINCETON GRAPHICS LS-300	1095	789
PANASONIC		
RS505 Image page scanner	1499	999
RS506 Page scanner	1899	1259



NEC/890 Laser $3095

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PRINTERS

HEWLETT PACKARD		
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Laser Printer II/D double sided	3995	2995
QMS PS/810 2 Meg., 35 fonts, Post/S.	5495	3879
APPLE Laser Writter NT	4550	3659
NEC890 Postscript, 3 meg	4975	3095

DIGITIZERS

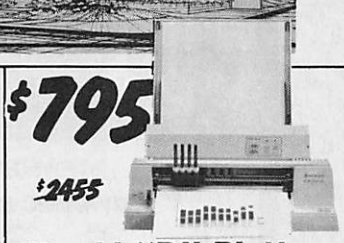
HITACHI		
HDG 1212 Puma 12x12"	595	359
HDG 1515 15x15	969	659
Tiger 1111C, 12x12 stylus extra	727	487
HDG 3648, 36x48"	5357	3995
SUMMAGRAPHICS		
Summa 1201 plus 12x12"	599	379
TB 3648, 36x48"	4748	3729
KYE Genius Tablet w/4 but. mouse	599	279
CALCOMP		
25180, 12x18"	1275	999
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DMP 52 single pen, 16 ips, C&D	3295	2495
DMP 56C size A-E, 16 ips	5695	3095
DMP61 single pen, 32 ips, A-D	4295	3095
PC695A 4 pen, size "B" 3 ips	799	595
CALCOMP PLOTTERS		
1023 Artisan A-D, 8 pen, 30 ips	4895	3795
1043GT size A-E, 8 pen, 24 ips	7995	5495
HEWLETT PACKARD		
7475A 6 pen size "B"	1895	1495
7550A 8 pen size "B" 32 ips	3900	2995
7595A 8 pen, size A-E, 24 ips	9990	7595
HITACHI PLOTTERS		
673/BM 4 pen, size "B" auto feed	2455	795
675 size "A-D" 8 pen	5600	2995
FUJITSU Imagegraph, 6 pen, 11x 32...	1295	895
IOLINE PLOTTERS		
LP3700 size E, 10 ips	4195	3195
LP3700MP 8 pen size "E" 10 ips	4695	3495
ROLAND PLOTTERS		
DPX2000 size "C" 8 pen with stand	2995	2195
DPX3300size"D" 8 pen with stand	4995	3495
ENTER COMPUTER		
SP600 size "B" 6 pen	995	659
SP1000 single pen size A-D	3995	2795
JDL 850, size "C" one meg. memory	3845	2789
VERSATEC 8524 Electrostatic	16,900	13789
NUMONICS		
5460 size "A-D"	2495	1859
5860 size "A-D" 8 pen	7495	5759

CAD SOFTWARE

AUTODESK		
AutoCad version 10,	2995	2195
AutoSketch Std & Enhanced 2.0	99	79
VERSACAD Designer	2995	1995
GENERIC CAD level 1	49	35
AMERICAN SM. BUS'N. Design Cad	299	179



EGA Color Monitor $219

Ideal for CAD/CAM and Desk Top publishing applications. The Roland CD/240 color monitor has a resolution of 720 pixels by 400/480 lines on a .31mm dot pitch 12" non-glare screen. VGA specifications in text mode EGA in graphic mode.
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40 Megabyte Hard Disk Kit $359

Forty megabyte internal hard disk drive, controller and cables all for only $359.
The kit includes the a 40 millisecond Miniscribe 3650 drive and a half slot Western Digital controller.





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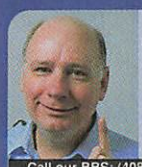
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Some programs benefit more than others, in particular, those that make heavy use of Floating Point, Trigonometric, Logarithmic and Exponential calculations show the most improvement. CAD, spreadsheets, some databases, and Mandlebrot programs are frequently written to use a co-processor if it's available.

How much your application will speed up depends on the ratio of time spent on math calculations versus other operations. A 3 to 10 times improvement is not uncommon certain operations are even faster.

The co-processor you need is specific to the type and speed of processor. For 8088/86 and 80386 based machines, the general rule is to use an 8087 or 80387 of the same speed as the processor, i.e. an 80386-25 requires an 80387-25.

80286 based machines frequently use a co-processor running at 2/3rds the processor speed, i.e. an 80286-12 requires an 80287-8.

Derick Moore, Director of Engineering

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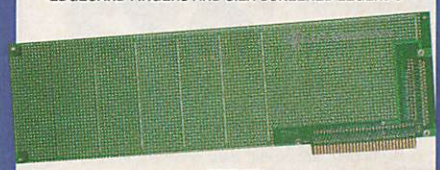
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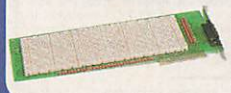
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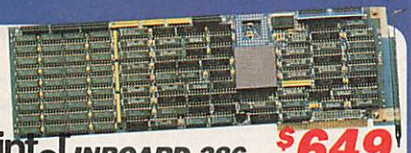


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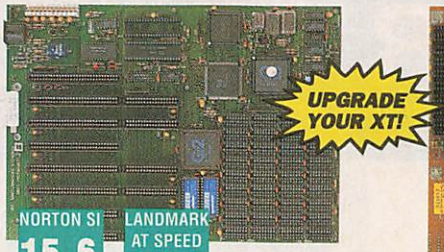
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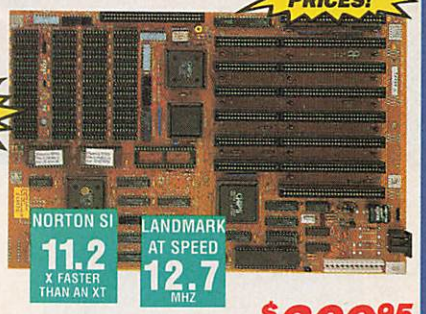


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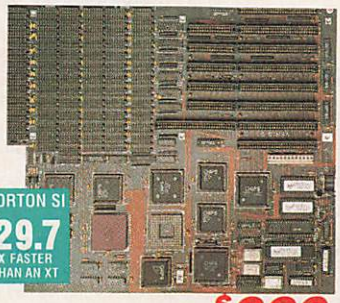
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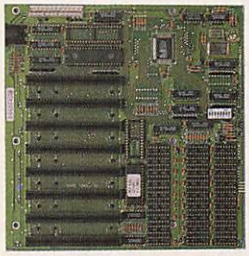


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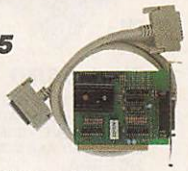
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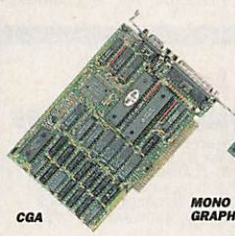
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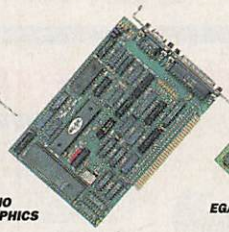
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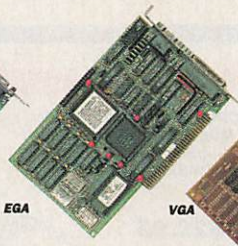
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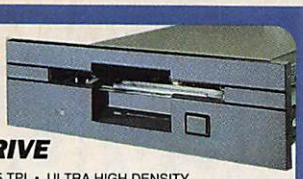
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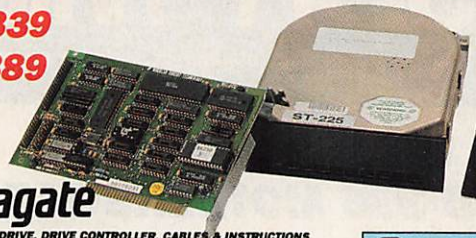
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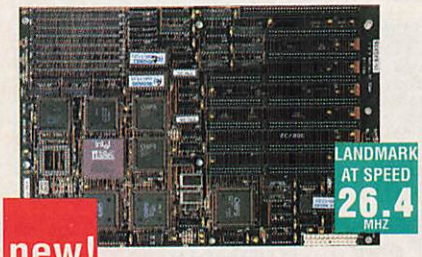
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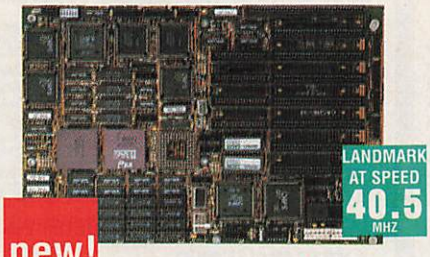
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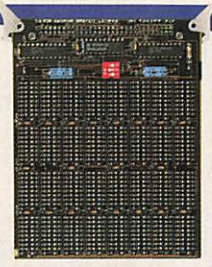
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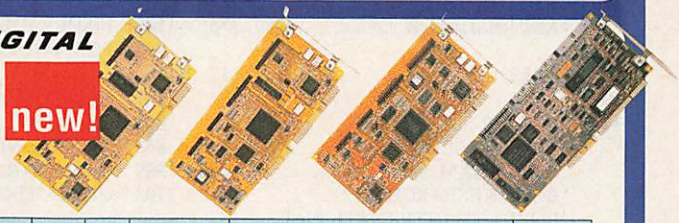
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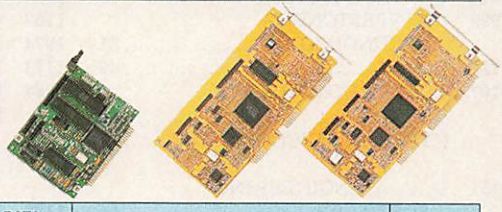
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COMING UP IN BYTE

The following articles are in the works for the December issue. Unless something unexpected happens, we'll be able to present them all.

PRODUCTS IN PERSPECTIVE:

One of the perennial buzzwords in computing is CASE (computer-aided software engineering). What is it? How well do CASE products perform, and what do they offer? Our December **Product Focus** zeros in on the subject.

System reviews will concentrate on two new 80386 machines from Acer and ADC.

In the **hardware review** category, we have a roundup of Macintosh 32-Bit QuickDraw boards and QMS's new ColorScript printer, which promises color PostScript at a groundbreaking price.

Software reviews include Common View, a C++ class library for Windows and Presentation Manager, and Watcom 386 C, a compiler that taps the full power of Intel's 80386.

Scheduled **application reviews** are Planet Software's library of functions that links Clipper applications to SQLBase; Hewlett-Packard's Accelerated X Window Display Server (AXDS/PC), an excellent budget saver for departments needing to turn IBM PC ATs into quality color X Window user stations; Publish It for the Mac; and Project Scheduler 4, the first midrange, graphically based project management software for the PC.

Our new **Reviewer's Notebook** section has articles on Aura Systems' ScuzzyGraph II, which gives other Macs the high resolution and color of their Mac II cousins; Visible Software's Dr. Pascal; The Rendition II, a medium- to high-resolution (1024- by 768-pixel) graphics controller for IBM PC ATs and compatibles from Renaissance GRX; and a second look at an updated United Innovations' wall-mount Mural 8000 plotter.

IN DEPTH:

The elusive dream of AI, something that has yet to materialize in a substantial form, is an ongoing quest for software and hardware designers. But some of our five primary senses have been replicated with mixed results. For some specialized tasks, mechanized "seeing," "hearing," and "speaking" have emerged at levels competitive with—and sometimes beyond those of—flesh and blood. For most other tasks, however, these computer-based "senses" are still woefully inadequate. Our In Depth section will concentrate on this burgeoning field of **sound, voice, and image processing**.

FEATURES:

This is the tenth anniversary of a product class, **the spreadsheet**, that many credit with first breaking the ice for the personal computer in business situations. How has the spreadsheet fared over the past decade, and what do its developers think now of their electronic progeny? Tune into the December Features section for some interesting answers.

Also slated for December, Dick Pountain has written a piece on the **Occam Transpiler**, now under development, which will make writing software for parallel processing easier.

Also, look for the regulary scheduled features of our columnists in both the **Expert Advice** and **Hands On** departments, industry news in **Microbytes**, new hardware and software of note in **What's New**, and the latest in noteworthy items tested by BYTE staffers in **Short Takes**.

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A. What is your level of management responsibility?

1 ☐ Senior-level Management
2 ☐ Other Management
3 ☐ Non-Management

B. What is your primary job function/principal area of responsibility? (Check one.)

4 ☐ Administration
5 ☐ Accounting/Finance
6 ☐ MIS/DP/Information Center
7 ☐ Product Design and Development
8 ☐ Research and Development
9 ☐ Manufacturing
10 ☐ Sales/Marketing
11 ☐ Purchasing
12 ☐ Personnel
13 ☐ Education/Training
14 ☐ Other: _____

C. Please indicate your organization's primary business activity: (Check one.)

Computer-Related Businesses:

15 ☐ Manufacturer (Hardware, Software)
16 ☐ Computer Retail Stores
17 ☐ Consultants
18 ☐ Service Bureau/Planning
19 ☐ Distributor/Wholesaler
20 ☐ Systems House/Integrator/VAR
21 ☐ Other: _____

Non-Computer-Related Businesses:

22 ☐ Manufacturing
23 ☐ Finance, Insurance, Real Estate
24 ☐ Retail/Wholesale
25 ☐ Education
26 ☐ Government
27 ☐ Military
28 ☐ Professions (Law, Medicine, Engineering, Architecture)
29 ☐ Consulting
30 ☐ Other Business Services
31 ☐ Transportation, Communications, Utilities
32 ☐ Other: _____

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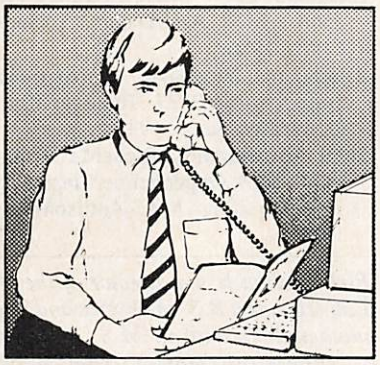
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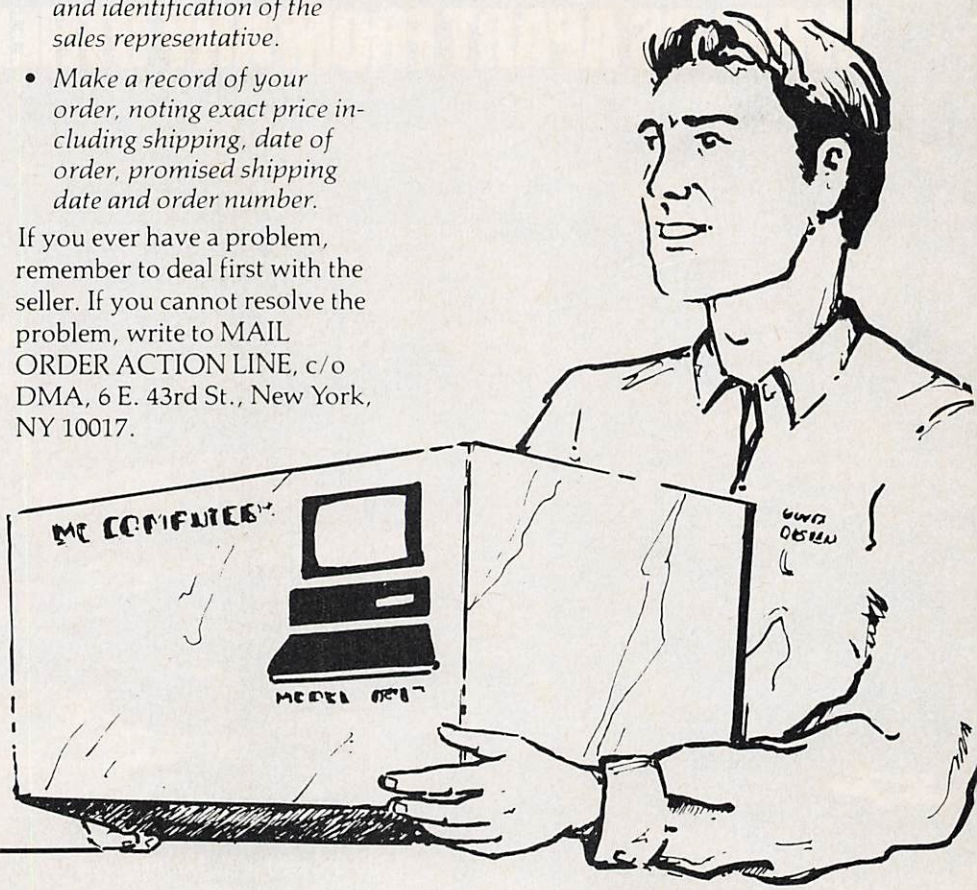
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continued from page 432

number and a buffer pointer. In my application, the first character of the message buffer contains either a "D"—indicating that the message buffer holds data—or an "E"—indicating that the message buffer is empty and the complete contents of the file have been transmitted. It's not unlike the way XMODEM works, only I don't supply any error-checking and correcting code. NetBIOS does that.

The heart of the program is a simple loop. The program reads a 1K-byte block from the file, places the data in the message buffer, and sends the message out using the `NBios_SessionSend()` function. The receiving end is doing much the same thing: receiving the data and writing it to the file, looping until it receives an EOF (End of File) block.

It's important to note that, once the session is established, the application issuing the CALL command has no special advantage over the application issuing the RECEIVE command. Communication between session partners is bidirectional; both sides of the session can send as well as receive.

Once the business of a session has concluded, both sides terminate the session by calling the HANG UP command. If any RECEIVE commands are pending, they're terminated. If any SEND commands are still awaiting completion, NetBIOS delays the HANG UP until those commands have either completed or timed out. My sample program follows the HANG UP command with a DELETE NAME command, clearing the local session name from the name table.

Hang Up

This has been only a brief foray into the coaxial-canopied jungles of networking. There's a great deal more to AppleTalk and NetBIOS that I haven't covered here; you'll have to explore it on your own. By now, however, you should be over your fear of network programming being something just this side of alchemy.

I've included a bibliography of some great sources of information on NetBIOS and AppleTalk. Like me, you'll be amazed at what you can do with software and hardware that—seen from the future of fiber-optic LANs stretching across the globe—will surely seem not much more than two tin cans and some string. ■

Editor's note: *This month's program comes in three parts. NETSEND.C sends a file via NetBIOS to the NETREC.C program. Both make use of a library of NetBIOS routines in NETLIB.C. All source code is available in a variety of formats. See page 5 for details.*

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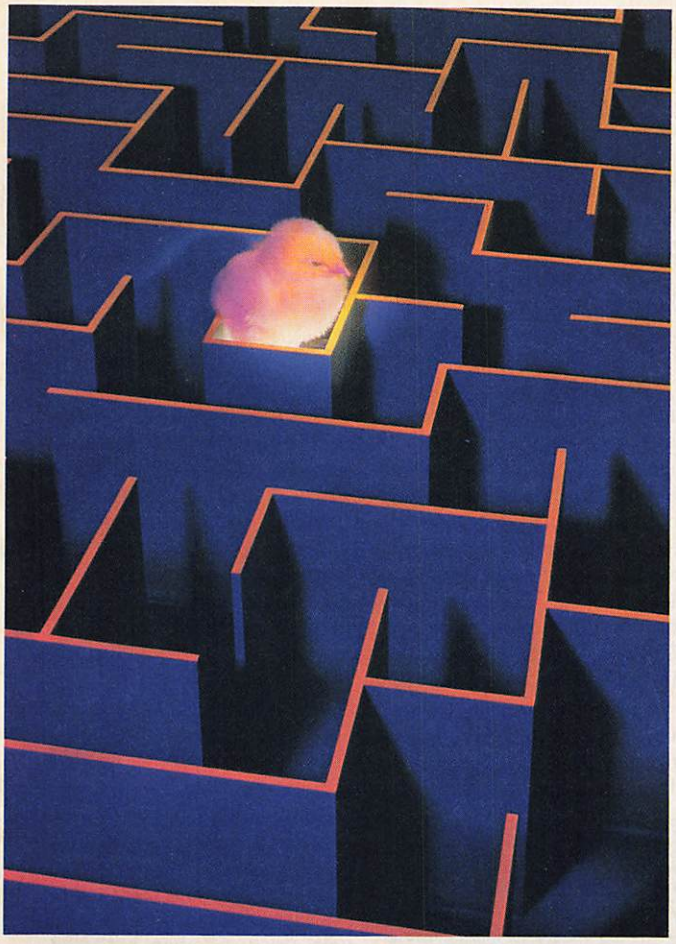
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Hugh Kenner

Bytes on Wings

BEYOND THE LIMITS:
Flight Enters the Computer Age

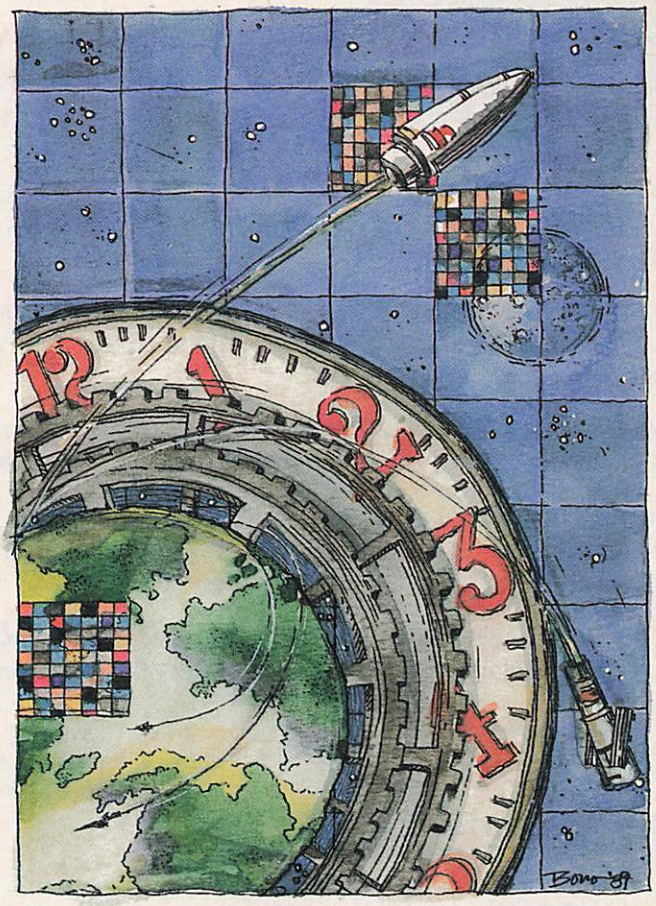
by Paul E. Ceruzzi

About 1800 it occurred to Napoleon that France, which had given the world the metric system, should also sponsor the world's first truly accurate log tables. When he snapped his imperial fingers, lo, it got done! It was done, in effect, by computer. High-level sages chose the algorithms. Programmers (as we'd now call them) worked out sequences of steps to transform each input into a multidigit real number. Now for the hardware. . . .

That consisted of numerous men with quill pens, seated at trestle tables on a vast gymnasium floor. This even pioneered the RISC philosophy, the men having been chosen for deft adding and subtracting, undistracted by any temptation to multiply or divide. The latter were dodges they had somehow never been taught, and specialists of their ilk were at a premium. Someone had observed that a man who added 3.99 to itself five times made fewer mistakes than a wise fool tempted by the highbrow shortcut of just multiplying 3.99 by 6. (The Greeks, by the way, had a word for wise fool: It's *sophomore*.)

Turn now to figure 2.5 of *Beyond the Limits*. In the late 1940s, little seems to have changed. We're in a "bull pen" at McDonnell Douglas, where an airplane is being designed. The photograph, which includes just a part of the room, is something that Franz Kafka might have hallucinated. In shirtsleeves, clutching ballpoints, perhaps 100 people hunch over papers. We're to imagine dozens more out of the frame to left and right; imagine, too, all of them putting in tense 8-hour days.

That's a snapshot of the computational machine that had put away the bad old times when "airplanes with structures too weak crashed, while others flew safely but poorly because they were overweight." For we now have "an adequate theory of structural analysis." Unhappily, it demanded millions of calculations.



Then somebody at Northrop Aircraft noticed in the accounting department an amenity the engineers didn't have: a vacuum-tube gizmo from IBM "that could multiply two numbers together and punch the results on a card in a few seconds." One got borrowed and was connected to another IBM machine that could print results on paper. And at IBM, where the policy of renting, not selling, equipment implied a captive customer unfree to make modifications, they were nonplussed at first, then alerted. Aha! "The basis for a new product they could sell to engineering firms that might otherwise not buy from IBM." That's the understatement of the century. Thus, 1949 gave us IBM's Card Programmed Calculator.

And we're off. The theme of Paul E. Ceruzzi's fascinating book is simply that the American computer industry was aerospace-driven from the very start. It was aerospace that *needed* all that number crunching. As I've noted in a previous column, astronomers also needed it. Astronomers, though, could never put federal billions on the table. The national interest is more tightly involved with the B-52 than with the orbit of Pluto.

The Pentagon, for years "the largest office building in the world," was built in 1942 to house myriad clerks doing what the erudite serfs in that McDonnell Douglas photo are doing: chores like working out how to "train a maximum number of pilots in a minimum time period with a minimum number of training airplanes and instructors."

That led to SCOOP (scientific computation of optimum problems), which by 1948 George Dantzig had reduced to sets of linear inequalities. Those sets—you guessed it—could finesse the problem, but they entailed scads of computation. (A sample query—what's in the cheapest bag of groceries with your minimum daily requirement of merely nine nutrients?—consumed 21 days at desk calculators.)

continued

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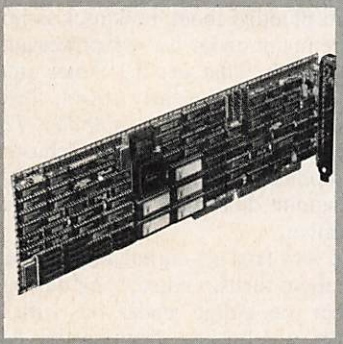
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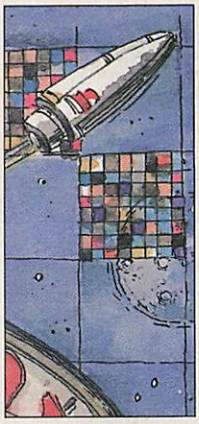
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By 1952 a Pentagon UNIVAC, exactly the second UNIVAC to be built, was crunching away at military SCOOPs. It weighed 15 tons, and just moving it into the Pentagon took three months. Today's equivalent sits on a desktop.

In 1953 IBM began shipping its answer to UNIVAC, Type 701. That rented for $15,000 a month. Of the 19 that were built, aerospace companies took 11. Two years later, the same companies were lining up for its successor, Type 704. You see the pattern.

We now pay the small sum we do for an IC because Air Force and NASA guidance drove the development of digital circuits.



Then there was missile tracking, which helped decide the analog-versus-digital face-off. To model something happening smoothly—moreover in real time, meaning fast enough for the model to be of any use—analog once seemed just the thing. Your nondigital watch is an analog computer. So, by one of Ceruzzi's neatest examples, is your car's differential gearing, which computes "a continuous weighted average" either when you're running straight or when you're rounding a curve and spinning the outer drive wheel faster than the inner.

Either way, "the differential gear distributes the engine's power so that the sum of the rotations of the two rear wheels is proportional to the rotation of the drive shaft." Now *that's* computation. And just seven toothed wheels can accomplish it. There's no time lag while we absorb numbers and get sums; and output is just what's wanted: torque, not more numbers.

The parallel with tracking a missile seems perfect: What we want is a correction to apply if it's veering off-course. Yet digital won, for the following two reasons. It suffers less from inaccuracy buildup as the problem gets more complex (and analog adds more gears). And it needn't be torn down and rebuilt from scratch each time we change the equation we want modeled.

Close as we are to the end of what we deem a digital century, it's hard for us to imagine how cogent such an issue could seem in our fathers' lifetime. Well, RAYDAC (1953) embodied a crucial decision: Do things digitally. When Raytheon installed RAYDAC at Point Mugu, it was state of the art: tape data storage, even parity checking! Although it did many things, it never did track missiles, its memory unit (sound pulses abounce in a tank of mercury) being too slow for real-time retrieval. But its sibling, Whirlwind, another Navy project, led to the Air Force's SAGE (for Semiautomatic Ground Environment), which was still monitoring North American skies as late as 1982. And "SAGE was the beginning of all systems, hardware and software."

But SAGE was *big*, and cramming a computerized guidance system into a Snark missile or, later, an Apollo capsule meant something *small*. True, Bell Labs hadn't developed the transistor with either aerospace or computers in mind. Yet "aerospace engineers will shave weight from anything they can"; by 1957 electronics made up half the cost of any missile, and "Air Force and NASA guidance drove the development of digital circuits in the 1960s." Which is why we now pay the trifling sum we do for an IC: hence the $10 calculator, the Walkman, and the home computer.

By 1965 IC pricing was down fivefold, to $12. The Air Force, the largest single purchaser, was arming hundreds of Minutemen at 2000 ICs each. And ICs since 1962 had been MIT's designated decision modules for the Block II Apollo Guidance Computer that it had under development for lunar landings. That happened under an MIT lab director named Charles Stark Draper. Asked (in 1960) when the equipment would be ready, he said, "Before you need it." Asked (incredibly), "How do we know you are telling the truth?," he said, "I'll go along and run it." (They didn't take him up, in any sense; by the time *Apollo 11* moon-landed, Draper was 68. His equipment, though, yes, all worked.)

It worked so well that alarms were set off that resonate yet. Can people and computers safely interact? Apollo (if you remember) meant detaching the lunar module from a vehicle in lunar orbit. The module was to (1) settle down on the moon; (2) stay while astronauts plodded about, took rock samples, and set up a flag; and (3) remount under its own power and rejoin the orbiter for return to earth. That was the choice among several scenarios fiercely debated in the early 1960s; for details, see Charles Murray and Catherine Bly Cox's *Apollo: The Ten-Year Race to Put a Man on the Moon* (Simon & Schuster, 1989), a book that tells the moon-shot story not, Tom-Wolfe-wise, from the astronautic viewpoint, but from what now seems more cogent, the administrative.

Well, in 1969 the very first all-digital autopilot had two jobs. One was deciding about thrust and steering during descent to the moon. The other was aiding rendezvous with the orbiter. And how its memory was limited! Nothing like disk drives—wires wound through ferrite cores. Splice in a feature, slice another out.

Alas, combined functions overloaded it by 13 percent, a glitch that tests failed to reveal. So on the last stages of the descent, an alarm no one could be sure about sounded repeatedly, and Houston went half mad, and Neil Armstrong's pulse rate hit its maximum (I'm not making this up), until he alighted with 24 seconds of reserve fuel. . . .

It was afterward that he thought up his famous words, "That's one small step for a man. . . ." Till then (so he told me in 1976), it hadn't occurred to him he'd better have something ready to *say*. The sweat must have been still on his brow.

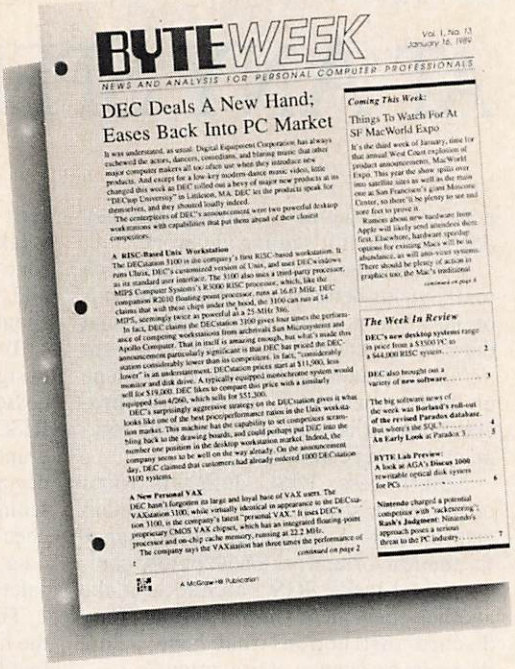
That alarm, though, keeps sounding. The computer's intolerance of ambiguity: Does that interfere with its usefulness to us, our ability to interact with it? That debate rages, muted because it's so seldom that we're dealing with life or death under a spotlight. I'll contribute: The computer is a difference detector. The human mind is a similarity detector. I'll go into what that implies another time.

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Hugh Kenner is a professor of English at Johns Hopkins University. His reviews have appeared in publications like the New York Times *and* Harper's. *His recent books include* A Sinking Island *and* Mazes. *He can be contacted on BIX as "hkenner."*

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NEWS AND ANALYSIS FOR PERSONAL COMPUTER PROFESSIONALS

DEC Deals A New Hand; Eases Back Into PC Market

It was understated, as usual. Digital Equipment Corporation has always eschewed the actors, dancers, comedians, and blaring music that other major computer makers all too often use when they introduce new products. And except for a few key modern-dance music video, little changed this week as DEC rolled out a bevy of major new products at its "DECtop University" in Littleton, MA. DEC let the products speak for themselves, and they shouted loudly indeed.

The centerpieces of DEC's announcement were two powerful desktop workstations with capabilities that put them ahead of their classist competitors.

A RISC-Based Unix Workstation

The DECstation 3100 is the company's first RISC-based workstation. It runs Ultrix, DEC's customized version of Unix, and uses DEC's windows as its standard user interface. The 3100 also uses a third-party processor, MIPS Computer Systems's R3000 RISC processor, which, like the companion R2010 floating-point processor, runs at 16.67 MHz. DEC claims that with these chips under the hood, the 3100 can run at 14 MIPS, seemingly twice as powerful as a 25-MHz 386.

In fact, DEC claims the DECstation 3100 gives four times the performance of competing workstations from archrivals Sun Microsystems and Apollo Computer. That in itself is amazing enough, but what's made this announcement particularly significant is that DEC has priced the DECstation considerably lower than its competitors. In fact, "considerably lower" is an understatement. DECstation prices start at $11,900, less monitor and disk drive. A typically equipped monochrome system would sell for $19,000. DEC likes to compare this price with a similarly equipped Sun 4/260, which sells for $51,300.

DEC's surprisingly aggressive strategy on the DECstation gives it what looks like one of the best price/performance ratios in the Unix workstation market. This machine has the capability to set competitors scrambling back to the drawing boards, and could perhaps put DEC into the number one position in the desktop workstation market. Indeed, the company seems to be well on the way already. On the announcement day, DEC claimed that customers had already ordered 1000 DECstation 3100 systems.

A New Personal VAX

DEC hasn't forgotten its large and loyal base of VAX users. The VAXstation 3100, while virtually identical in appearance to the DECstation 3100, is the company's latest "personal VAX." It uses DEC's proprietary CMOS VAX chipset, which has an integrated floating-point processor and on-chip cache memory, running at 22.2 MHz.

The company says the VAXstation has three times the performance of

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Coming This Week:

Things To Watch For At SF MacWorld Expo

It's the third week of January, time for that annual West Coast explosion of product announcements, MacWorld Expo. This year the show spills over into satellite sites as well as the main one at San Francisco's giant Moscone Center, so there'll be plenty to see and tore feet to prove it.

Rumors about new hardware from Apple will likely send attendees there first. Elsewhere, hardware upgrade options for existing Macs will be in abundance, as will anti-virus systems. There should be plenty of action in graphics too, the Mac's traditional

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The Week in Review

DEC's new desktop systems range in price from a $3500 PC to a $44,000 RISC system. 2

DEC also brought out a variety of **new software**. 3

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Nintendo charged a potential competitor with "hackneering"; **Rash's Judgment:** Nintendo's approach poses a serious threat to the PC industry. 7

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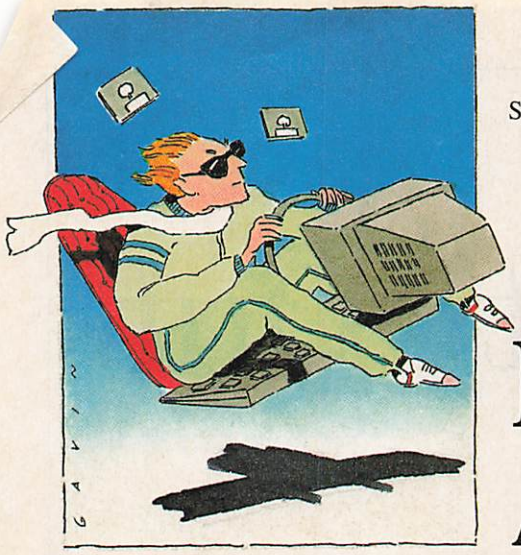
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STOP BIT ■ Dave Nelson

RISCs: Unsafe at Any Speed

Is the quest for more and more MIPS worth the RISC?

The newest technical workstations are powered by RISC microprocessors. These microprocessors will soon be available as coprocessors for personal computers, to speed up compute-intensive tasks such as image processing. Yet RISC microprocessors remain controversial, and for good reason.

RISC designers increase *average* instruction execution speeds by eliminating the complex, multiple-cycle instructions (e.g., floating-point arithmetic and character-string manipulation) found in conventional processors. The remaining instructions (typically register-to-register operations) can then be performed in one simplified machine cycle—the minimum number of steps in which an instruction can be executed.

And the discarded instructions? Their functions are taken over by software, auxiliary coprocessors, or cache-resident subroutines. In any case, they no longer detract from the MIPS (for millions of instructions per second) ratings of the RISC processor. RISC architects eagerly sacrifice instruction-set power to increase MIPS. Unfortunately, as Nick Tredennick (a senior IBM researcher who specializes in processor design) put it, "MIPS are like RPM: They tell you how fast the engine is running, but they don't tell you if it's doing any work."

Whether you think the RISC approach really yields better performance depends on how you measure performance—and there is no general agreement on how to *define* computer performance, let alone on how to measure it. In any case, processor speed is only one aspect of computer system performance.

Nevertheless, RISC designers focus on processor speed because it is the main determinant of computer performance for their favorite workloads: purely computational tasks. RISC architects make another convenient simplification: They discard instructions that have a low "average frequency of execution."

When an instruction, such as a multiple-character MOVE, is discarded due to low frequency of execution, its function is typically taken over by software. However, that MOVE operation will take much longer to execute as a software subroutine than as a "built-in" processor instruction. This increases the product of (frequency)×(duration) for that operation and *reduces* overall performance. One result of ignoring duration is that RISC processors sometimes take longer to process a given workload than CISC (complex-instruction-set computer) processors with lower MIPS ratings.

RISC designs also exacerbate the so-called von Neumann bottleneck, which exists when instructions and data are accessed over a single path that connects the processor with its main storage unit. Because a RISC instruction doesn't do much, a processor must access and execute lots of them to accomplish what it could do with a few multicycle instructions in a CISC processor. This consumes processor cycles, main storage accesses, and cache memory space.

To mitigate the effect of RISC's high ratio of instruction-to-operand access, RISC designers introduce complex auxiliary-support mechanisms, such as instruction pipelines and multiple register sets. These mechanisms, together with weak instructions, make system software for a RISC inherently more complicated, and thus less reliable, than the corresponding CISC software.

To speed instruction execution, RISC designers require all operands to be accessed from typeless registers. Thus, RISC processors acquire artificial operand uniformity at the expense of rendering operands typeless and thereby forfeiting processor-based type- and value-checking. Since incorrect operations on data values are a major source of errors, safety is being sacrificed for speed.

The RISC movement is also repeating the history of processor design, a history that began with simple, register-oriented instruction sets. "Enhanced" RISC processors have already appeared. They "extend" RISC processors with privileged (e.g., cache-resident) subroutines that perform "complex" operations (i.e., operations that actually process data).

RISC chips have had a lasting influence on processor design. In addition to providing tricks for increasing MIPS ratings, the conservative RISC approach has also inspired innovative processor designs. For example, some new minisupercomputers can execute several instructions per machine cycle due to multiple instruction-execution units, sophisticated synchronization circuitry, and complex compilers.

Safe processor architectures, such as object-oriented designs, are not yet in favor with computer designers. But the same parallelism that lets a processor execute multiple instructions per machine cycle can also support concurrent verification of data and program integrity. When computer designers realize this, they can design safe processors that also have terrific MIPS ratings. ■

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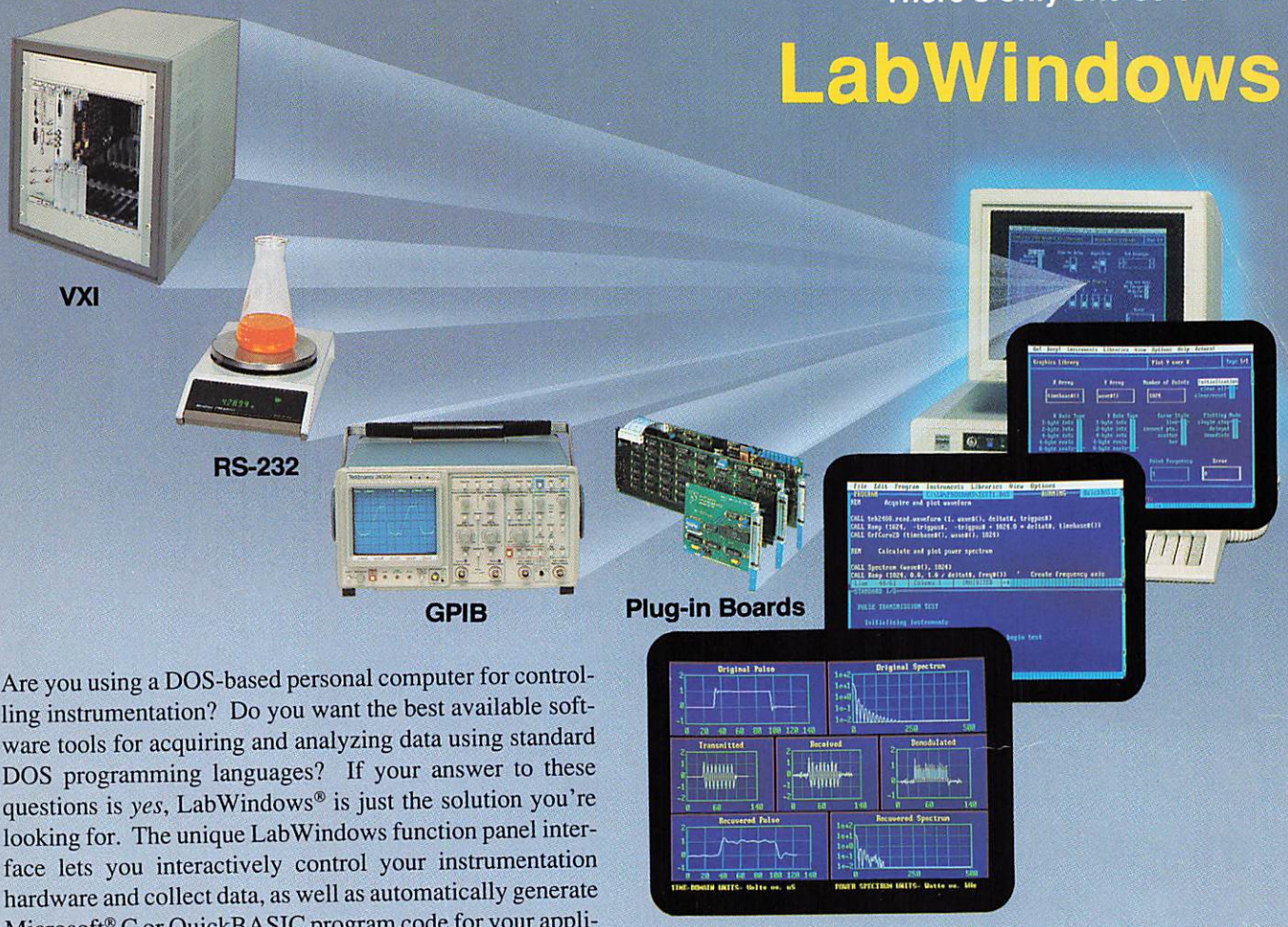
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